ULN2003B 高电压、高电流达灵顿晶体管阵列

1 特性

- 输出泄漏电流 (I_{CEX}) 超过 ULN2003A 的四倍
- 500mA 额定集电极电流（单路输出）
- 高压输出 50V
- 钳位二极管输出
- 可兼容各类逻辑的输入
- 继电器驱动器应用

2 应用

- 继电器驱动器
- 锤式驱动器
- 灯驱动器
- 显示屏驱动器（LED 和气体放电元件）
- 线路驱动器
- 逻辑缓冲器

3 说明

ULN2003B 是一款高电压、高电流达灵顿晶体管阵列。 这个器件包含 7 个高压输出型 NPN 达灵顿晶体管对，这些晶体管具有针对电感负载开关的共阴极钳位二极管。 单个达灵顿对的集电极电流额定值为 500mA。 将达灵顿对并联可以提供更高的电流。

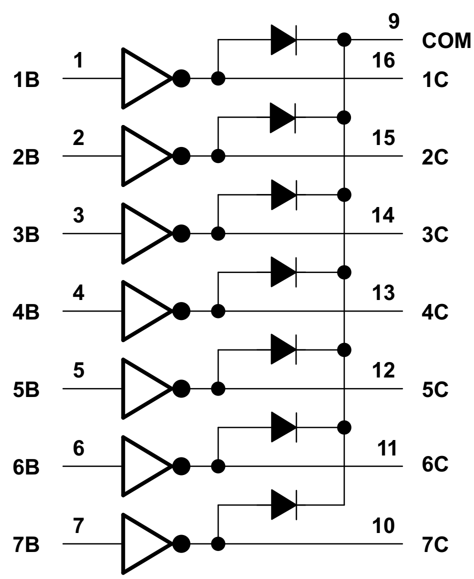
ULN2003B 的每个达灵顿对具有一个 2.7kΩ 基极串联电阻器，可直接用于晶体管逻辑 (TTL) 或互补金属氧化物半导体 (CMOS) 器件。

器件信息[1]

部件号	封装	封装尺寸（标称值）
ULN2003B	PDIP (16)	19.30mm x 6.35mm
	SOIC (16)	9.90mm x 3.91mm
	TSSOP (16)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



目录

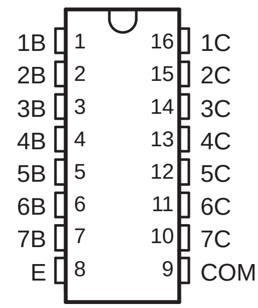
5 修订历史记录

Changes from Original (June 2014) to Revision A **Page**

- 完整版的最初发布版本。 ... 1

6 Pin Configuration and Functions

D, N, OR PW PACKAGE
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
<1:7>B	1 - 7	Input	Channel 1 through 7 darlington base input
<1:7>C	16 - 10	Output	Channel 1 through 7 darlington collector output
E	7	–	Common Emmitter shared by all channels (typically tied to ground)
COM	8	Input/Output	Common cathode node for flyback diodes (required for inductive loads)

7 Specifications

7.1 Absolute Maximum Ratings[1]

at 25°C free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Collector-emitter voltage			50	V
	Clamp diode reverse voltage[2]			50	V
V_I	Input voltage[2]			30	V
	Peak collector current[3][4]			500	mA
I_{OK}	Output clamp current			500	mA
	Total emitter-terminal current			–2.5	A
T_A	Operating free-air temperature range		–40	105	°C
θ_{JA}	Package thermal impedance[3][4]	D package		81	°C/W
		N package		49.7	
		PW package		105	
T_J	Operating virtual junction temperature			150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
(3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]		2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]		500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I		0	5	V
V_{CC}		0	50	V
T_J	Junction Temperature	-40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		ULN2003B		UNIT
		PW	D	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.4	81.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	32.9	40.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	51.3	38.9	
ψ_{JT}	Junction-to-top characterization parameter	2.1	10.9	
ψ_{JB}	Junction-to-board characterization parameter	50.6	38.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2003B			UNIT
					MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	图 12	V_{CE} = 2 V	I_C = 200 mA			2.4	V
				I_C = 250 mA			2.7	
				I_C = 300 mA			3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	图 11	I_I = 250 µA,	I_C = 100 mA		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6	
I_{CEX}	Collector cutoff current	图 8	V_{CE} = 50 V,	I_I = 0			10	µA
V_F	Clamp forward voltage	图 14	I_F = 350 mA			1.7	2	V
$I_{I(off)}$	Off-state input current	图 9	V_{CE} = 50 V,	I_C = 500 µA	50	65		µA
I_I	Input current	图 10	V_I = 3.85 V			0.93	1.35	mA
I_R	Clamp reverse current	图 13	V_R = 50 V				50	µA
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25	pF

7.6 Electrical Characteristics, T_A = –40°C to 105°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2003B			UNIT
					MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	图 12	V_{CE} = 2 V	I_C = 200 mA			2.7	V
				I_C = 250 mA			2.9	
				I_C = 300 mA			3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	图 11	I_I = 250 µA,	I_C = 100 mA		0.9	1.2	V
			I_I = 350 µA,	I_C = 200 mA		1	1.4	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.7	
I_{CEX}	Collector cutoff current	图 8	V_{CE} = 50 V,	I_I = 0			20	µA
V_F	Clamp forward voltage	图 14	I_F = 350 mA			1.7	2.2	V
$I_{I(off)}$	Off-state input current	图 9	V_{CE} = 50 V,	I_C = 500 µA	30	65		µA
I_I	Input current	图 10	V_I = 3.85 V			0.93	1.35	mA
I_R	Clamp reverse current	图 13	V_R = 50 V				100	µA
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25	pF

7.7 Switching Characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output			0.25	1	µs
t_{PHL}	Propagation delay time, high- to low-level output			0.25	1	µs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O ≈ 300 mA	V_S – 20			mV

7.8 Switching Characteristics, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output			1	10	µs
t_{PHL}	Propagation delay time, high- to low-level output			1	10	µs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O ≈ 300 mA	V_S – 50			mV

7.9 Typical Characteristics

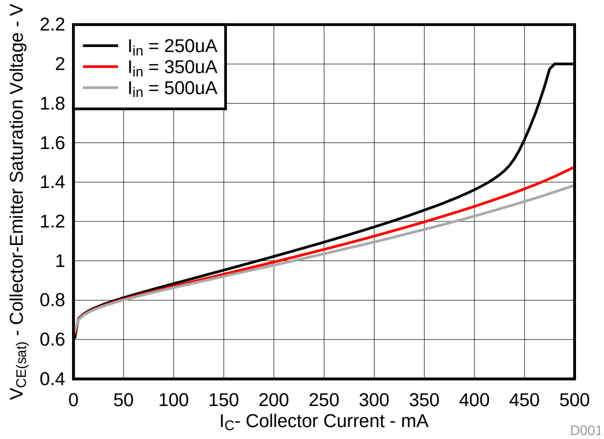


图 1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

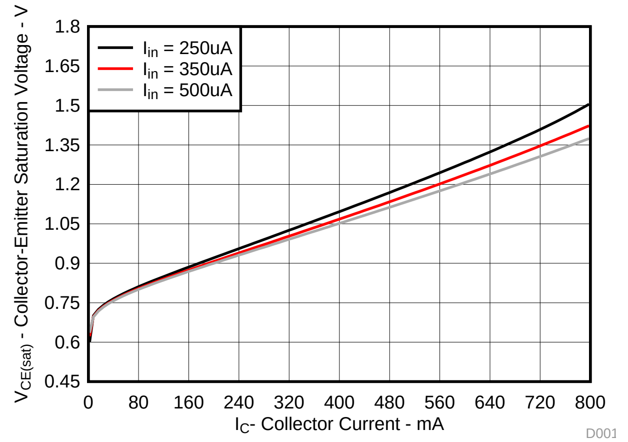


图 2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlingtons in Parallel)

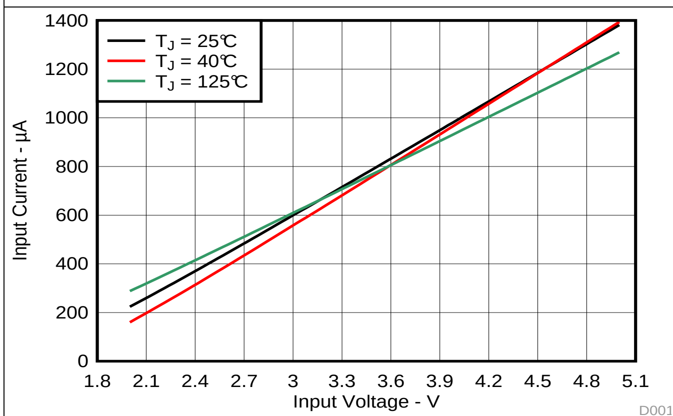


图 3. Input Current vs Input Voltage

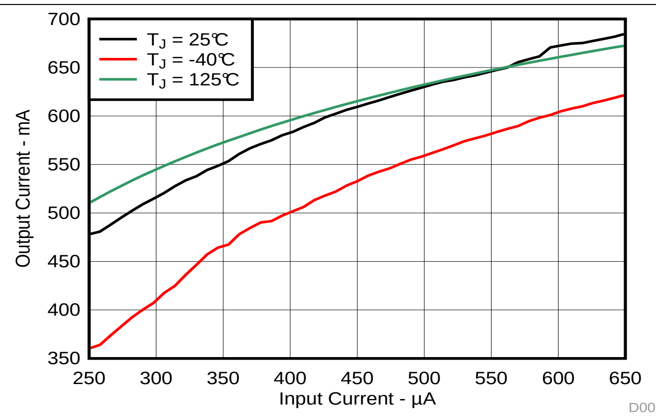


图 4. Output Current vs Input Current

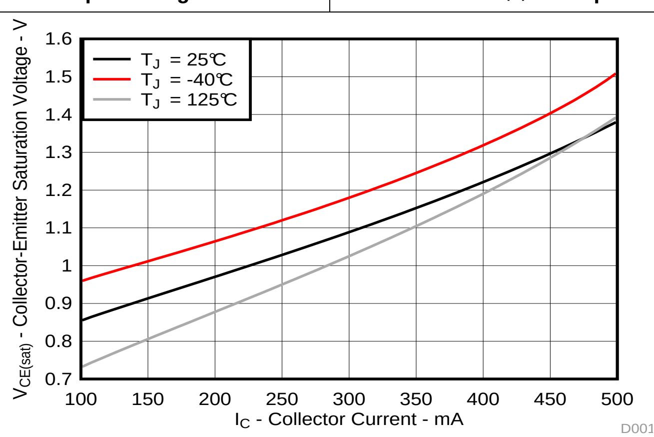


图 5. Collector-Emitter Saturation Voltage vs Collector Current

7.10 Thermal Information

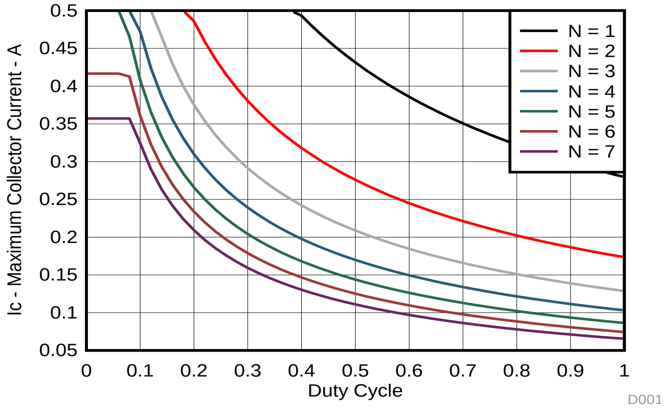


图 6. D Package Maximum collector Current vs Duty Cycle

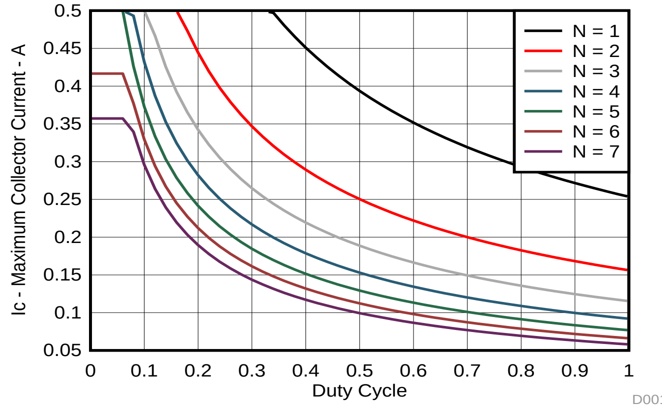


图 7. PW Package Maximum collector Current vs Duty Cycle

8 Parameter Measurement Information

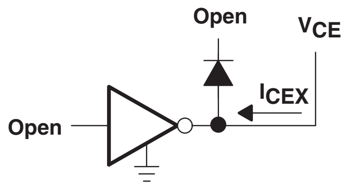


图 8. I_{CEX} Test Circuit

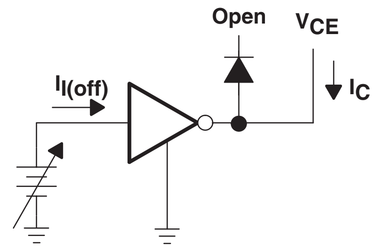


图 9. $I_{I(off)}$ Test Circuit

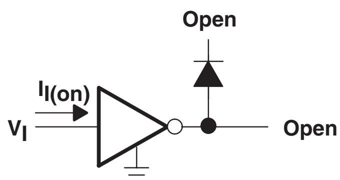


图 10. I_I Test Circuit

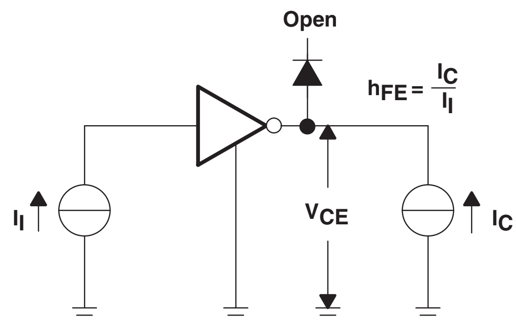


图 11. h_{fe} , $V_{CE(sat)}$ Test Circuit

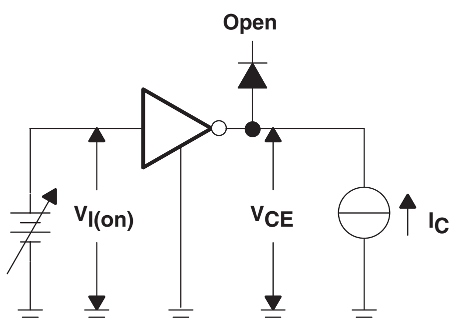


图 12. $V_{I(on)}$ Test Circuit

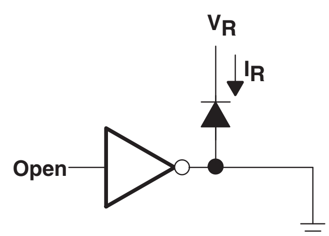


图 13. I_R Test Circuit

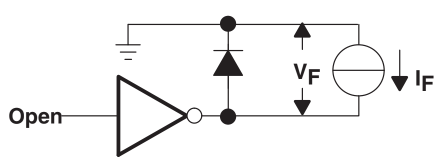


图 14. V_F Test Circuit

9 Detailed Description

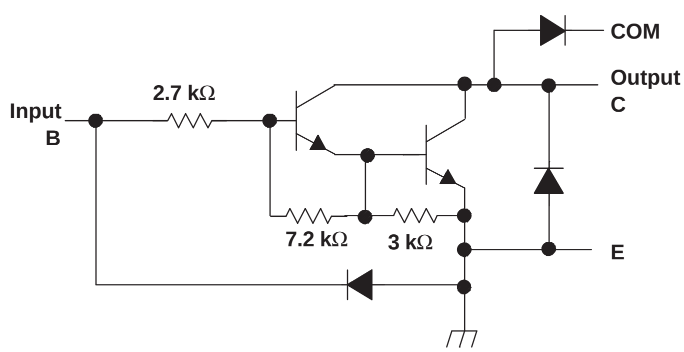
9.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This is due to it's integration of 7 Darlington transistors that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULN2003B comprises seven high voltage, high current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULN2003B has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5.0 V or 3.3 V. The ULN2003B offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

This device can operate over a wide temperature range (–40°C to 105°C).

9.2 Functional Block Diagram



All resistor values shown are nominal.

图 15. Schematic (Each Comparator)

9.3 Feature Description

Each channel of ULN2003B consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very high current gain (β2). This can be as high as 10,000 A/A at certain currents. The very high β allows for high output current drive with a very low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current via the 2.7 kΩ resistor connected between the input and base of the pre-driver Darlington NPN. The 7.2 kΩ & 3.0 kΩ resistors connected between the base and emitter of each respective NPN act as pull-downs and suppress the amount of leakage that may occur from the input.

The diodes connected between the output and COM pin is used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply via the kick-back diode.

In normal operation the diodes on base and collector pins to emitter will be reversed biased. If these diode are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

9.4 Device Functional Modes

9.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, ULN2003B is able to drive inductive loads and supress the kick-back voltage via the internal free wheeling diodes.

9.4.2 Resistive Load Drive

When driving a resistive load, a pull-up resistor is needed in order for ULN2003B to sink current and for there to be a logic high level. The COM pin can be left floating for these applications.

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

ULN2003B will typically be used to drive a high voltage and/or current peripheral from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of ULN2003B, driving inductive loads. This includes motors, solenoids & relays. Each load type can be modeled by what's seen in 图 16.

10.2 Typical Application

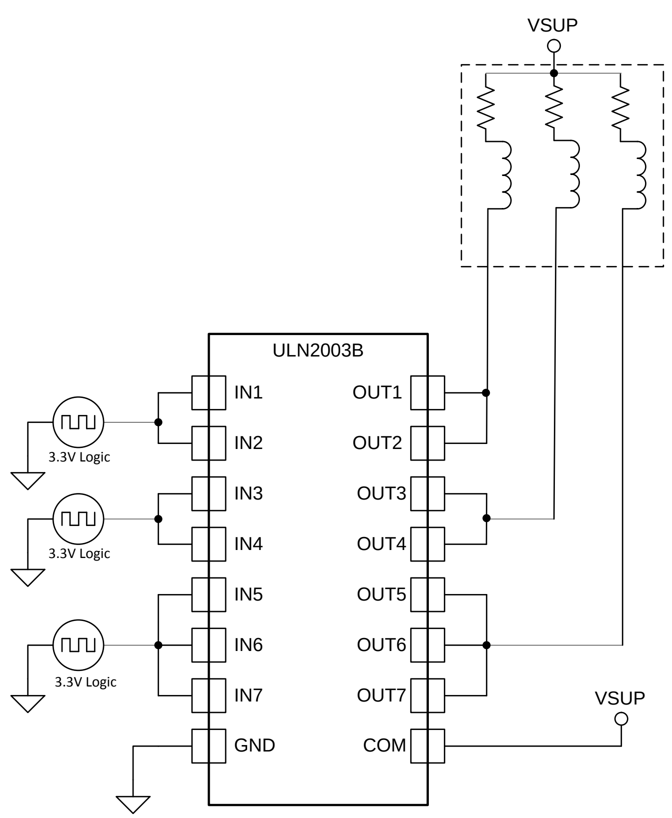


图 16. ULN2003B as Inductive Load Driver

Typical Application (接下页)

10.2.1 Design Requirements

For this design example, use the parameters listed in 表 1 as the input parameters.

表 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
GPIO Voltage	3.3 V or 5.0 V
Coil Supply Voltage	12 V to 48 V
Number of Channels	7
Output Current (R_{COIL})	20 mA to 300 mA per channel
Duty Cycle	100%

10.2.2 Detailed Design Procedure

When using ULN2003B in a coil driving application, determine the following:

- Input Voltage Range
- Temperature Range
- Output & Drive Current
- Power Dissipation

10.2.2.1 Drive Current

The coil current is determined by the coil voltage (VSUP), coil resistance & output low voltage (V_{OL} or $V_{CE(SAT)}$).

$$I_{COIL} = (V_{SUP} - V_{CE(SAT)}) / R_{COIL} \quad (1)$$

10.2.2.2 Output Low Voltage

The output low voltage (V_{OL}) is the same thing as $V_{CE(SAT)}$ and can be determined by, 图 1, 图 2, or 图 5.

10.2.2.3 Power Dissipation & Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. The number of coils driven can be determined by 图 6 or 图 7.

For a more accurate determination of number of coils possible, use the below equation to calculate ULN2003B on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li}$$

Where:

N is the number of channels active together.

V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as $V_{CE(SAT)}$ (2)

In order to guarantee reliability of ULN2003B and the system the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation ($PD_{(MAX)}$) dictated by below equation 公式 3.

$$PD_{(MAX)} = \left(T_{J(MAX)} - T_A\right) / \theta_{JA}$$

Where:

$T_{J(MAX)}$ is the target maximum junction temperature.

T_A is the operating ambient temperature.

θ_{JA} is the package junction to ambient thermal resistance. (3)

It is recommended to limit ULN2003B IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

10.2.3 Application Curves

The following curves were generated with ULN2003B driving an OMRON G5NB relay – V_{in} = 5.0V; V_{sup}= 12 V & R_{COIL}= 2.8 kΩ

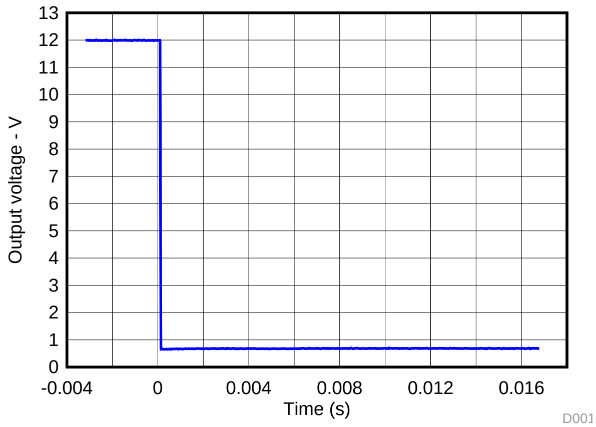


图 17. Output Response With Activation of Coil (Turn On)

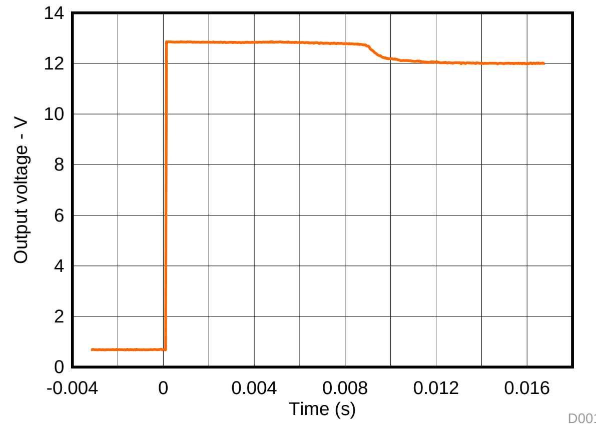


图 18. Output Response With De-activation of Coil (Turn Off)

11 Power Supply Recommendations

This part does not need a power supply; however, the COM pin is typically tied to the system power supply. When this is the case, it is very important to make sure that the output voltage does not heavily exceed the COM pin voltage. This will heavily forward bias the fly-back diodes and cause a large current to flow into COM, potentially damaging the on-chip metal or over-heating the part.

12 Layout

12.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive UNL2003B. Care must be taken to separate the input channels as much as possible, as to eliminate cross-talk. Thick traces are recommended for the output, in order to drive whatever high currents that may be needed. Wire thickness can be determined by the trace material's current density and desired drive current.

Since all of the channels currents return to a common emitter, it is best to size that trace width to be very wide. Some applications require up to 2.5 A.

12.2 Layout Example

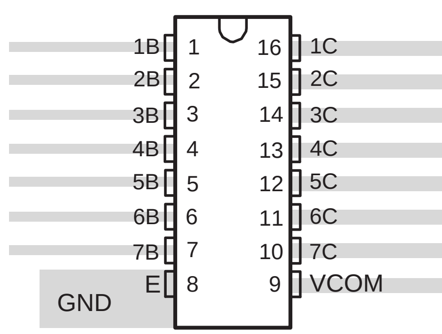


图 19. Package Layout

13 器件和文档支持

13.1 商标

All trademarks are the property of their respective owners.

13.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

14 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ULN2003BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 105	ULN2003B	Samples
ULN2003BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 105	ULN2003BN	Samples
ULN2003BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 105	UN2003B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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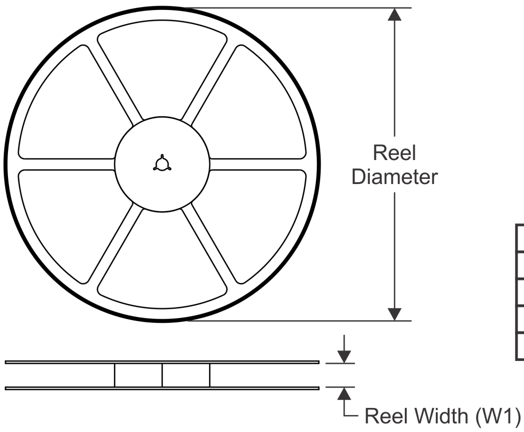
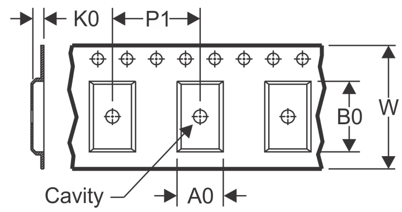
TAPE AND REEL INFORMATION

REEL DIMENSIONS

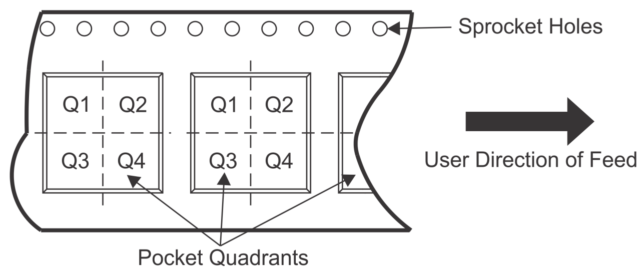


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

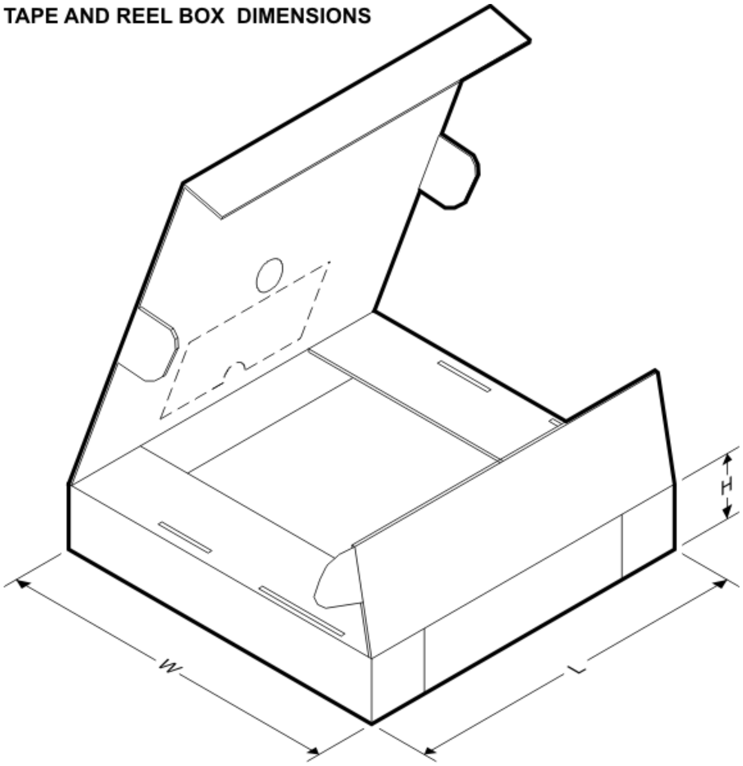
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2003BDR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ULN2003BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

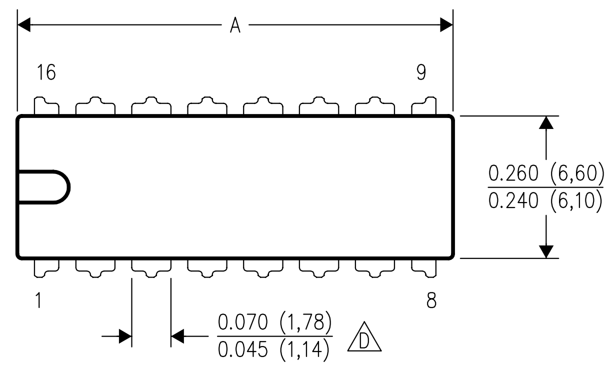


*All dimensions are nominal

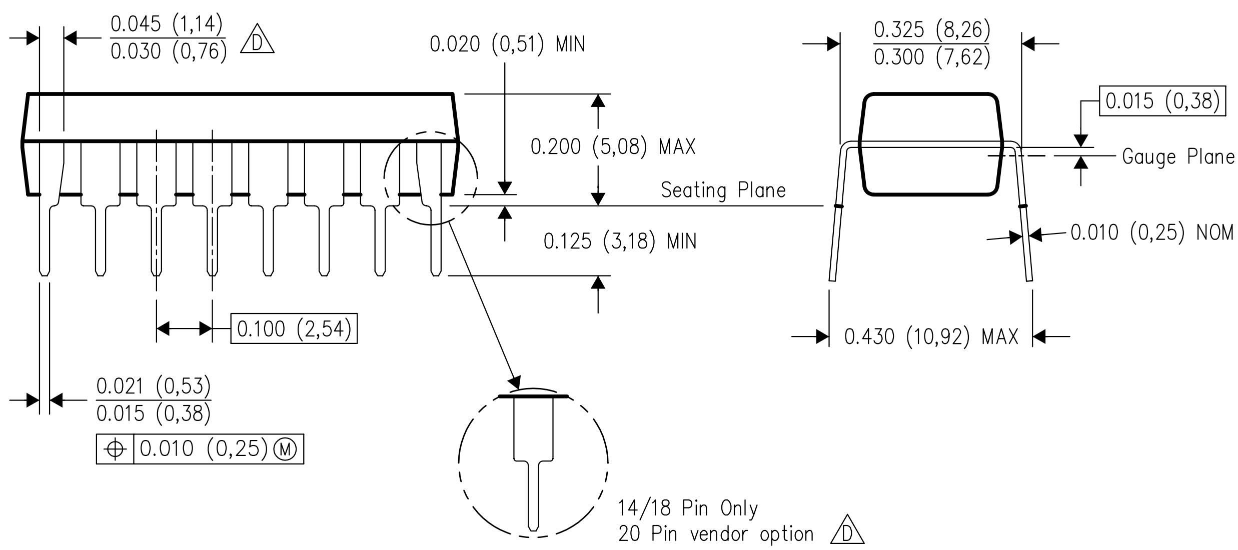
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2003BDR	SOIC	D	16	2500	364.0	364.0	27.0
ULN2003BDR	SOIC	D	16	2500	367.0	367.0	38.0
ULN2003BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
ULN2003BPWR	TSSOP	PW	16	2000	364.0	364.0	27.0

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



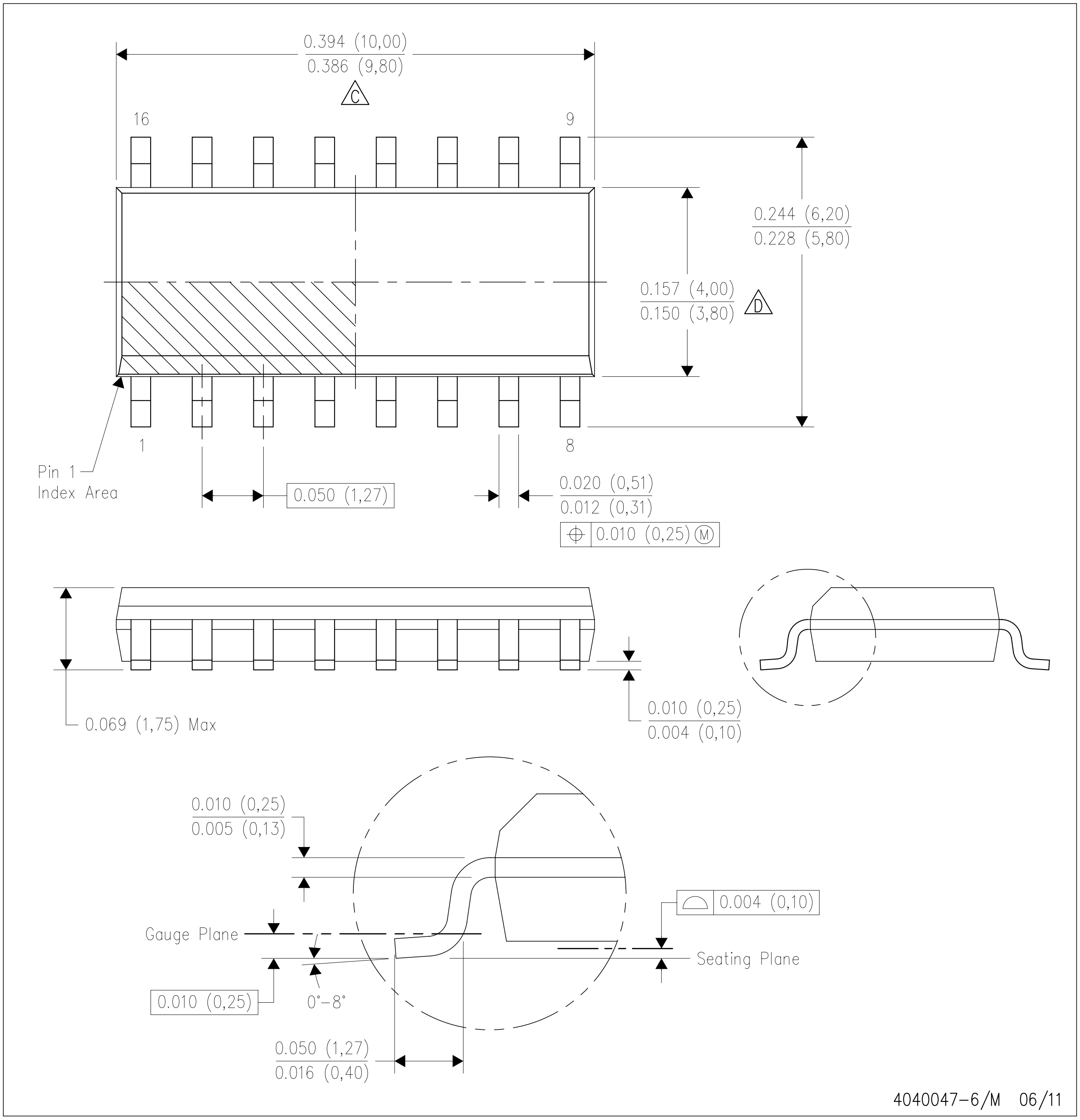
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

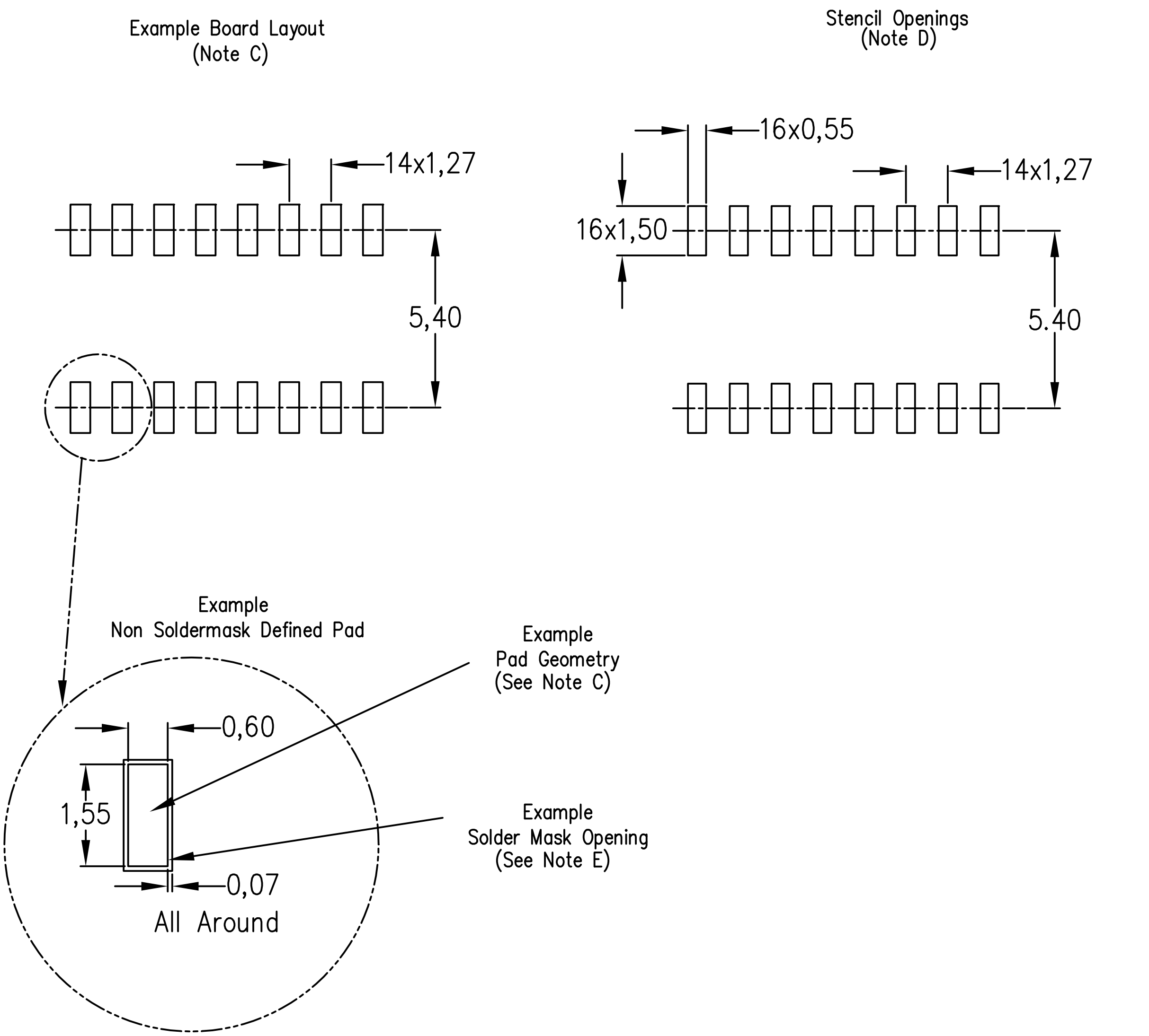
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

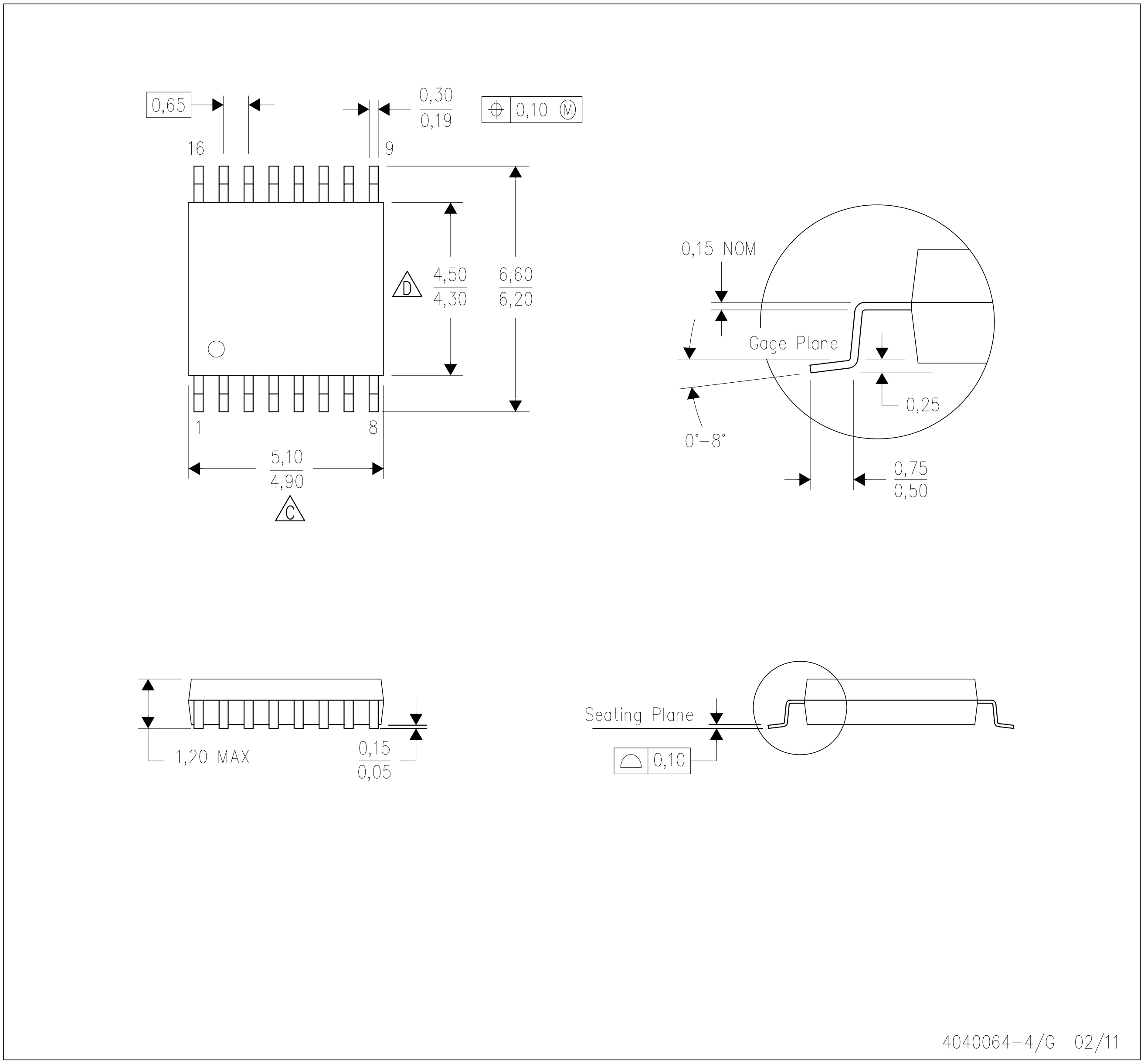
D (R–PDSO–G16) PLASTIC SMALL OUTLINE



4211283–4/E 08/12

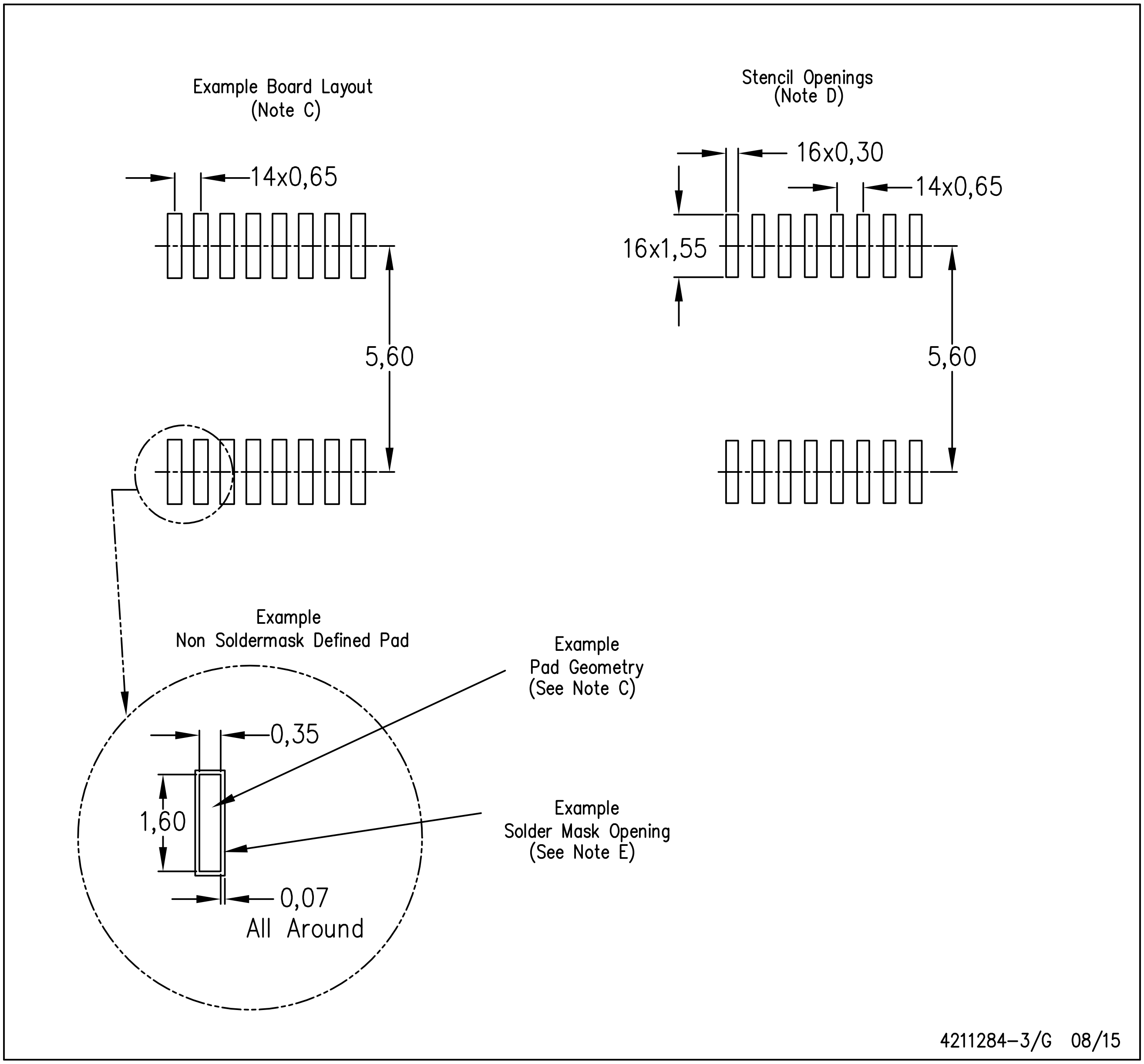
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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