TEXAS INSTRUMENTS

TWL3016

GSM/DCS Baseband and Voice A/D and D/A RF Interface Circuit With Power Supply Management

Data Manual

November 2003

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1 Introduction

This chapter provides an overview of the Texas Instruments TWL3016 device and its features.

1.1 Description

The TWL3016 device is an analog baseband (ABB) device which, together with a digital baseband (DBB) device, is part of a TI TMS320™ DSP (digital signal processor) solution intended for digital cellular telephone applications including the GSM 900, DCS 1800, and PCS 1900 standards (dual-band capability).

The TWL3016 device includes a complete set of baseband functions that perform the interfacing and processing of voice signals, the baseband in-phase (I) and quadrature (Q) signals which support both the single-slot and multislot modes, and MS Class 12 for GMSK modulation types (3GPP TS 05.02). The TWL3016 device also includes associated auxiliary RF control features, supply voltage regulation, battery charging controls, and switch on/off system analysis.

The TWL3016 device interfaces with the DBB device through a digital baseband serial port (BSP) and a voiceband serial port (VSP). The signal ports communicate with a DSP core (LEAD). A microcontroller serial port (USP) communicates with the microcontroller core and a time serial port (TSP) communicates with the time processing unit (TPU) for real-time control.

A specific module is dedicated to support the 1.8-V/3-V SIM card interface. The module includes the generation of the SIM card supply voltage, as well as level shifters to adapt the SIM card signal levels to the microcontroller I/O signal levels. The TWL3016 device meets JTAG testability standard (IEEE Std 1131.1 – 1990) through a standard test access port (TAP) and boundary scan.

The TW3016 device also includes an on-chip voltage reference, under-voltage detection, and power-on reset circuits. The TWL3016 device is packaged in Texas Instruments 143-terminal, 0,5-mm pitch, MicroStarJunior™ ball grid array (GQW).

1.2 Features

The TWL3016 device supports the following features:

- Applications include the GSM 900, PCS 1900, and DSC 1800 cellular telephones
- Baseband coder/decoder (codec) single- and multislot with I/Q RF interface
- Auxiliary RF converters
- Five-channel analog-to-digital converter (ADC)
- Six low-dropout (LDO), linear voltage regulators targeted for core, general I/O, memory I/O, SIM I/O, with low quiescent current mode
- LDO voltage regulators dedicated to the USB interface
- High voltage (20 V) Li-Ion or Ni-MH battery charging control
- Voltage detectors (with power-off delay)
- Dedicated very low quiescent current supply domain
- Voice codec
    - 13.5-bit linear codec
    - Differential input MIC AMP
    - Two single input AUXI/HSMIC AMP

- – Bias amplifier for MIC/HSMIC
- – Differential output earphone driver
- – Differential output speaker driver (8-Ω load)
- – Single output AUXO
- Audio DAC based on I2S format
  - – 16-bit linear DAC
  - – Stereo headphone drivers with pseudoground to eliminate external capacitors (32-Ω load)
  - – Soft volume change/mute features
- 143-terminal MicroStarJunior™ BGA

1.3 Trademarks

MicroStar Junior BGA is a trademark of Texas Instruments.

TMS320 DSP is a trademark of Texas Instruments.

Other trademarks are the property of their respective owners.

1.4 Ordering Information

ORDERING NUMBER	VOLTAGE	T_A
TWL3016B1GQW	-0.3 V to 7 V	$-30°$C to 85$°$C

2 Terminal Descriptions

This section provides the terminal descriptions for the TWL3016 device. Figure 2−1 shows the signal assigned to each terminal in the package. Table 2−1 and Table 2−2 provide a cross-reference between each terminal number and the signal name on that terminal. Table 2−1 is arranged in terminal number order, and Table 2−2 lists the signals in alphabetical order.

**GQW PACKAGE
(BOTTOM VIEW)**
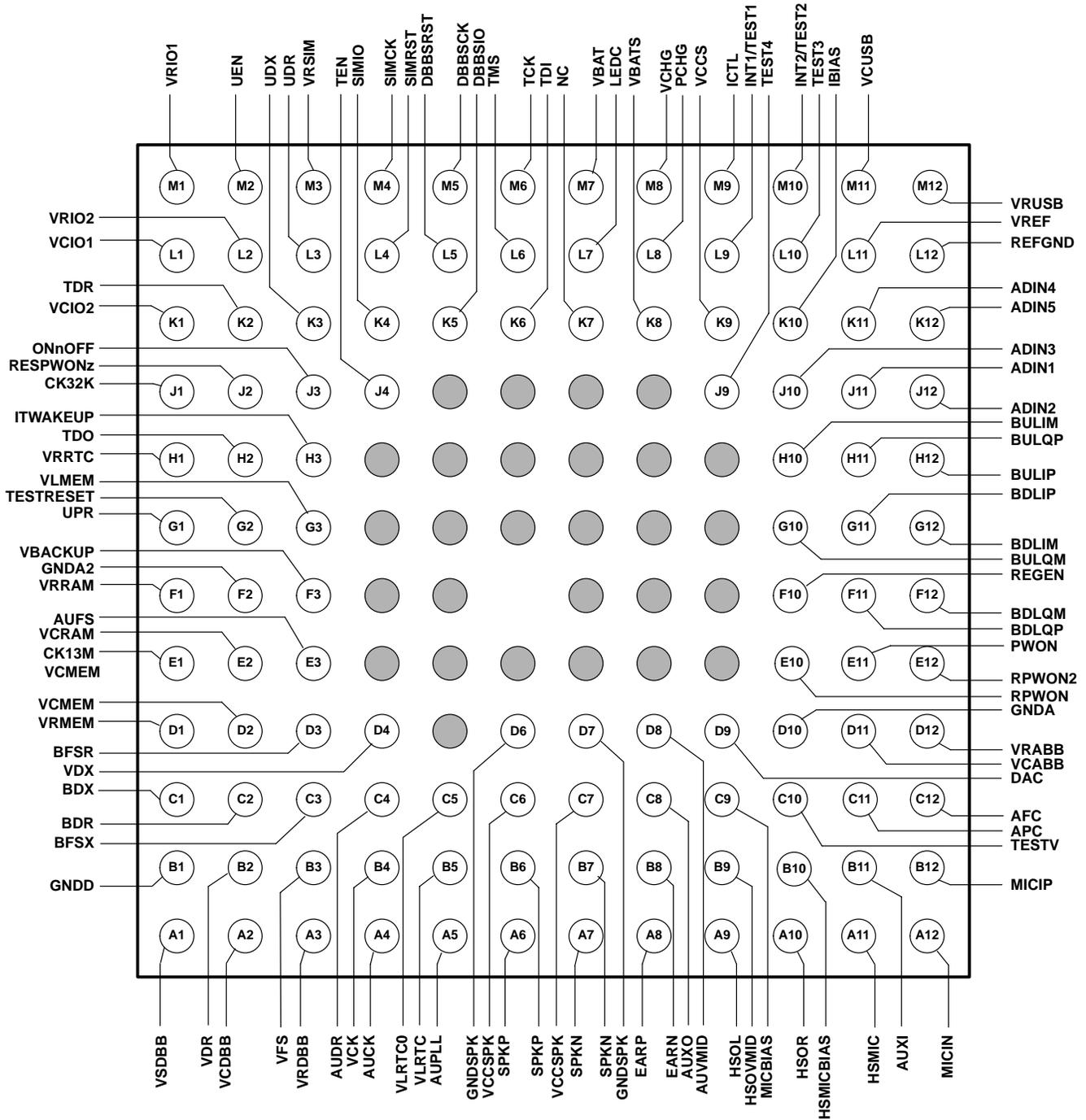
NOTE: All NC terminals are connected to GND during test.

Figure 2–1. TWL3016 GQW Package Terminal Assignments

Table 2–1. Signal Names Sorted by GQW Terminal Number

NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME
A1	VSDBB	D1	VRMEM	G1	UPR	K1	VCIO2
A2	VCDBB	D2	VCMEM	G2	TESTRESET	K2	TDR
A3	VRDBB	D3	BFSR	G3	VLMEM	K3	UDX
A4	AUCK	D4	VDX	G4	GND	K4	SIMIO
A5	AUPLL	D5	GND	G5	GND	K5	DBBSIO
A6	SPKP	D6	GNDSPK	G6	GND	K6	TDI
A7	SPKN	D7	GNDSPK	G7	GND	K7	NC
A8	EARP	D8	AUVMID	G8	GND	K8	VBATS
A9	HSOL	D9	DAC	G9	GND	K9	VCCS
A10	HSOR	D10	GNDA	G10	BULQM	K10	IBIAS
A11	HSMICP	D11	VCABB	G11	BDLIP	K11	ADIN4
A12	MICIN	D12	VRABB	G12	BDLIM	K12	ADIN5
B1	GNDD	E1	CK13M	H1	VRRTC	L1	VCIO1
B2	VDR	E2	VCRAM	H2	TDO	L2	VRIO2
B3	VFS	E3	AUFS	H3	ITWAKEUP	L3	UDR
B4	VCK	E4	GND	H4	GND	L4	SIMRST
B5	VLRTC	E5	GND	H5	GND	L5	DBBSRST
B6	SPKP	E6	GND	H6	GND	L6	TMS
B7	SPKN	E7	GND	H7	GND	L7	LEDC
B8	EARN	E8	GND	H8	GND	L8	PCHG
B9	HSOVMID	E9	GND	H9	GND	L9	INT1/TEST1
B10	HSMICBIAS	E10	RPWON	H10	BULIM	L10	TEST3
B11	AUXI	E11	PWON	H11	BULQP	L11	VREF
B12	MICIP	E12	RPWON2	H12	BULIP	L12	REFGND
C1	BDX	F1	VRRAM	J1	CK32K	M1	VRIO1
C2	BDR	F2	GNDA2	J2	RESPWONz	M2	UEN
C3	BFSX	F3	VBACKUP	J3	ON_nOFF	M3	VRSIM
C4	AUDR	F4	GND	J4	TEN	M4	SIMCK
C5	VLRTC0	F5	GND	J5	GND	M5	DBBSCK
C6	VCCSPK			J6	GND	M6	TCK
C7	VCCSPK	F7	GND	J7	GND	M7	VBAT
C8	AUXO	F8	GND	J8	GND	M8	VCHG
C9	MICBIAS	F9	GND	J9	TEST4	M9	ICTL
C10	TESTV	F10	REGEN	J10	ADIN3	M10	INT2/TEST2
C11	APC	F11	BDLQP	J11	ADIN1	M11	VCUSB
C12	AFC	F12	BDLQM	J12	ADIN2	M12	VRUSB

Table 2–2. Signal Names Sorted Alphanumerically to GQW Terminal Number

SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER
ADIN1	J11	GND	E5	IBIAS	K10	UDX	K3
ADIN2	J12	GND	E6	ICTL	M9	UEN	M2
ADIN3	J10	GND	E7	INT1/TEST1	L9	UPR	G1
ADIN4	K11	GND	E8	INT2/TEST2	M10	VBACKUP	F3
ADIN5	K12	GND	E9	ITWAKEUP	H3	VBAT	M7
AFC	C12	GND	F4	LEDC	L7	VBATS	K8
APC	C11	GND	F5	MICBIAS	C9	VCABB	D11
AUCK	A4	GND	F7	MICIN	A12	VCCS	K9
AUDR	C4	GND	F8	MICIP	B12	VCCSPK	C6
AUFS	E3	GND	F9	NC	K7	VCCSPK	C7
AUPLL	A5	GND	G4	ON_nOFF	J3	VCDBB	A2
AUVMID	D8	GND	G5	PCHG	L8	VCHG	M8
AUXI	B11	GND	G6	PWON	E11	VCIO1	L1
AUXO	C8	GND	G7	REFGND	L12	VCIO2	K1
BDLIM	G12	GND	G8	REGEN	F10	VCK	B4
BDLIP	G11	GND	G9	RESPWONz	J2	VCMEM	D2
BDLQM	F12	GND	H4	RPWON	E10	VCRAM	E2
BDLQP	F11	GND	H5	RPWON2	E12	VCUSB	M11
BDR	C2	GND	H6	SIMCK	M4	VDR	B2
BDX	C1	GND	H7	SIMIO	K4	VDX	D4
BFSR	D3	GND	H8	SIMRST	L4	VFS	B3
BFSX	C3	GND	H9	SPKN	A7	VLMEM	G3
BULIM	H10	GND	J5	SPKN	B7	VLRTC	B5
BULIP	H12	GND	J6	SPKP	A6	VLRTC0	C5
BULQM	G10	GND	J7	SPKP	B6	VRABB	D12
BULQP	H11	GND	J8	TCK	M6	VRDBB	A3
CK13M	E1	GNDA	D10	TDI	K6	VREF	L11
CK32K	J1	GNDA2	F2	TDO	H2	VRIO1	M1
DAC	D9	GNDD	B1	TDR	K2	VRIO2	L2
DBBSCK	M5	GNDSPK	D6	TEN	J4	VRMEM	D1
DBBSIO	K5	GNDSPK	D7	TESTRESET	G2	VRRAM	F1
DBBSRST	L5	HSMICBIAS	B10	TESTV	C10	VRRTC	H1
EARN	B8	HSMICP	A11	TEST3	L10	VRSIM	M3
EARP	A8	HSOL	A9	TEST4	J9	VRUSB	M12
GND	D5	HSOR	A10	TMS	L6	VSDBB	A1
GND	E4	HSOVMID	B9	UDR	L3		

Table 2–3 shows the terminal functions for the TWL3016 device.

Table 2–3. Terminal Functions

TERMINAL		SUPPLIES	I/O	DESCRIPTION	COMMENTS
NAME	NUMBER				
ADIN1	J11	VRABB/GNDA	I/O	Monitoring ADC input 1 and battery type current source	
ADIN2	J12	VRABB/GNDA	I/O	Monitoring ADC input 2 and battery temperature current source	
ADIN3	J10	VRABB/GNDA	I	Monitoring ADC input 3 and battery temperature current source	
ADIN4	K11	VRABB/GNDA	I	Monitoring ADC input 4 (spare)	
ADIN5	K12	VRABB/GNDA	I	Monitoring ADC input 5 (spare)	
AFC	C12	VRABB/GNDA	O	Automatic frequency control DAC output	External capacitor
APC	C11	VRABB/GNDA	O	Automatic power control DAC output	
AUCK	A4	VRIO/GNDD	O	I2S serial port clock	
AUDR	C4	VRIO/GNDD	I	I2S serial port receive data	
AUFS	E3	VRIO/GNDD	O	I2S serial port frame synchronization	
AUPLL	A5	VRABB/GNDA	I/O	Audio PLL filter	External capacitor
AUVMID	D8	VRABB/GNDA	I/O	Audio VMID filter	External capacitor
AUXI	B11	VRABB/REFGND	I	Auxiliary speech signal input	
AUXO	C8	VRABB/GNDA	O	Auxiliary speech signal output	
BDLIM	G12	VRABB/GNDA	I	In-phase input (I–) baseband codec downlink	
BDLIP	G11	VRABB/GNDA	I	In-phase input (I+) baseband codec downlink	
BDLQM	F12	VRABB/GNDA	I	Quadrature input (Q–) baseband codec downlink	
BDLQP	F11	VRABB/GNDA	I	Quadrature input (Q+) baseband codec downlink	
BDR	C2	VRIO/GNDD	I	Baseband serial port receive data	
BDX	C1	VRIO/GNDD	O	Baseband serial port transmit data	
BFSR	D3	VRIO/GNDD	I	Baseband serial port receive frame synchronization	
BFSX	C3	VRIO/GNDD	O	Baseband serial port transmit frame synchronization	
BULIM	H10	VRABB/GNDA	O	In-phase output (I–) baseband codec uplink	
BULIP	H12	VRABB/GNDA	O	In-phase output (I+) baseband codec uplink	
BULQM	G10	VRABB/GNDA	O	Quadrature output (Q–) baseband codec uplink	
BULQP	H11	VRABB/GNDA	O	Quadrature output (Q+) baseband codec uplink	
CK13M	E1	VRIO/GNDD	I	13-MHz master clock input and BSP/TSP/USP clock	
CK32K	J1	VRRTC/GNDD	I	32-kHz clock input	
DAC	D9	VRABB/GNDA	O	Auxiliary 10-bit DAC output	
DBBSCK	M5	VRIO/GNDD	I	SIM card shifters clock input	
DBBSIO	K5	VRIO/GNDD	I/O	SIM card shifters data	External pullup
DBBSRST	L5	VRIO/GNDD	I	SIM card shifters reset input	
EARN	B8	VRABB/GNDA	O	Earphone amplifier output (–)	
EARP	A8	VRABB/GNDA	O	Earphone amplifier output (+)	
GNDA	D10	GNDA	I/O	Power ground return for VRABB	
GNDA2	F2	GNDA2	I/O	Power ground return for VBAT and VCHG	
GNDD	B1	GNDD	I/O	Power ground return for VRIO/UPR	
GNDSPK	D6	GNDSPK	I/O	8-Ω speaker amplifier ground	
GNDSPK	D7	GNDSPK	I/O	8-Ω speaker amplifier ground	
HSMICBIAS	B10	VRABB/REFGND	O	Head set microphone bias supply	

Table 2–3. Terminal Functions (Continued)

TERMINAL		SUPPLIES	I/O	DESCRIPTION	COMMENTS
NAME	NUMBER				
HSMICP	A11	VRABB/REFGND	I	Head set microphone amplifier input	
HSOL	A9	VRABB/REFGND	O	Head set 32-Ω driver (single ended)	
HSOR	A10	VRABB/REFGND	O	Head set 32-Ω driver (single ended)	
HSOVMID	B9	VRABB/REFGND	O	Head set 32-Ω bias supply	
IBIAS	K10	VRABB/REFGND	I/O	Bias current reference resistor (120 kΩ)	External resistor
ICTL	M9	VCHG/GNDA2	O	Charger external transistor control	
INT1/TEST1	L9	VRIO/GNDD	I/O	Fast interrupt/test pad 1 (default is INT1)	
INT2/TEST2	M10	VRIO/GNDD	I/O	Microcontroller interrupt/test pad 2 (default is INT2)	
ITWAKEUP	H3	VRRTC/GNDD	I	Real-time wake-up input	
LEDC	L7	VCHG/GNDA2	I	LED driver: charging device indicator	
MICBIAS	C9	VRABB/REFGND	O	Microphone bias supply	
MICIN	A12	VRABB/REFGND	I	Microphone amplifier input (–)	
MICIP	B12	VRABB/REFGND	I	Microphone amplifier input (+)	
ONnOFF	J3	VRRTC/GNDD	O	Digital baseband reset (at each switch on)	
PCHG	L8	VCHG/GNDA2	O	Battery precharge output current	
PWON	E11	VBAT/GNDD	I	On button input	Pullup
REFGND	L12	REFGND	I/O	Reference voltage ground	
REGEN	F10	VBAT/GNDD	O	External regulator enable	Pulldown
RESPWONz	J2	VRRTC/GNDD	O	Digital baseband power-on reset (first battery plug)	
RPWON	E10	VBAT/GNDD	I	Remote power-on (other than button)	Pullup
RPWON2	E12	VBAT/GNDD	I	Remote power-on 2 (other than button)	Pullup
SIMCK	M4	VRSIM/GNDD	O	SIM card shifters clock output (1.8 V/3 V)	
SIMIO	K4	VRSIM/GNDD	I/O	SIM card shifters data (1.8 V/3 V)	External pullup
SIMRST	L4	VRSIM/GNDD	O	SIM card shifters reset output (1.8 V/3 V)	
SPKN	A7	VCCSPK/GNDSPK	O	8-Ω speaker amplifier output (–)	
SPKN	B7	VCCSPK/GNDSPK	O	8-Ω speaker amplifier output (–)	
SPKP	A6	VCCSPK/GNDSPK	O	8-Ω speaker amplifier output (+)	
SPKP	B6	VCCSPK/GNDSPK	O	8-Ω speaker amplifier output (+)	
TCK	M6	VRIO/GNDD	I	Scan test clock	Pulldown
TDI	K6	VRIO/GNDD	I	Scan path input	Pullup
TDO	H2	VRIO/GNDD	O	Scan path output	3–state
TDR	K2	VRIO/GNDD	I	Time serial port input	
TEN	J4	VRIO/GNDD	I	Time serial port enable	
TESTRESET	G2	UPR/GNDD	I	Reset input for test mode only	Pulldown
TESTV	C10	VBAT/GNDA2	O	Regulator output sense (reserved for test purpose)	
TEST3	L10	VRIO/GNDD	I/O	Special test I/O terminals	Pullup
TEST4	J9	VRIO/GNDD	I/O	Special test I/O terminals	Pullup
TMS	L6	VRIO/GNDD	I	JTAG test mode select	Pullup
UDR	L3	VRIO/GNDD	I	Microcontroller serial port receive data	
UDX	K3	VRIO/GNDD	O	Microcontroller serial port transmit data	3–state
UEN	M2	VRIO/GNDD	I	Microcontroller serial port enable	
UPR	G1	UPR/GNDD	O	Uninterrupted power rail output	External capacitor

Table 2–3. Terminal Functions (Continued)

TERMINAL		SUPPLIES	I/O	DESCRIPTION	COMMENTS
NAME	NUMBER				
VBACKUP	F3	VBACKUP/GNDD	I/O	Backup battery input	External capacitor
VBAT	M7	VBAT/GNDA2	I/O	Battery voltage sense input	External capacitor
VBATS	K8	VCCS/GNDA2	I	Battery voltage sense	
VCABB	D11	VCABB/GNDA2	I/O	Input of regulator VRABB	
VCCS	K9	VCCS/GNDA2	I	Charging current sense	
VCCSPK	C6	VCCSPK/GNDSPK	I/O	8-Ω speaker amplifier supply	
VCCSPK	C7	VCCSPK/GNDSPK	I/O	8-Ω speaker amplifier supply	
VCDBB	A2	VCDBB/GNDD	I/O	Input of regulator VRDBB	
VCHG	M8	VCHG/GNDA2	I/O	Charger voltage input	External capacitor
VCIO1	L1	VCIO/GNDD	I/O	Input 1 of regulator VRIO and VRSIM	
VCIO2	K1	VCIO/GNDD	I/O	Input 2 of regulator VRIO and VRSIM	
VCK	B4	VRIO/GNDD	O	Voiceband serial port clock	
VCMEM	D2	VCMEM/GNDD	I/O	Input of regulator VRMEM	
VCRAM	E2	VCRAM/GNDD	I/O	Input of regulator VRRAM	
VCUSB	M11	VCUSB/GNDD	I/O	Input of regulator VRUSB	
VDR	B2	VRIO/GNDD	I	Voiceband serial port receive data	
VDX	D4	VRIO/GNDD	O	Voiceband serial port transmit data	
VFS	B3	VRIO/GNDD	O	Voiceband serial port frame synchronization	
VLMEM	G3	UPR/GNDD	I	Select output voltage of VRMEM	
VLRTC	B5	UPR/GNDD	I	Select output voltage of VRRTC and VRDBB	
VLRTC0	C5	UPR/GNDD	I	Select output voltage of VRRTC and VRDBB	
VRABB	D12	VRABB/GNDA	O	Regulator VRABB output	External capacitor
VRDBB	A3	VRDBB/GNDD	O	Regulator VRDBB output	External capacitor
VREF	L11	VRABB/REFGND	I/O	Reference voltage (1.18 V)	External capacitor
VRIO1	M1	VRIO/GNDD	O	Regulator VRIO output 1	External capacitor
VRIO2	L2	VRIO/GNDD	O	Regulator VRIO output 2	External capacitor
VRMEM	D1	VRMEM/GNDD	O	Regulator VRMEM output	External capacitor
VRRAM	F1	VRRAM/GNDD	O	Regulator VRRAMoutput	External capacitor
VRRTC	H1	VRRTC/GNDD	O	Regulator VRRTC output	External capacitor
VRSIM	M3	VRSIM/GNDD	O	Regulator VRSIM output	External capacitor
VRUSB	M12	VRUSB/GNDD	O	Regulator VRUSB output	External capacitor
VSDBB	A1	VRDBB/GNDD	I	Regulator VRDBB input feedback	

3 Functional Description

This section describes the functional blocks that comprise the TWL3016 device. Figure 3–1 is a block diagram of the device.
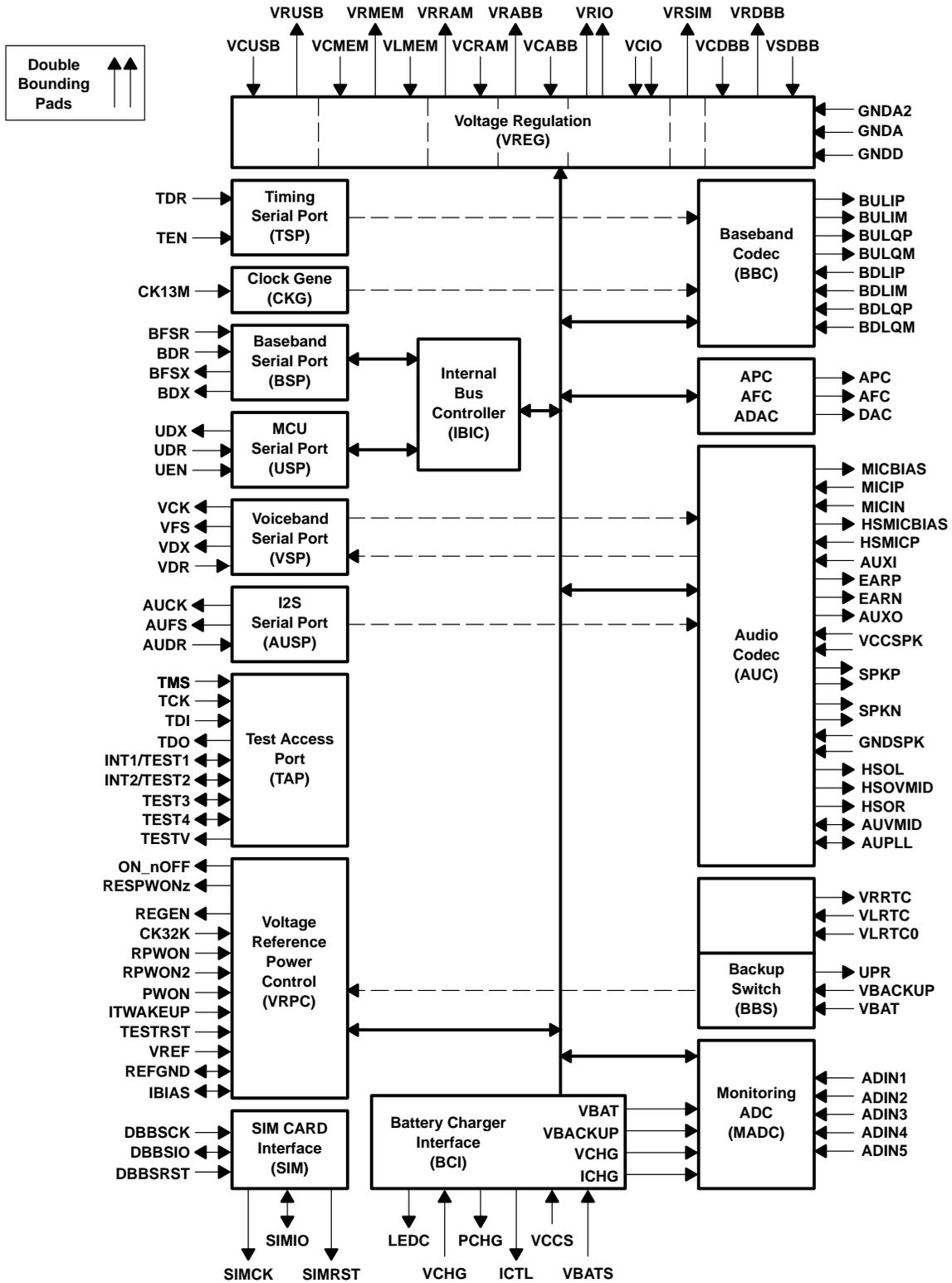
Figure 3–1. TWL3016 Functional Block Diagram

3.1   Audio Codec

The audio codec (AUC) consists of a voice coder-decoder (codec) dedicated to GSM applications and an audio stereo line. The voice codec circuit processes analog audio components in the uplink path and transmits this signal to the DSP speech coder through the voice serial port (VSP). In the downlink path, the codec converts the digital samples of speech data received from the DSP via the VSP port into analog audio signals. The voice codec supports an 8-kHz (default) or a 16-kHz sampling frequency. The stereo audio path converts audio component data received from the I2S serial interface (AUSP) into analog audio.

The AUC includes input amplifiers for microphones (headset, phone, auxiliary) and output amplifiers (stereo/mono headset, phone speaker, 8-Ω speaker, auxiliary).

The AUC also performs the programmable gain, volume control, and side-tone functions for the uplink and downlink path of the voice codec. A common programmable gain and two independent volume controls are available for the right and left channels of the stereo path.

3.2   Baseband Codec

The baseband codec (BBC) is composed of a baseband uplink (BUL) path and a baseband downlink (BDL) path.

The BUL path modulates the data bursts coming from the DSP via the baseband serial port (BSP). Modulation is performed by a Gaussian minimum shift keying (GMSK) modulator, according to GSM specification 5.04. The GMSK modulator, which is implemented digitally, generates the in-phase (I) and quadrature (Q) components. These components are converted into analog baseband by two 10-bit DACs and filtered by third-order low-pass filters. The BUL path includes secondary functions such as dc offset calibration and I/Q gain unbalance.

The BDL path converts the baseband analog I and Q components from the RF receiver into digital samples. The resulting signals are filtered through a digital FIR to isolate the desired data from the adjacent channels. During reception of the burst I and Q components, the digital data are sent to the DSP via the BSP at a rate of 270.833 kHz. The BDL path includes a dc offset calibration.

Timing windows of the BUL and BDL paths are controlled through the time serial port (TSP) by the TPU of the digital baseband (DBB) device.

Implementation of the BBC allows multislot and full-duplex operation.

3.3   Low-Dropout Linear Voltage Regulator

Several low-dropout (LDO) regulators perform linear voltage regulation. These regulators, connected to the main battery, supply power to:

- Internal analog blocks
- Internal digital blocks and the DBB I/Os
- The DBB core
- External memories
- SIM card and SIM card drivers

All these regulators allow a low current consumption working mode, SLEEP mode, but with a reduced current capability.

A regulator supplies USB I/Os, with an input voltage derived from an USB connector.

The last LDO (VRRTC) is a programmable regulator that generates the supply voltages for the real time clock (32 kHz) of the DBB processor and dedicated I/Os. The main or backup battery supplies VRTC, using the uninterrupted power rail (UPR). This LDO has an ultralow current consumption.

3.4 Backup Battery Switch

The backup battery switch (BBS) generates at its output an uninterrupted power rail (UPR) to supply the minimum necessary circuitry of the power-control functions continuously, either from the main battery or from the backup battery. This UPR is connected to the UPR output terminal for decoupling purposes. No external load is allowed on UPR.

3.5 SIM Card Shifters (SIMS)

To allow the use of both 1.8-V and 3-V SIM card types, a SIM level-shifter module in the TWL3016 device interfaces the SIM signals (DBBSRST, DBBSIO, and DBBSCK) at a constant VRIO level from the DBB device with the SIM card (SIMRST, SIMIO, and SIMCK) at a 1.8-V or 3-V level depending on SIM type.

3.6 Monitoring ADC

The monitoring ADC (MADC) consists of a 10-bit analog-to-digital converter (ADC) combined with an 9-input analog multiplexer. Five of the nine inputs are available externally, and the remaining four inputs are dedicated to main battery voltage, backup battery voltage, charger voltage, and charger current monitoring. Of the five available external inputs, three are standard inputs, and the two that are associated with current sources are intended for battery temperature and battery type measurements.

Conversion requests, input/output channels, and results reading can be performed either through the BSP, through the USP, or through the TSP interface.

3.7 Voltage Reference/Power-On Control

The external resistor connected between the IBIAS and REFGND terminals sets the value of the bias currents of the analog functions from the band-gap voltage.

The voltage reference/power-on control (VRPC) block controls the power on, power off, switch on, and switch off sequences.

Some block functions are performed even in the off state. These permanent functions ensure the wake-up of the device, such as, ON/OFF button detection or charger detection.

Interrupt INT2 is generated either for the following events: PWON, RPWRON, RPWON2, a charger plug/unplug is detected, or an USB plug/unplug is detected while the device is in power on. Interrupt INT1 is generated when abnormal low battery voltage condition is detected. See Section 4.6.7, *Interrupt Handling*.

3.8 Baseband Serial Port

The baseband serial port (BSP) is a bidirectional (transmit/receive) serial port. Both receive and transmit operations are double-buffered and permit a continuous communication stream. Format is a 16-bit data packet with transmit and receive frame synchronization signals. In the receive mode, the data (BDR) and the frame synchronization signal (BFSR) are given by the DBB device. In the transmit mode, the data (BDX) and the frame synchronization signal (BFSX) are given by the TWL3016 device. The CK13M master clock is used as a clock for both transmit and receive modes.

The BSP allows read and write access of all internal registers under the arbitration of the internal bus controller. But its transmit path is allocated to the BDL path during burst reception for I and Q data transmissions.

3.9 Time Serial Port

The time serial port (TSP) controls in real time the radio activation windows of the TWL3016 device: BUL power-on, BUL calibration, BUL transmit, BDL power-on, BDL calibration, BDL receive, and the ADC conversion start.

These real-time control signals are processed by the TPU of the DBB device and transmitted serially to the TWL3016 device via the TSP, which consists of a very simple two-terminal serial port. The TEN terminal is an enable, the TDR terminal is the data receive. The CK13M master clock divided by two is used internally as the clock for this serial port.

3.10 Microcontroller Serial Port

The microcontroller serial port (USP) is a bidirectional (transmit/receive) synchronous serial port. It consists of three terminals: data transmit (UDX), data receive (UDR), and port enable (UEN). The clock signal is the CK13M master clock. Transfers are initiated by the external microcontroller, which pushes data into the USP via the UDR, while synchronous data contained in the transmit buffer of the USP is pushed out via the UDX. A minimum of eight rising edges of the CK13M or CK32K clocks (depending on the status of bit 6 (ACTIVMCLK) in the power down register) separate two consecutive USP accesses.

The USP allows read and write access of all internal registers under the arbitration of the internal bus controller.

3.11 Voiceband Serial Port

The voice serial port (VSP) is a bidirectional (transmit/receive) configurable serial port. It consists of four terminals: data transmit (VDX), data receive (VDR), the frame synchronization signal (VFS), and the clock signal (VCK). Both receive and transmit operations are double-buffered and permit a continuous communication stream. Format is a 16-bit data packet with frame synchronization. The serial interface may be configured for the following two operating modes:

- 8-kHz frame synchronization signal (default mode) and 500-kHz (default)/1-MHz programmable master clock signal

- 16-kHz frame synchronization signal and 500-kHz (default)/2-MHz programmable master clock signal

3.12 Stereo Audio (I2S) Serial Port

The audio serial port (AUSP) is a synchronous serial port. It consists of three terminals: data receive (AUDR), the left/right frame synchronization signal (AUFS), and the clock signal (AUCK). Format is a 2*20-bit data packet with a programmable sampling frequency (F_S = [8–48k] Hz). The TWL3016 device delivers a 40*F_S master data clock. The stereo audio interface allows the I2S reception mode.

3.13 Automatic Frequency Control

The automatic frequency control (AFC) function consists of a digital-to-analog converter (DAC) optimized for high-resolution dc conversion. The AFC controls the frequency of the GSM 13-MHz oscillator to maintain mobile synchronization on the base station and to allow proper transmission and demodulation.

3.14 Automatic Power Control

The automatic power control (APC) generates an envelope signal to control the power ramp up, power ramp down, and power level of the radio burst. The APC structure is intended to support single-slot and multislot transmissions with smooth power transitions when consecutive bursts are transmitted at different power levels.

The APC includes a DAC and a RAM, in which the shape of the edges (ramp up and ramp down) of the envelope signals are stored digitally. This envelope signal is converted to an analog signal by a 10-bit DAC.

Timing of the APC is generated internally and depends on the real-time signals coming from the TSP and the contents of two registers that control the relative position of the envelope signal versus the modulated I and Q components.

3.15 Auxiliary DAC

The auxiliary DAC (ADAC) is a general-purpose 10-bit DAC.

3.16 High Voltage (20 V) Battery Charger Interface

The TWL3016 battery charger interface (BCI) controls the charging of either a 1-cell Li-Ion battery or a 3-series Ni-MH/Ni-Cd cell battery with the support of the microcontroller (the DBB device).

The battery is monitored using the 10-bit ADC converter from the MADC to measure the battery voltage, battery temperature, battery type, battery charge current, and battery charger input voltage.

The magnitude of the charging current is set by 8 bits of a programming register converted by the 8-bit DAC, whose output sets the reference input of the charging current control loop. The magnitude of the charging voltage is set by 10 bits of a programming register converted by a 10-bit DAC, whose output sets the reference input of the charging voltage control loop.

The BCI also performs some auxiliary functions. These functions are battery precharge, battery over-temperature detection, battery over-voltage detection, battery end-of-charge current detection, and back-up.

An external LED may be driven depending of the charger status. When the TWL3016 device is in off or sleep mode, the LED control follows the precharge state. When the TWL3016 device is in active mode, the LED is controlled through bit 5 (LEDC) in the battery control 2 register (see Section 5.3.7.4).

The BCI is under register control. These registers can be programmed either through the BSP or through the USP.

4 Detailed Description

4.1 Audio Codec

The audio codec consists of a voice codec dedicated to the GSM application and an audio stereo line. The voice codec circuitry processes analog audio components in the voice uplink (VUL) path and applies this signal to the voice signal interface for eventual baseband modulation. In the voice downlink (VDL) path, the codec circuitry changes voice component data received from the voice serial interface (VSP) into analog audio. The voice codec supports an 8-/16-kHz sampling frequency. The stereo audio path converts audio component data received from the I2S serial interface into analog audio. The following paragraphs describe these uplink/downlink and audio stereo functions in more detail.

Figure 4–1. Audio Codec Block Diagram

Table 4–1 shows the available signals on the audio codec outputs, depending on the programmed configuration.

Table 4–1. Audio Codec Output Signals

SERIAL INTERFACE	EARAMP	AUXAMP	SPKAMP	HSOAMPL	HSOAMPR
VSP	Voice speech	Voice speech	Voice speech	Voice speech	Voice speech
I2S	Audio mono	Audio mono	Audio mono	Audio mono	Audio mono
VSP + I2S	Voice speech + Audio mono	Voice speech + Audio mono	Voice speech + Audio mono	Voice speech + Audio stereo left / Audio mono	Voice speech + Audio stereo right / Audio mono

4.1.1 Voice Uplink Path

The VUL path includes two input stages. The first stage is a microphone amplifier, compatible with electret microphones containing an FET buffer with open drain output. The microphone amplifier has a gain of typically 25.6 dB and a bias generator provides an external voltage of 2.0 V to 2.5 V to bias the microphone (MICBIAS terminal). The auxiliary audio input can be used as an alternative source for higher level of speech signals. This stage performs single-ended-to-differential conversion and provides a programmable gain of 4.6 dB or 28.2 dB. The input of the auxiliary audio stage and the microphone biasing voltage can also be available on the headset microphone terminals (HSMIC and HSMICBIAS). When the auxiliary audio input is used, the microphone input is disabled and powered down. The auxiliary audio input and the headset microphone gain stage can't be active at the same time. The auxiliary audio input and the headset microphone input can be used as differential inputs of the microphone amplifier, the microphone input terminals are then set to a high impedance state and a biasing voltage can be available on the HSMICBIAS or MICBIAS terminal.

The resulting fully differential signal is fed to the analog-to-digital converter (ADC) which is determined by the value of the internal voltage reference.

The analog-to-digital conversion is performed by a third-order Σ-Δ modulator with a sampling rate of 1 MHz/2 MHz. Output of the ADC is fed to a speech digital filter, which performs the decimation down to 8 kHz/16 kHz and band-limits the signal with both low-pass and high-pass transfer functions. Programmable gain can be set digitally from –12 dB to +12 dB in 1-dB steps and is programmed with bits 4–0 (VULPG(4:0)) of the voiceband uplink register (see Section 5.3.10.4). The speech samples are then transmitted to the DSP via the VSP at a rate of 8 kHz/16 kHz. Programmable functions of the VUL path, power-up, input selection, and gain are controlled using the BSP or the USP serial interfaces. The VUL path can be powered down using bit 0 (VULON) of the power down register (see Section 5.3.3.3).
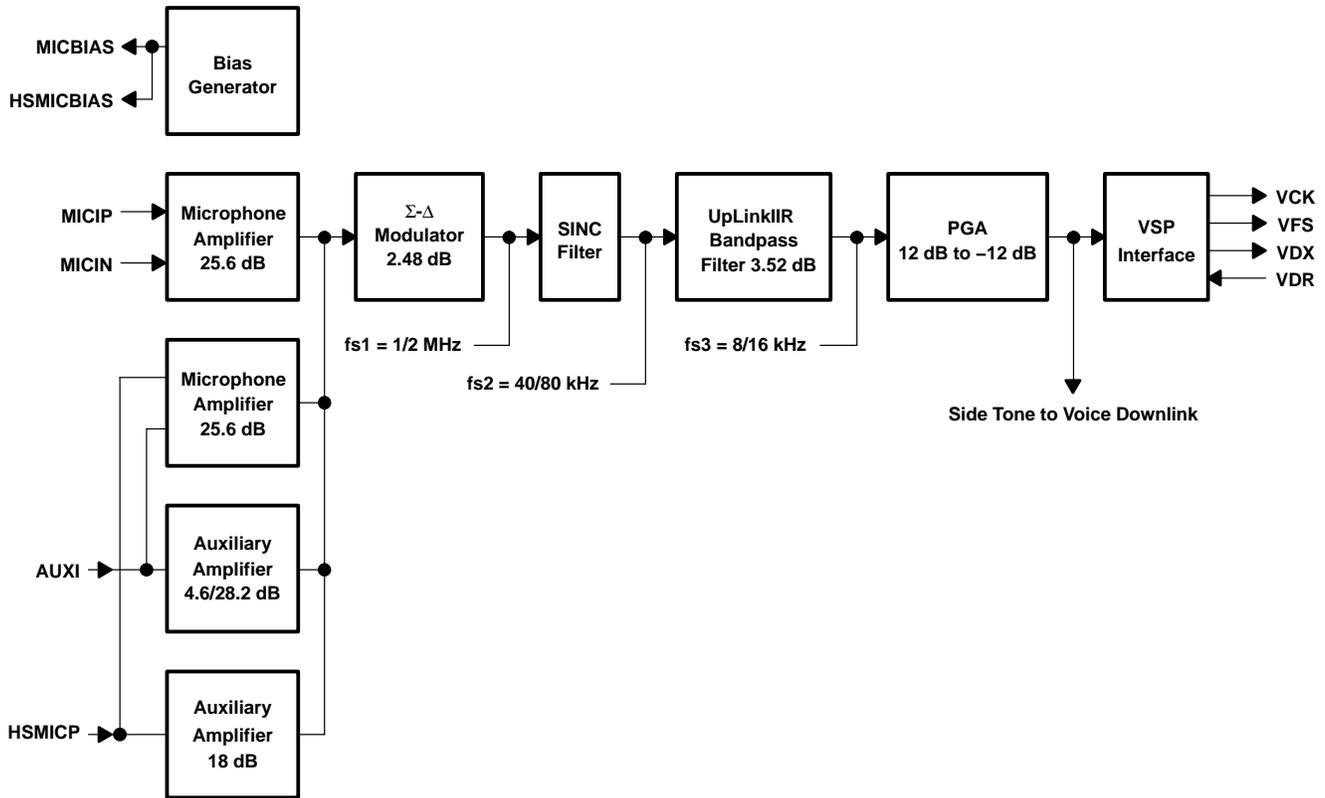
Figure 4–2. Voice Uplink Path

4.1.2 Voice Downlink Path

The VDL path receives speech samples at the rate of 8 kHz/16 kHz from the DSP via the VSP and converts them to analog signals to drive the external speech transducer.

The digital speech coming from the DSP is first fed to a speech digital filter that has two functions. The first function interpolates the input signal and increases the sampling rate from 8 kHz/16 kHz up to 40 kHz/80 kHz to allow the digital-to-analog conversion to be performed by an over-sampling digital modulator. The second function band-limits the speech signal with both low-pass and high-pass transfer functions. The filter and PGA gain can be bypassed by programming bit 9 (VFBYP) in the voiceband control register 1 (see Section 5.3.10.1). The highpass of the speech downlink filter can be bypassed using bit 3 (HPFBYP) of the audio control register (see Section 5.3.10.6).

The interpolated and band-limited signal is fed into a second order Σ-Δ digital modulator sampled at 1 MHz or 2 MHz to generate a 4-bit (9-level) over-sampled signal. This signal is then passed through a dynamic element matching block and then to a 4-bit digital-to-analog converter (DAC).

Due to the over-sampling conversion, the analog signal obtained at the output of the 4-bit DAC is mixed with a high frequency noise. Because a 4-bit digital output is used, a first-order RC filter (included in the output stage) is enough to filter this noise.

The volume control and the programmable gain are performed in the TX digital filter. Volume control is performed in steps of 6 dB from 0 dB to –24 dB. In the mute state, attenuation is higher than 40 dB. A fine adjustment of gain is possible from –6 dB to +6 dB in 1-dB steps to calibrate the system depending on the earphone characteristics. This configuration is programmed with the voiceband control register.

The earphone amplifier provides a full differential signal on the terminals EARP and EARN, and an auxiliary output amplifier provides a single signal on terminals AUXO. The 8-Ω speaker amplifier provides a differential signal on the SPKP and SPKN terminals. The VDL path can be powered down by bit 1 (VDLON) of the power down register (see Section 5.3.3.3).
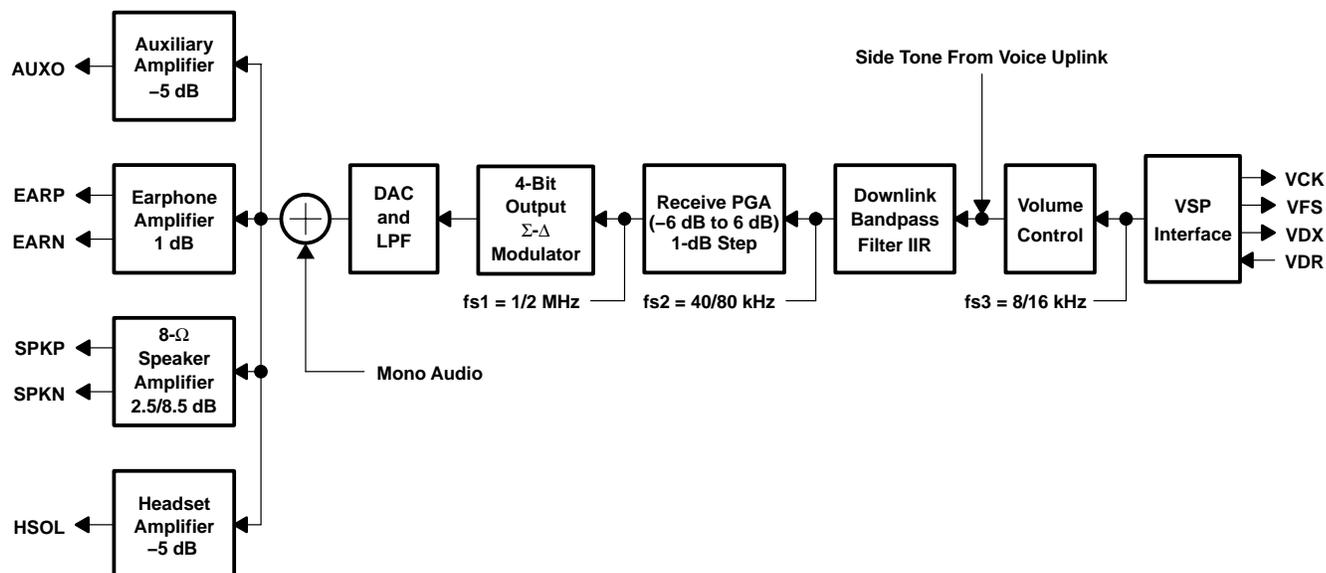
Figure 4–3. Voice Codec Downlink Path

4.1.3 Stereo Audio Path

The stereo audio path receives left and right signal samples at the rate of a programmable frequency, from 8 kHz to 48 kHz, via the I2S serial interface and converts them to analog signals to drive the external audio signal or speech transducers.

The digital audio signal is first fed to an audio digital filter that has two functions. The first function interpolates the input signal and increases the sampling rate to allow the digital-to-analog conversion to be performed by an over-sampling digital modulator. The second function band-limits the audio signal with a low-pass transfer functions. The interpolated and band-limited signal is fed to a second order Σ-Δ digital modulator sampled at f_{S1} frequency to generate a 4-bit (9-level) over-sampled signal. This signal is then passed through a dynamic element matching block and then to a 4-bit DAC.

Due to the over-sampling conversion, the analog signal obtained at the output of the 4-bit DAC is mixed with a high frequency noise. Because a 4-bit digital output is used, a first-order RC filter (included in the output stage) is enough to filter this noise.

The volume control is performed in the audio digital filter. Volume control is performed in steps of 1 dB from 0 dB to –30 dB. In mute state, attenuation is higher than 40 dB. The gain is independently programmable on the left and right channels, using the same audio stereo path control register (see Section 5.3.10.8). A common adjustment of gain is possible at 0 dB or +6 dB. A digital left/right adder and a –6 dB attenuator allows output of a mono audio path. These configurations are programmed with the audio control register (see Section 5.3.10.6).

The left and right headset amplifiers provide the stereo signal on the HSOL and HSOR terminals. A pseudoground is provided on the HSOVMID terminal to eliminate external capacitors. The mono audio signal can be provided on the right or the right and left headset outputs. The mono audio signal can be added to the speech signal and provided on the auxiliary, earphone and/or 8-Ω speaker outputs. The audio stereo/mono path can be powered down and configured with the power down, audio control, and audio PLL registers (see Sections 5.3.3.3, 5.3.10.6, and 5.3.10.9, respectively)
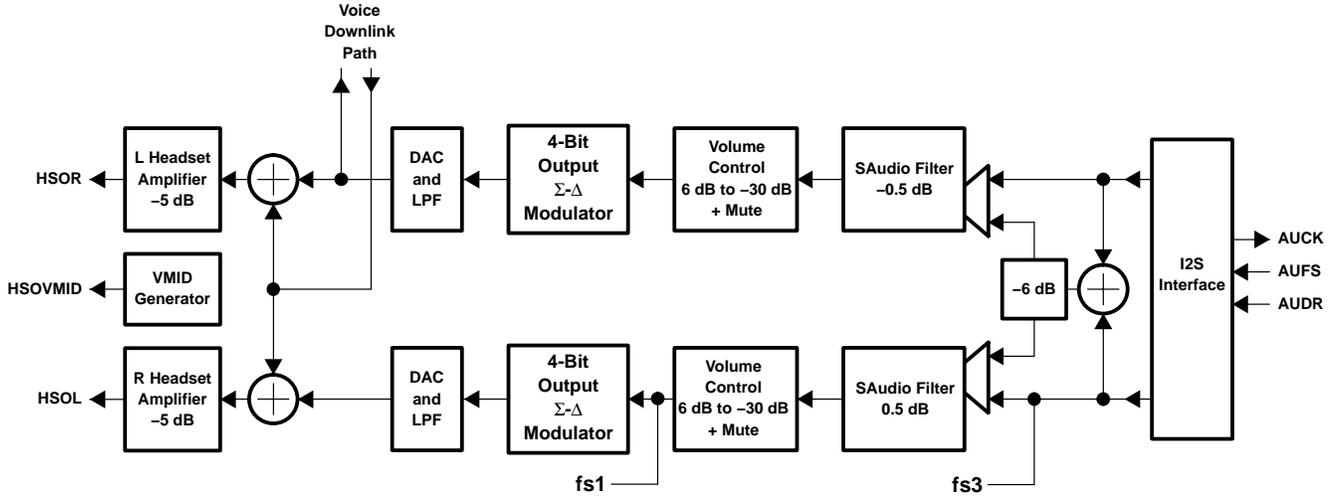
Figure 4–4. Stereo Audio Path

Table 4–2. Tel PLL

MASTER MODE TEL 16 kHz PLL FREQUENCY PLAN: CLKIN = 13 MHz										
VCO = (Nf/Nr) * CLKIN FS1 = (1/Nm) VCO FS2 = (1/Nd)*FS1 VCK = (1/Nb)*FS1 FS3 = VFS = (1/Nfs)*FS1										
Nr	Nf	VCO	Nm	FS1	Nd	FS2	Nb	VCK	Nfs	VFS
1	2	26 MHz	13	2 MHz	25	80 kHz	2	1 MHz	125	16 kHz

Table 4–3. Stereo Audio PLL

MASTER MODE AUDIO PLL FREQUENCY PLAN: CLKIN = 13 MHz						
VCO = (NF/NR)*CLKIN FS1 = (1/NM)*VCO AUCK = FS1/2 AUFS = AUCK/40						
Nr	Nf	VCO	Nm	FS1	AUCK	AUFS
2210	2176	12.8 MHz	20	640 kHz	320 kHz	8 kHz
1625	2205	17.64 MHz	20	882 kHz	441 kHz	11.025 kHz
2210	2176	12.8 MHz	10	1.28 MHz	640 kHz	16 kHz
1625	2205	17.64 MHz	10	1.764 MHz	882 kHz	22.05 kHz
2210	2176	12.8 MHz	5	2.56 MHz	1.280 MHz	32 kHz
1625	2205	17.64 MHz	5	3.528 MHz	1.764 MHz	44.1 kHz
1625	2400	19.2 MHz	5	3.84 MHz	1.92 MHz	48 kHz

4.2   Baseband Uplink and Downlink Path

The baseband codec includes a two-channel (I and Q) baseband uplink (BUL) path and a two-channel (I and Q) baseband downlink (BDL) path.

4.2.1   Baseband Uplink Path

The BUL path performs modulation of burst data sent from the DSP radio interface (RIF) to the baseband serial port (BSP). The modulator circuit in the BUL path performs the Gaussian minimum shift keying (GMSK) in accordance with the 3GPP specification TS 05.04.

The GMSK modulator is implemented digitally, the Gaussian filter computed on 3 bits of the input data stream being encoded in Sin/Cos look-up table in ROM, and it generates the in-phase (I) and quadrature (Q) digital samples with an interpolation ratio of 16.

The raw burst data (as yet unmodulated) received via the BSP is loaded in a burst RAM prior to performing the modulation. Burst RAM and multi-slot operation are described in a paragraph below.

The GMSK modulator has a bit-rate of 270.833 kHz, the same rate as its symbol rate. The resulting bit stream is Gaussian filtered, and then the I and Q digital samples are generated with an interpolation ratio of 16 from the symbol rate, that is, at 4.33 MHz.

These digital I and Q words are sampled at 4.33 MHz and applied to the inputs of a pair of 10-bit DACs. The analog outputs are then passed through third-order Bessel filters to reduce out-of-band noise and image frequency and to obtain a modulated output spectrum consistent with 3GPP specification TS 05.05.

Fully differential signals are available at terminals BULIP, BULIM, BULQP, and BULQM.

To minimize phase trajectory error, the dc offset of the I and Q channels can be minimized using offset calibration capability. During offset calibration, input words of the 10-bit DACs are set to zero code and a 6-bit sub-DAC is used to minimize the dc offset at analog outputs.

The entire content of a burst, including guard bits, tail bits, and data bits, is stored in one of two burst buffers before starting the transmission. The presence of two burst buffers is dictated by the need to support multi-slot transmission: one buffer is loaded with new data while the content of the second buffer is pushed into the GMSK modulator for transmission.

Single slot or multi-slot mode is selected using bit 5 (MSLOT) of the baseband codec control register (see Section 5.3.9.8). When single slot mode is selected, only the content of burst buffer 1 is used for modulation. Output level can be selected with bits 8–6 (OUTLEV(2:0)) of the baseband codec control register.

The typical sequence of a burst transmission consists of:

1. Powering up the BUL path

2. Performing an offset calibration

3. Modulating the content of the burst buffer

Timing of this sequence is controlled via the TSP, which receives the serial real-time control signal from the TPU of the digital baseband (DBB) device. Three real-time signals control the transmission of a burst BULON, BULCAL, and BULENA; each signal corresponds to a time window.

BULON high sets the BUL path in power-on mode after a delay corresponding to the power-on settling time of the analog block. BULCAL enables the offset calibration window. During BULCAL, inputs of 10-bit DACs are forced to code zero and a low-offset comparator senses the dc level at the BULIP/BULIM and BULQP/BULQM outputs, and the result of the comparison modifies the content of the offset registers, which drives the 6-bit sub-DACs to minimize the offset error. The duration of the calibration phase depends on the time needed to sweep the sub-DAC dynamic range. Modulation starts with the rising edge of BULENA and ends 32 one-quarter bits after the falling edge of BULENA. At the end of modulation, the modulator is reinitialized by setting the pointers of burst buffers and the filter ROM to the base address. The I vector is set to its maximum value, while the Q vector is set to 0.

A capability exists to unbalance the gain between I and Q channels in order to allow compensation of natural gain mismatch or imperfection of RF mixer via the baseband uplink absolute gain calibration register (see Section 5.3.9.5).

The output common mode voltage of BULIP, BULIM, BULQP, and BULQM can be set to several values with bits 2–0 (SELVMID(2:0)) of the baseband codec control register (see Section 5.3.9.8).
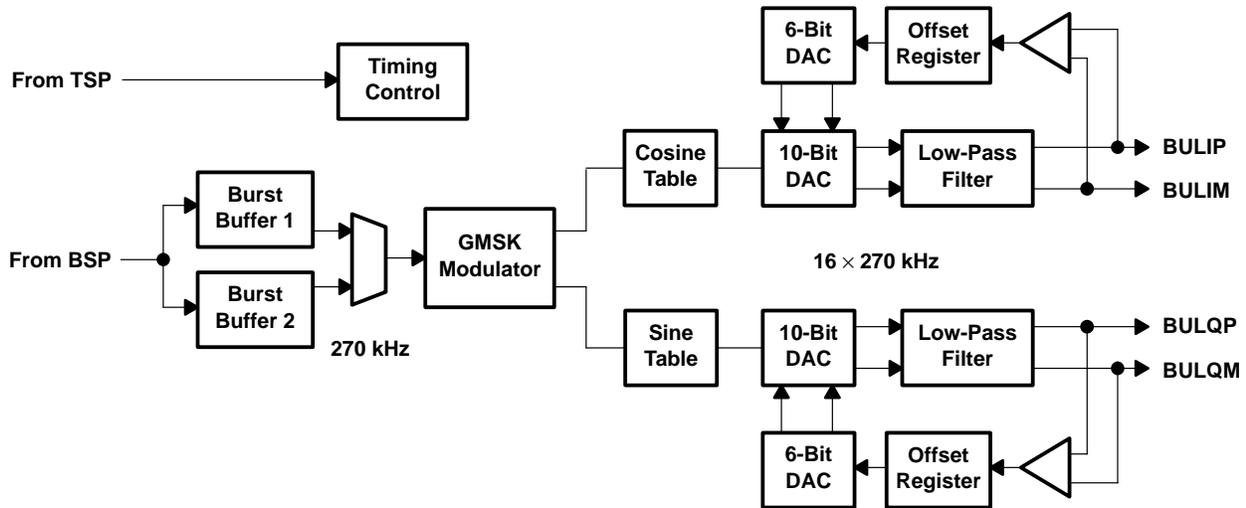
Figure 4–5. Baseband Uplink Block Diagram

4.2.2 Baseband Downlink Path

The BDL path includes two identical circuits for processing the analog baseband I and Q components generated by the RF circuits. The first stage of the BDL path is a continuous second-order anti-aliasing filter that prevents aliasing of out-of-band frequency components due to sampling in the ADC. This filter serves also as an adaptation stage between external and on-chip circuitry.

The antialiasing filter is followed by a fourth-order Σ-Δ modulator that performs analog-to-digital conversion at a sampling rate of 6.5 MHz. The ADC provides 2-bit words to a digital filter that performs the decimation by a ratio of 24 to lower the sampling rate to 270.8 kHz. The ADC also provides channel separation by providing enough rejection of the adjacent channels to allow the demodulation performances required by the GSM specification.

The BDL path includes an offset register, in which the value representing the channel dc offset is stored. This value is subtracted from the output of the digital filter before transmiting the digital samples to the DSP via the BSP. Upon reset, the offset register is loaded with 0s; its content is updated during the calibration process.

The typical sequence of a burst reception consists of:

1. Powering up the BDL path

2. Performing an offset calibration

3. Converting and filtering the I and Q components, and transmitting digital samples

Timing of this sequence is controlled via the TSP, which receives the serial real-time control signals from the TPU of the DBB device. Three real-time signals control the transmission of a burst: BDLON, BDLCAL, and BDLENA. Each signal corresponds to a time window.

BDLON high sets the BDL path in power-on mode after a delay corresponding to the power-on settling time of the analog block. BDLCAL enables the offset calibration window. Two offset calibration modes are possible and are selected by the state of bit 9 (EXTCAL) of the baseband codec control register (see Section 5.3.9.8). When EXTCAL is 0, the analog inputs are disconnected from the external world and internally shorted. The result of the conversion performed in this state is stored in the offset register. When EXTCAL is 1, the analog input remains connected to external circuitry, and the result of the conversion, including in this case internal offset plus external circuitry offset, is stored in the offset register. The duration of the calibration window depends mainly on the settling time of the digital filter.

Data conversion starts with the rising edge of the BDLENA signal; however the first eight I and Q samples are not transmitted to the DSP, because they are not meaningful due to the group delay of the digital filter. The rising edge

of BDLENA is also used by the IBIC to enable transfer of received data to the DBB device, via the BSP interface, during the entire reception window. At the falling edge of BDLENA, the conversion in progress is completed and samples are transmitted before stopping the conversion process. Finally, BDLON low sets the BDL path in power-down mode.
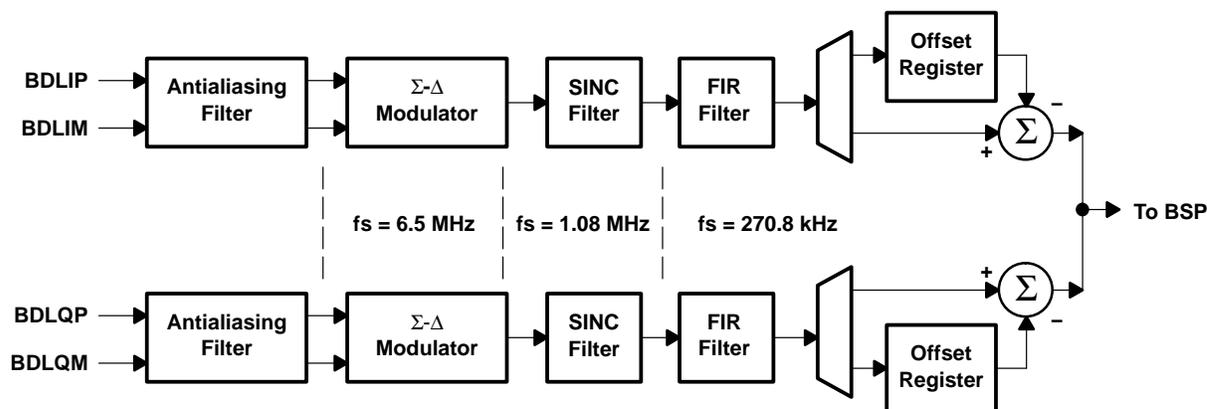
Figure 4–6. Baseband Downlink Block Diagram

4.3 Low-Dropout Voltage Regulators

The TWL3016 device allows three operating modes for the RABB, RIO, RDBB, RRAM, RMEM, and RSIM voltage regulators:

1. ACTIVE mode during which the regulator is able to deliver its full power

2. SLEEP mode during which the output voltage is maintained with a very low power consumption but with a low current capability

3. OFF mode during which the output voltage is not maintained and the power consumption is null

These regulators are rising up in ACTIVE mode only and each of them has a regulation ready signal, RSU. During the switched-off and backup states of the mobile phone, the voltage regulators are set to a SLEEP or OFF mode depending on the system requirements. The regulator voltages are decoupled by a low ESR capacitor connected across the corresponding V_{DD} and ground pins of the DBB package. Besides its voltage filtering function, this capacitor also has a voltage storage function that could give a delay for data protection purposes when the main battery is unplugged.

4.3.1 RDBB

RDBB is a low-dropout (LDO) voltage regulator that provides the power to the digital core located in the DBB device. RDBB is supplied from the main battery (VCDBB) and delivers two programmable regulated voltages (VRDBB and VSDBB). The VRDBB voltage value is programmable (three values) through the use of control bits 1 (RDBB1) and 0 (RDBB0) of the battery charging configuration register (see Section 5.3.7.5). The default value applied during mobile phone start-up 1.3 V, 1.5 V, or 1.8 V depends on the VLRTC and VLRTC0 input terminals level.

4.3.2 RRAM

RRAM is an LDO voltage regulator that provides the power to the external memory devices used in the GSM system (static RAM). RRAM is supplied from the main battery (VCRAM) and provides a regulated voltage (VRRAM). The VRRAM voltage value can be set to 1.8 V or 2.8 V using an external input signal (VLMEM). This voltage regulator prevents reverse current leakage in the OFF mode.

4.3.3 RMEM

RMEM is an LDO voltage regulator that provides the power supply to external memory devices used in the GSM system (Flash RAM). RMEM is supplied from the main battery (VCMEM) and provides a regulated voltage (VRMEM). The VRMEM voltage value can be set to 1.8 V or 2.8 V using an external input signal (VLMEM).

4.3.4 RIO

RIO is an LDO voltage regulator providing the power supply to the peripherals of the DBB device (including I/O and digital core of the TWL3016 device). RIO is supplied from the main battery on two terminals (VCIO1 and VCIO2) which are connected together internally. VRIO provides a 2.8-V regulated voltage on two output terminals (VRIO1 and VRIO2) which are also connected together internally. The TWL3016 device also requires externally connecting VCIO1 to VCIO2 and VRIO1 to VRIO2.

4.3.5 RABB

RABB is an LDO voltage regulator providing the power supply to the analog blocks of the TWL3016 device. RABB is supplied from the main battery (VCABB) and delivers a 2.8-V regulated voltage (VRABB). A separate ground return terminal (GNDA) is provided for the internal TWL3016 analog circuitry.

4.3.6 RUSB

RUSB is an LDO voltage regulator providing the power supply of external I/O linked to an USB interface. RUSB is supplied from the USB connector (VCUSB) and delivers a 3.3-V regulated voltage (VRUSB). An auto-detect circuitry allows an auto-start of the regulator (if bit 5 (RUSBEN) of the VRPC SIM card and regulators control register is set to 1, see Section 5.3.1.6) and updates a status register bit, when an USB insertion occurs.

4.3.7 RSIM

RSIM is an LDO voltage regulator providing the power supply of SIM card and SIM card drivers. RSIM is supplied from the main battery (VCDBB) and provides a programmable regulated voltage (VRSIM). The VRSIM output value can be set to 1.8 V or 2.95 V through the use of bit 0 (SIMSEL) of the VRPC SIM card and regulators control register (see Section 5.3.1.6).

4.3.8 RRTC

RRTC is an LDO voltage regulator that provides the power supply to the real-time clock (32-kHz oscillator) located in the DBB device and dedicated I/Os. RRTC is supplied from the UPR line, switched on the main or backup battery, depending on the mobile phone state. RRTC provides a programmable regulated voltage (VRRTC) and is always ON, as long as a valid energy source is present. The VRRTC voltage value is programmable (three values) through the use of bits 3 (RRTC1) and 2 (RRTC0) of the battery charging configuration register (see Section 5.3.7.5). Default value applied during mobile phone start-up 1.3 V, 1.5 V, or 1.8 V depends on the VLRTC and VLRTC0 input terminals level. The current load capability and the power consumption of this regulator are very low.
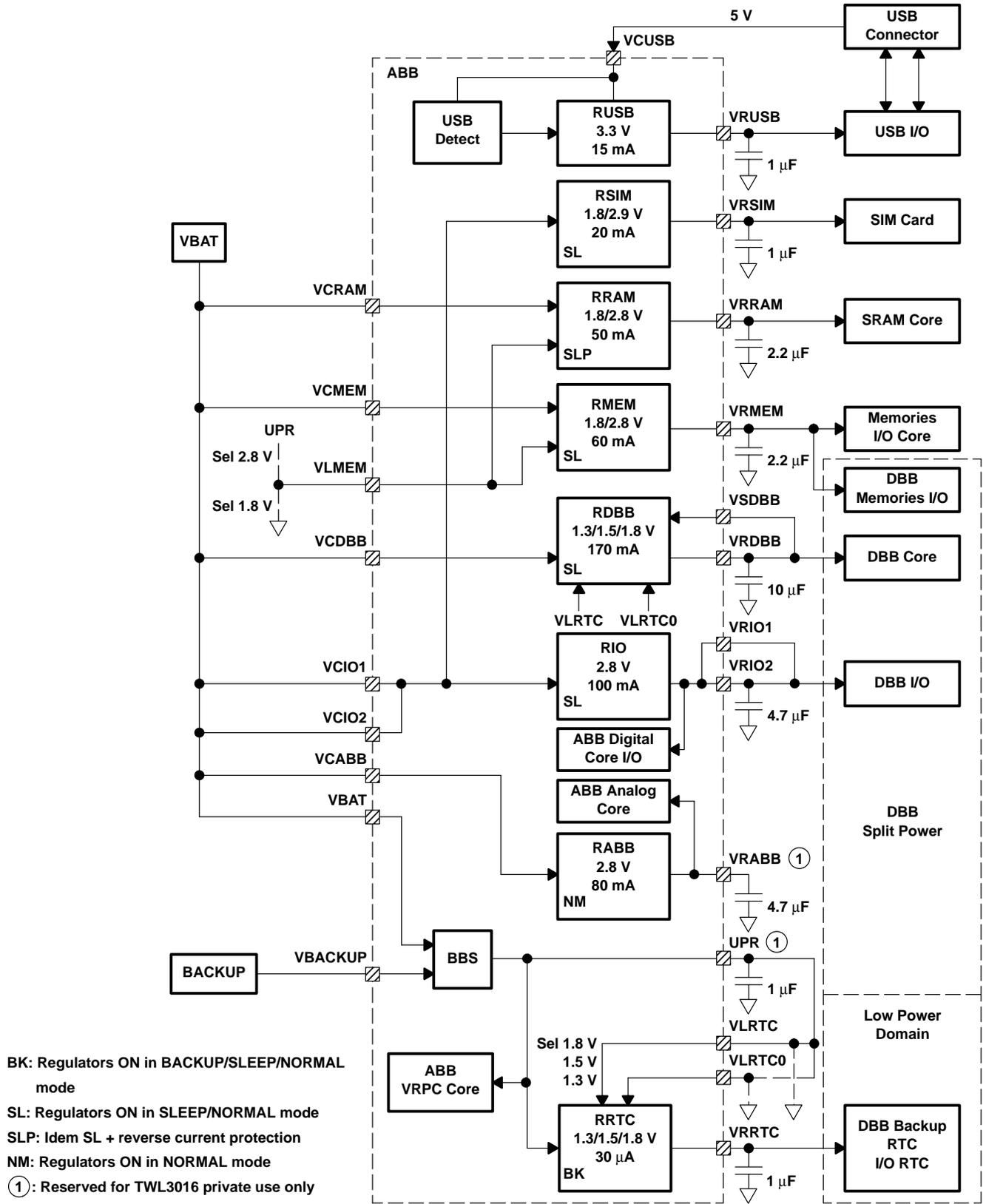
Figure 4–7. Voltage Supply System Block Diagram

BK: Regulators ON in BACKUP/SLEEP/NORMAL mode

SL: Regulators ON in SLEEP/NORMAL mode

SLP: Idem SL + reverse current protection

NM: Regulators ON in NORMAL mode

(1): Reserved for TWL3016 private use only

4.4 SIM Card Digital Interface

The SIM card digital interface ensures the translation of logic levels between the DBB device and SIM card for the transmission of three different signals: a clock derived from a clock elaborated in the DBB device to the SIM card (DBBSCK–SIMCK), a reset signal from the DBB device to the SIM card (DBBSRST–SIMRST), and serial data from the DBB device to SIM card (DBBSIO–SIMIO) and vice-versa.

External pull-up resistors must be connected on DBBSIO and SIMIO to VRIO and VRSIM, respectively.

Bit 3 (SIMLEN) of the VRPC SIM card and regulators control register (see Section 5.3.1.6) activates/deactivates the transmission of these signals.

When SIMLEN is 0, there is a low impedance 0 on terminals SIMRST, SIMCK, and SIMIO. This is also the case when there is no power on the SIM card, that is, when VRSIM = 0 V.
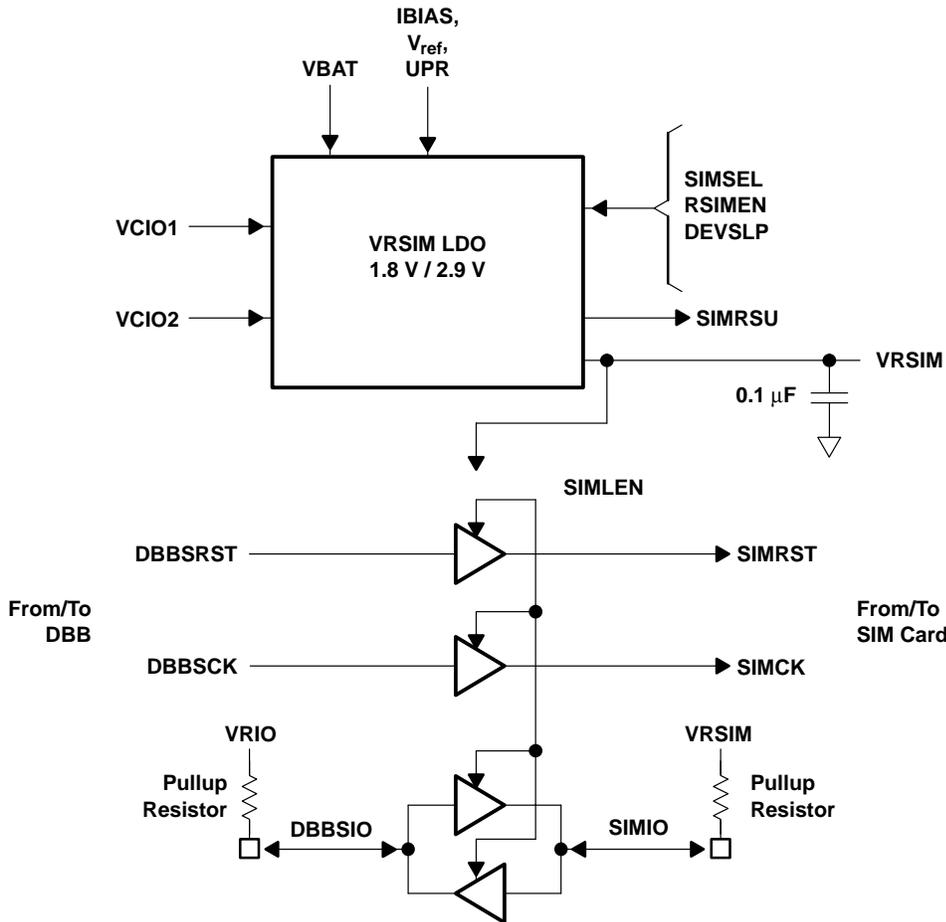
Figure 4–8. SIM Interface Block Diagram

4.5 Monitoring ADC

The monitoring section includes a 10-bit ADC and 10-bit/9-word RAM. The ADC monitors:

- Four internal analog values:
  - Battery voltage (VBAT)
  - Battery charger voltage (VCHG)
  - Current charger (current-to-voltage (I-to-V) converter) (ICHG)

- – Backup battery voltage (VBKP)
- Five external analog values:
  - – Battery type (ADIN1)
  - – Battery temperature (ADIN2)
  - – ADIN3
  - – ADIN4
  - – ADIN5

The selection of the input and reading of the control registers is done via the serial interfaces.

The power down is controlled by bit 4 (MADCON) of the power down register (see Section 5.3.3.3). If bit 5 (KEEPON) of the power down register is high, then the ADC converter is always on, even after a sequence of conversions. If the KEEPON bit is low, then the ADC converter is on after a conversion request and it is automatically off at the end of a sequence of conversions. At the end of a conversion cycle, an interrupt INT2 can be sent. A conversion cycle is launched:

- Programming a write access in one of the nine output data registers (VBATREG, VCHGREG, ICHGREG, VBKPREG, ADIN1REG, ADIN2REG, ADIN3REG, ADIN4REG, and ADIN5REG)
- Setting the STARTADC signal high through the TSP interface

4.6 Reference Voltage and Power Control

4.6.1 Block Descriptions

The band-gap voltage reference is filtered (RC filter) using an external capacitor connected across the VREF output and an analog ground (REFGND). The VREF voltage is scaled, distributed, and buffered inside the device. The band-gap is started in fast mode (not filtered) and is set automatically by the VRPC in the slow mode (filtered, less noisy) after a switch-on sequence.

The bias currents of the TWL3016 analog blocks are generated using an external resistor connected across the IBIAS terminal and an analog ground (REFGND). The current flowing through this resistor is then multiplied, mirrored, and distributed across the device.

A power-on reset block (POR) provides a reset signal for the VRPC state machine. This reset signal becomes high when the internal power supply rail (UPR) reaches 2.6 V on a rising edge and becomes back low when the power supply rail reaches 2.1 V on a falling edge. The POR block forces internal signal RSTz low as soon as possible during UPR ramp-up until UPR has passed the minimum operating voltage limit. For testing purposes, the TESTRESET signal provides an unconditional reset to the TWL3016 device.

An embedded timer allows a system reset (setting the RESPWONz output terminal to 0) if the PWON input terminal is maintained at a low value for longer than a PORSTD*T delay (~32 s).

UVLO is a comparison block. It compares the battery voltage to a reference (3.2 V). This second comparator has an hysteresis of 200 mV (below the threshold voltage 3.2 V) to avoid the variations of the main battery voltage when exceeding 3.2 V. The result of this comparison determines whether the next step can be reached during the logic from the OFF to ACTIVE state during a switch-on sequence.

The BBS has also a comparison block. It compares the battery voltage to a reference (2.8 V). The result of this comparison automatically generates a switch-off sequence from any state to the BACKUP state.

VRPCD is a digital block that is mainly composed of state machines and timers to control the switch-on and switch-off sequences.

4.6.2 Definitions

States:

- NOBAT state: the mobile phone is not powered by any battery.

- BACKUP state: the mobile phone is powered only with the backup battery and maintains only the VRRTC supply.

- OFF state: the mobile phone is powered by the main battery and maintains only the VRRTC supply.

- ACTIVE state: the mobile phone is powered by the main battery, all supplies are enabled, and the internal ABB reset is released.

- SLEEP state: the mobile phone is powered by the main battery, selected supplies are enabled, and the ABB device is in low consumption mode.

State transitions:

- Power on: the mobile phone is powered by the main or backup battery.

- Power off: the mobile phone is not powered by any battery.

- Switch on: the mobile phone is powered and awaken from the OFF state to reach the ACTIVE state.

- Switch off: the mobile phone is powered and switched from the ACTIVE or SLEEP state to reach the OFF or BACKUP state.

4.6.3 Power-On Condition

On the plug-in of a valid main battery, an internal reset is generated (POR); the level of UPR (above 2.6 V) controls its setting at 1 state.

After a power-on sequence, the TWL3016 device is in the OFF state.

4.6.4 Power-Off Condition

This state is reached when there is not enough voltage in the main and the backup batteries or when both batteries are disconnected.

4.6.5 Switch-On Condition

ON_PWON: when a falling edge is detected, after debouncing, on the PWON terminal.

ON REMOTE: When a falling edge is detected, after debouncing, on the RPWON or RPWON2 terminal.

IT_WAKE_UP: When a rising edge is detected on the ITWAKEUP terminal.

CHARGER_IC plugged: When a charger voltage rising above VBAT + 0.4 V is detected, after debouncing, on the VCHG terminal.

USB plugged: When an USB supply voltage above 3.8 V is detected (level detect), after debouncing, on the VCUSB terminal.

When these conditions occur in the switch-off state, the switch-on sequence is started and controlled by the VRPC.

There are two cases when these conditions do not start the switch-on sequence:

- When the main battery is under 3.2 V.

- When the system is in backup mode (power is supplied by the backup battery).

In the ACTIVE state, any switch-on condition is not considered but can generate an interrupt (charger IC plug, USB plug, PWON, RPWON, RPWON2 terminals). The 32-kHz clock automatically performs a debouncing, starting with the falling/rising edge of the PWON, RPWON, RPWON2, VCUSB, and VCHG terminals. The switch-on condition is taken in account, if still present, after the debouncing delay.

A third case may be programmed (using bit 9 (MSKBATCHK) of the VRPC SIM card and regulators control register, see Section 5.3.1.6) to avoid a switch-on sequence running with no main battery present. This case may occur when a battery charger is plugged in: the automatic precharge raises the main battery voltage up to 3.6 V even if no battery is connected. The main battery presence is checked, sensing the thermistor value through the ADIN2 terminal. The main battery presence check functionality is default inactive and implies the use of a backup battery. The value of the MSKBATCHK control bit is maintained in the BACKUP mode.

4.6.6 Switch-Off Condition

On MCU command: when the microcontroller sets bit 0 (DEVOFF) of the VRPC device mode register to 1 (see Section 5.3.1.2).

On main battery removal or deep discharge, when the main battery voltage is lower than 2.8 V (emergency condition), a debouncing delay is applied to the output of the 2.8-V comparator.

> **NOTE:** When a switch-off sequence is started, the sequence is completed even if a switch-on condition occurs.

4.6.7 Interrupt Handling

The VRPC block handles two kinds of interrupts:

- The interrupt related to the voltage level of the main battery resulting in an emergency switch-off procedure. This interrupt is considered as priority and sets the INT1 terminal to low.
- The interrupt related to accessories plugged/unplugged or the push button. These interrupts can generate a signal sent on the INT2 terminal active on low level, depending on the interrupt mask register. Events generating an INT2 are:
  - The charger is plugged or unplugged (managed by the battery charger interface).
  - There is a falling edge on the PWON terminal.
  - There is a rising/falling edge or low level after debouncing on the RPWON or RPWON2 terminal. The event detect mode is programmed using the VRPC device mode register (see Section 5.3.1.2).
  - An USB connector is plugged (USB supply detected) or unplugged.
  - The monitoring the ADC end-of-conversion interrupt
  - An over-voltage, over-temperature or end-of-charge current signaled by the battery charger interface comparator

The INT2 interrupts are generated in the ACTIVE and SLEEP modes. INT2 generation needs an internal clock CK13M or CK32K. Set bit 6 (ACTIVMCLK) of the power down register (see Section 5.3.3.3) properly in case the CK13M clock is not present.

4.6.8 Debouncing

The 32-kHz clock is used to automatically perform a debouncing, starting with: the falling/rising edge of the RPWON and RPWON2 terminals, the falling edge of PWON terminal, and the rising edge of the VCUSB and VCHG terminals. The terminal event is taken in account, if still present, after the debouncing delay. This delay is given by:

- NDEBB*TCK32K for the PWON, RPWON, and RPWON2 terminals
- NDEBV*TCK32K for the VCUSB and VCHG terminals, and the output of the 2.8-V comparator

Only one signal can be debounced at a time and the priority order of the PWON, RPWON, or RPWON2 terminal event over the debouncing process is the following:

1. RPWON
2. PWON
3. RPWON2

If the higher priority event is currently in the debouncing process, then the last activated signal is queued and will be debounced after the end of the previous debouncing process. If the lower priority event is currently in the debouncing process, then it will be delayed and the following event will be debounced.

NO-BAT

Enable VRRTC

PORz = 0   RESPWONz = 0   ABB RSTz = 0   ONnOFF = 0   REGEN = 0

All ABB and DBB are reset. VRDBB, VRMEM, VRIO, and VRABB are disabled.

VBAT > VBACKUP and VBAT > 2.6 V or
VBAT < VBACKUP and VBAT > 2.8 V

PORz = 1
RESPWONz = 1

CK32K Synchronous State Machine

VBAT < 2.8 V and
VBAT < VBACKUP

BACKUP ← → **OFF** **SLEEP** VBAT < 2.8 V

VBAT > 2.8 V or
VBAT > VBACKUP

Switch-On Condition   Switch-On Condition   ITWAKEUP = 1

VBAT < 2.8 V and   VBAT > 2.8 V or
VBAT < VBACKUP   VBAT > VBACKUP

Yes

PWON = 0 ?   No

Using MSKOFF ②
Disable VRxxx
Set REGEN Value
Disable/Sleep Band Gap
DEVOFF = 0
Reset VRPCSTS ②

INT2 = 0

Enable Band Gap

Enable
Sleep Mode
for
Band Gap
–
Using
MSKSLP ②
Enable
Sleep Mode
for
VRDBB
VRMEM
VRIO
VRABB
VRRAM
VRSIM
Set
REGEN
Value
Reset
VRPCSTS ②

Wait
PORSTD*T ②

Wait: NBGOFF*T   NBGSL*T ①

UPR <
2.1 V   PWON = 0

ABB RSTz = 0
ONnOFF = 0

No   VBAT >
3.2 V ?

ALL MODE ③

TESTRST = 1 ④

Yes
CHGSTS
= 1 ?

Enable
Band Gap
VRDBB, VRMEM
VRRAM, VRIO
VRABB
Set REGEN = 1

PORz = 0
RESPWONz = 0
ABB RSTz = 0
ONnOFF = 0

MSKBATCHK
= 0 ?   No

No

Yes

No   BATSTS = 1 ?   Yes

Wait 5*T
WATCH DOG TIMER

Enable VRDBB, VRABB, VRMEM
Set REGEN = 1, RAMEN = 1

Wait
SLPDLY*20T

②

Wait: NLD1OFF*T   NLD1SL*T ①

TESTRST = 0

RSTINT1 = 1

Regulator
OK ?

PORz = 1
RESPWONz = 1
ABB RSTz = 1
ONnOFF = 1

INT1 = 1   INT1 = 0

Enable VRIO

Wait: NLD2OFF*T   NLD2SL*T ①

Regulator
OK ?

No

Yes   MSKINT1
= 1 ?

ONnOFF = 1
ABB RSTz = 1
DEVSLP = 0

DEVOFF = 1   VBAT < 2.8 V   DEVSLP = 1

Active

① See VRPC State Machine Timing Characteristics

② See VRPC register decription

③ System reset is not available in BACKUP mode

④ TESTRST = 1 is for test/debug purposes only

PWON, RPWON, RPWON2 Event
VCHG, VCUSB Event
BCI Comparator Event → Send INT2

Figure 4–9. VRPC State Machine Flowchart

4.7   Automatic Frequency Control

The automatic frequency control function (AFC) consists of a DAC optimized for high-resolution dc conversion. The AFC digital interface includes two registers that can be written or read using either the BSP or the USP under the arbitration of the IBIC. The content of these registers controls a 13-bit DAC, operating at a sampling frequency set with the AFC working frequency register (see Section 5.3.4.3), whose purpose is to correct frequency shifts of the voltage-controlled oscillator to maintain the GSM 13-MHz master clock frequency in a 0.1-ppm range.

The AFC value is programmed with automatic frequency control register 1 (which contains the 10 LSBs) and automatic frequency control register 2 (which contains the 3 MSBs). The three MSBs are fed to the DAC through automatic frequency control register 2, whose content is updated with the content of a shadow register when LSBs are written in automatic frequency control register 1, so proper operation of the AFC is ensured by writing the MSBs first and then the LSBs.

Monotonicity is ensured by the structure of the DAC, with Σ-Δ digital modulators followed by an analog FIR, which performs one-bit digital-to-analog conversion and low-pass filtering. Further low-pass filtering is provided by the RC formed by the internal output resistor (25 kΩ) and an external capacitor (33 nF). However, most of the filtering is ensured by a voltage-controlled oscillator with high quality factor to provide a very low-frequency low-pass filtering.

Bit 3 (AFCON) of the power down register (see Section 5.3.3.3) controls power up of the AFC.

4.8   Automatic Power Control

The automatic power control (APC) generates an envelope signal to control the power ramp up, power ramp down, and power level of the radio burst. The APC structure is intended to support single-slot and multislot transmission with smooth power transition when consecutive bursts are transmitted at different power levels.

The APC includes a simple processor that generates 10-bit words at a rate of 2167 kHz. This processor computes the shape of the ramp-up and ramp-down transitions of the envelope signal from the value of the power level step and from the 16 coefficients of the desired shaping filter, which are stored in a random access memory (APCRAM) with an interpolation factor of 4. The power step is obtained by subtracting the content of the y-level registers which contains the previous power level from the x-level register which contains the new power level. The automatic power control RAM register (see Section 5.3.5.4) includes 16 10-bit words. The 5 LSBs of each word represent the coefficients of the ramp-up shaping filter, while the 5 MSBs represent the coefficients of the ramp-down shaping filter. Ramp-up or ramp-down coefficient selection depends on the sign of the power step to be performed—ramp-up for positive step and ramp-down for negative step.

Bit 6 (SEL256128) of the DAC input offset and gain register (see Section 5.3.5.5) allows selection of two slopes for ramp-up and ramp-down: a normal slope when SEL256128 is 0 and a multiplied-by-two slope when at 1.

The sum of the coefficients is normalized and must be equal to 256 for both ramp-up and ramp-down coefficients in the case of normal slope and equal to 128 in the case of X2 slope. The APCRAM register is loaded once with ramp-up and ramp-down shaping filter coefficients adapted to the power amplifier used if the RF section and only the power register need to be updated from burst to burst depending on the desired power of the radio burst. The sequence of digital input words of the DAC10 is given by the following expressions:

When SEL256128 = 0:

$$\text{level} = \text{level}_{\text{init}} + \Sigma_{I=0..15}\left(\text{step}_{\text{lev}}/256\right) * \left(\text{up[i]} * \left(1 - \text{sign}_{\text{step}}\right) + \text{dw[i]} * \text{sign}_{\text{step}}\right) \tag{1}$$

When SEL256128 = 1:

$$\text{level} = \text{level}_{\text{init}} + \Sigma_{I=0..15}\left(2 * \text{step}_{\text{lev}}/256\right) * \left(\text{up[i]} * \left(1 - \text{sign}_{\text{step}}\right) + \text{dw[i]} * \text{sign}_{\text{step}}\right) \tag{2}$$

where:

> level$_{init}$ is the current power level.

> step$_{lev}$ is the power level step to be done.

> up[i] are the coefficients of the ramp-up shaping filter.

> dw[i] are the coefficients of the ramp-down shaping filter.

> sign$_{step}$ is the sign of step$_{lev}$ (0 for plus, 1 for minus).

The shaping filter generates 16 steps for ramp-up and 16 steps for ramp-down. In order to minimize image frequencies due to this sampling, a 4-time linear interpolation generates a 64-step signal at the input of the DAC.

Before being fed to the 10-bit DAC (DAC10), the content of the offset register is added to the 10-bit words computed by the APC processor. The sum of the level register and the offset register must not be more than 1023. This offset generates a voltage at the APC output at power on to set the RF power amplifier to its conduction threshold.

The output of the 10-bit DAC is finally sent to the APC output through the output amplifier stage, which provides some low-pass continuous time filtering to smooth the APC signal.

Timing of the APC is generated by a control logic block for the signals coming from the TPS (BULON) and the baseband uplink digital BULD (BULDRAMP).

Two delay registers (APC ramp delay 1 (see Section 5.3.5.1) and APC ramp delay 2 (see Section 5.3.5.2)) contain two 10-bit words to control the effective start of the ramp-up or ramp-down relative to the BULDRAMP signal. APC ramp delay 1 register contains the 5 LSBs of the two 10-bit words while APC ramp delay 2 register contains the 5 MSBs of the two 10-bit words. This delay can be adjusted independently for ramp-up and ramp-down from 0 to 1023 by quarter-bit units.
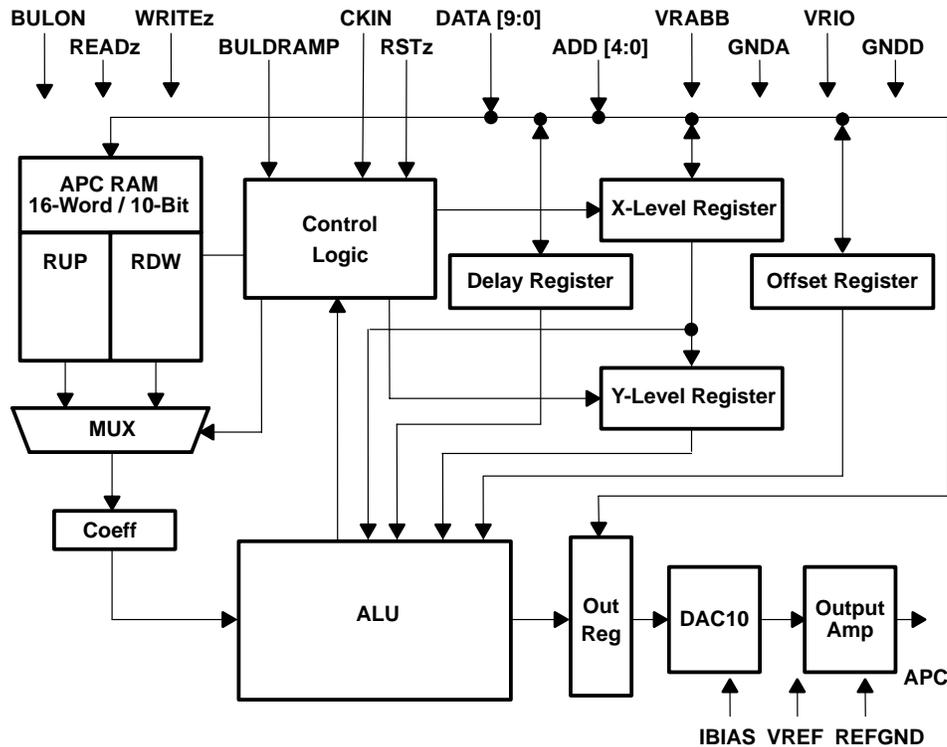
Figure 4–10. APC Block Diagram

4.9 Auxiliary DAC

Auxiliary DAC10 is a general-purpose 10-bit DAC. It includes a 10-bit register which can be accessed in read or write mode via the BSP or the USP under the arbitration of the IBIC, a 10-bit DAC, and an output amplifier.

4.10 Backup Battery Charge

The backup battery, in case it is rechargeable, can be recharged from the main battery. A programmable voltage regulator powered by the main battery allows recharging of the backup battery. The backup battery charge must be enabled using a control bit register and then started when the two following conditions are met:

1.   Main battery voltage > backup battery voltage

2.   Main battery > 2.8 V

The comparators of the BBS give the two thresholds of the backup battery charge start-up. The programmed voltage for the charger gives the end-of-charge threshold.

4.11 Main Battery Charger Interface

The charging device is a low-output impedance dc voltage source of 20 V absolute maximum. An external PMOS power transistor in series with a power Schottky diode, connected across terminals VCHG and VCCS of the TWL3016 device, controls the current flowing from the charging device to the main battery. The Schottky diode prevents reverse leakage current from the main battery in case the charging device is connected to the mobile phone without delivering any voltage at its output (charging device not plugged into the ac wall outlet, for example).

The main function of the battery charger interface is the charging control of both 1-cell Li-Ion battery or 3-series Ni-MH/Ni-Cd cell battery with the support of an external microcontroller.

The charging scheme for the Li-Ion battery is constant current first (typical current is 1xC) followed by constant voltage charging once a certain voltage threshold is reached (4.2 V typical). Charging is stopped when the charging current at constant voltage has decreased down to C/20 (typical). Because the BCI works in the linear mode, the power dissipation around the external components must be taken into account.

For the Ni-MH/Ni-Cd, the battery charging scheme is constant current only. Charging is stopped when ΔV across battery terminals versus time inverts from positive to slightly negative (typically, a few mV per cell) or by any other criteria involving battery voltage or battery temperature. Ni-MH/Ni-Cd 3-cell battery voltage can reach 5.5 V at the end of a charge cycle.

In addition to the above charging schemes, another scheme is systematically applied when a battery charger is connected to a switched off mobile phone: a constant charging current (typically C/20) is applied to the battery when the battery voltage is lower than 3.6 V. If the battery voltage is lower than 3.2 V (battery partially discharged or fully discharged), then the mobile phone is not started until the battery gets sufficiently recharged to greater than 3.2 V; when this happens, the microcontroller is started to control the fast charge cycle of the main battery, and the C/20 current is switched off.

A watchdog timer, using the CK32K clock, automatically stops the battery charging after a programmable delay, see Section 5.3.7.6, *Battery Charging Watchdog Register*.

4.11.1   Battery Monitoring

Battery monitoring is performed by the multiplexed 8-channel 10-bit ADC MADC used to measure the battery voltage, battery temperature, battery type, battery charge current, battery charger input voltage, and the backup battery voltage. The signals are converted into digital 10-bit words, stored in auxiliary ADC output registers (respectively, battery voltage conversion (see Section 5.3.2.3), analog 2 voltage conversion (see Section 5.3.2.8), analog 1 voltage conversion (see Section 5.3.2.7), battery current charger conversion (see Section 5.3.2.5), battery voltage charger conversion (see Section 5.3.2.4), and backup battery voltage conversion (see Section 5.3.2.6)) and transmitted to an external microcontroller via the USP interface.

Battery charging current is sensed using a 220-mΩ external resistor connected across the VCCS and VBATS terminals. The battery voltage value is measure using the VBAT terminal.

A battery over-voltage or battery over-temperature threshold can be set using the 10-bit main battery voltage charging register (see Section 5.3.7.1). A comparator, using bits 9 (PROCTL1) and 8 (PROCTL0) of the main battery current

charging register (see Section 5.3.7.2), and bit 9 (PROEN) of the battery control 2 register (see Section 5.3.7.4), switches off the charging current when the battery voltage or battery temperature reaches the threshold given by the main battery voltage charging register. An INT2 interrupt can be generated when the comparator detects the programmed threshold. A positive coefficient thermistor (connected to the ADIN2 terminal) is required to use the over-temperature detection feature.

4.11.2 Constant Current/Constant Voltage Charging

The magnitude of the reference charging current is set using the 8-bit main battery current charging register (see Section 5.3.7.2). An 8-bit DAC converts the contents of this register. The magnitude of the reference charging voltage is set using the 10-bit main battery voltage charging register (see Section 5.3.7.1). A 10-bit DAC converts the contents of this register. Both DAC outputs set the reference input of the analog charge loop. An error amplifier drives the gate of an external PMOS device via the ICTL terminal. Bit 0 (MESBAT) of the battery control 1 register (see Section 5.3.7.3) must be activated to allow a constant voltage charging mode.

Bits 4 (CHDISPA) and 2 (CHBPASSPA) of the battery control 2 register (see Section 5.3.7.4) set the external PMOS transistor to off or fully on.

For Li-Ion rechargeable batteries, when the battery voltage measured at the VBATS terminal by the MADC reaches 4.2 V ±30 mV, the microcontroller sets the charging control loop into constant voltage mode by changing bit 1 (CHIV) of the battery control 2 register from 1 to 0.

An external microcontroller must monitor the battery and control the charge loop via the USP serial interface.

During the constant voltage charging phase, the battery charging current is continuously monitored by the microcontroller through the use of the MADC. When this current goes below a certain limit (C/20) the battery is declared fully charged and the microcontroller terminates the charge by forcing bit 0 (CHEN) of the battery control 2 register to 0.

The end-of-charge current threshold can be set using the 8-bit main battery current charging register. A comparator allows, using bits 9 (PROCTL1) and 8 (PROCTL0) of the main battery current charging register, and bit 9 (PROEN) of the battery control 2 register, to switch off the charging current when the charge current fall below the threshold given by the main battery current charging register. An INT2 interrupt can be generated when the comparator detects the programmed threshold.

4.11.3 Main Battery Temperature and Main Battery Type Measurements

In order to measure the temperature and identify the type of the battery, the BCI includes dc current sources that provide a bias current through the ADIN1 and ADIN2 or ADIN3 input terminals of the MADC. These three terminals must be connected to the thermal sensing devices (thermistor) and to the battery type resistor. The resulting voltages can be measured using the MADC. For power consumption saving, these current sources are active only in switched-on mode when a measurement is required. The current source on ADIN2 or ADIN3 is programmable (3 bits) in the 10-µA to 80-µA range. The current source on ADIN1 is arbitrarily set to 10 µA.

Bit 6 (THEN) bit of the battery control 1 register (see Section 5.3.7.3) enables the thermistor current source. Bits 5–3 (THSENS(0–2)) set the current magnitude between 10 and 80 µA. Bit 8 (THENSA) allows the use of ADIN2 or ADIN3 input for thermal sensing. The battery type current source has a fixed value of 10 µA and is enabled by bit 7 (TYPEN).

A calibration routine storing the voltage across thermal sensor at two temperatures is necessary to compensate for dispersions of voltage across thermal sensor terminals.
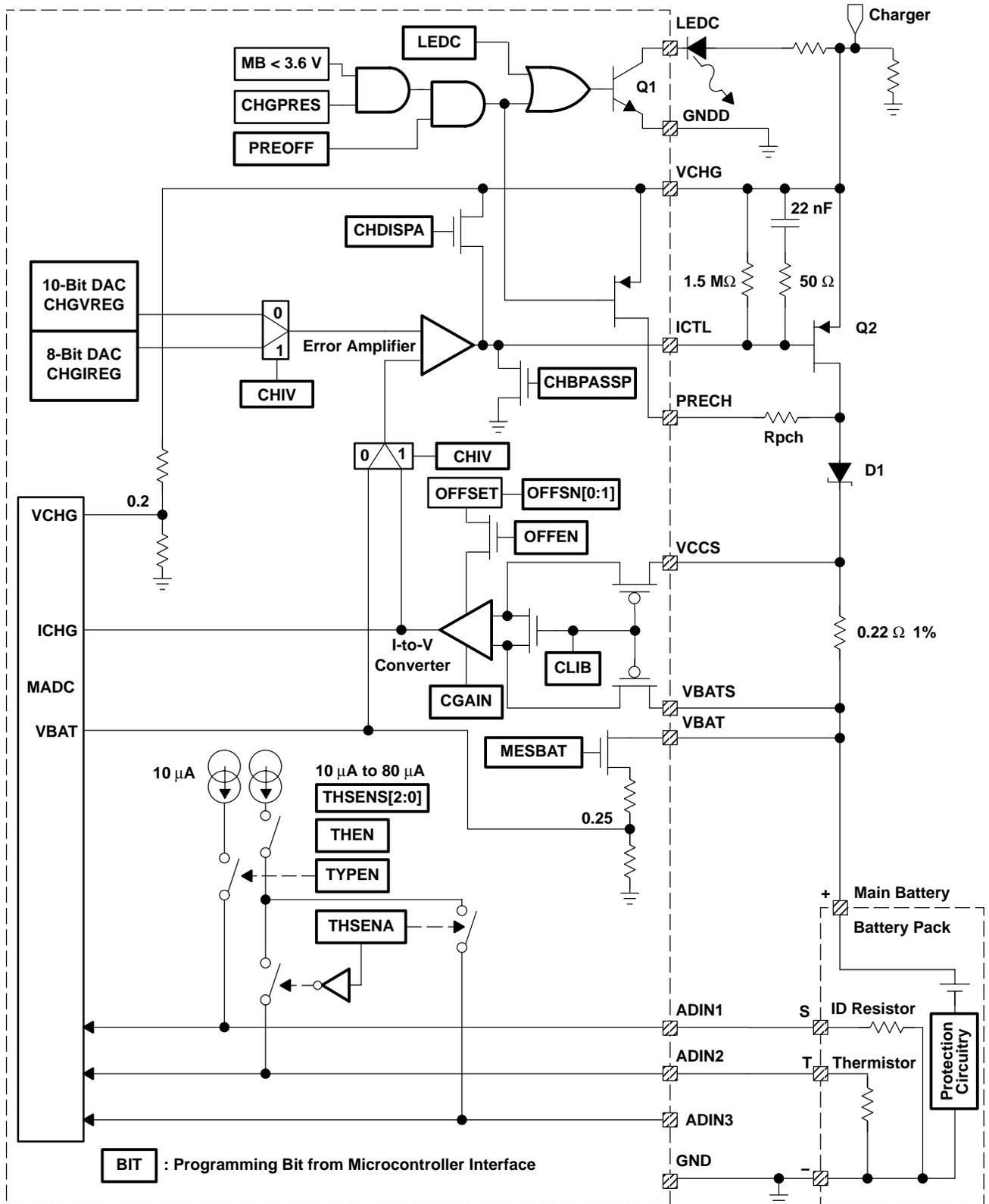
Figure 4–11. Battery Charger Block Diagram

4.12 Test Access Port

The TAP module provides a JTAG interface according to IEEE Std 1149.1. This interface uses the four dedicated I/O signals: TMS, TCK, TDI, and TDO.

The inputs TMS and TDI contain a pullup device which makes their state high when they are not driven; the input TCK contains a pulldown device which makes its state low when it is not driven; and the output TDO is a 3-state output which is high impedance except when data are shifted between TDI and TDO.

> TCK is the test clock signal.

> TMS is the test mode select signal.

> TDI is the scan path input.

> TDO is the scan path output.

The JTAG operations are controlled by a state machine, which is reset by the internal global reset.

A test mode is selected by writing a 5-bit word (instruction) into the instruction register (IR). This register consists of two stages: a shift register and a buffer register. The shift register is connected between TDI and TDO and allows a serial shift in of the instruction. The test access port instruction register (see Section 5.3.3.5) is either loaded with the value of the shift register (if WRTEN = 0) or through a serial interface (USP or BSP if WRTEN = 1), depending on the value of bit 0 (WRTEN) of the test access port control register (see Section 5.3.3.4).

4.12.1 Scan Registers

The TAP includes three scan registers.

The boundary scan register is inserted between the physical boundary (terminal) and the system boundary (internal signal). It is mainly intended for test at board level to capture the input terminal state, force the output terminal state, force the internal input signal, or capture the internal output signals, depending on the selected test mode (SAMPLE/ PRELOAD, EXTEST, or INTEST). These features check board connectivity between devices (EXTEST) or internally activate the device independently of the state of its input terminals (INTEST).

The identification register contains the ID code of the device.

The bypass register accesses test data registers in other components on a board-level test data path.

The scan registers are reset by the TWL3016 internal global reset RSTz during the test-logic-reset state from the state machine.

4.12.2 Public Instructions

As defined in IEEE Std1149.1 the public instructions are:

NAME	OPCODE	DESCRIPTION
BYPASS	11111 (63)	Connects the bypass register between TDI and TDO.
SAMPLE/ PRELOAD	00010 (02)	Connects the boundary scan register between TDI and TDO. This mode allows capturing a snapshot of device I/O states.
EXTEST	00000 (00)	Connects the boundary scan register between TDI and TDO. This mode allows capturing the state of the input terminals and forces the state of the output terminals. For example, it can be used for printed-circuit board connections test.
IDCODE	00001 (01)	Connects the identification register between TDI and TDO. This is the default configuration at reset. The identification register's content is: xxxx 0000 0000 0111 0111 0000 0010 1111 (xxxx represents the revision number)
INTEST	01001 (09)	Connects the boundary scan register between TDI and TDO. This mode allows forcing the internal system input signals via the parallel latches of the boundary register and to capture internal system outputs. (This mode can be used for device internal test independently of the state of its input terminals.) The internal master clock is derived from TCK and is active in the run-test-idle state of the state machine to allow single step operation of the device.

4.12.3 Boundary Scan

The boundary scan on analog terminals are only available as input boundary scan cell for capture mode only.

CELL	TYPE	NB SCAN CELL	ORDER	SIGNAL NAME
DBBSCK	Digital	1	1	Digital input
DBBSRST	Digital	1	2	Digital input
INT1TEST1	Digital	1	3	Digital output
INT2TEST2	Digital	1	4	Digital output
TEST3	Digital	3	5	Digital input
			6	Digital output
			7	Output disable
TEST4	Digital	3	8	Digital input
			9	Digital output
			10	Output disable
ADIN5	Analog	1	11	Analog input
ADIN4	Analog	1	12	Analog input
ADIN3	Analog	1	13	Analog input
ADIN2	Analog	1	14	Analog input
ADIN1	Analog	1	15	Analog input
BULIM	Analog	1	16	Analog input
BULIP	Analog	1	17	Analog input
BULQP	Analog	1	18	Analog input
BULQM	Analog	1	19	Analog input
BDLIM	Analog	1	20	Analog input
BDLIP	Analog	1	21	Analog input
BDLQP	Analog	1	22	Analog input
BDLQM	Analog	1	23	Analog input
APC	Analog	1	24	Analog input
AFC	Analog	1	25	Analog input
DAC	Analog	1	26	Analog input
MICIP	Analog	1	27	Analog input
MICIN	Analog	1	28	Analog input
AUXI	Analog	1	29	Analog input
HSMICIP	Analog	1	30	Analog input
HSMICBIAS	Analog	1	31	Analog input
MICBIAS	Analog	1	32	Analog input
HSOR	Analog	1	33	Analog input
HSOVMID	Analog	1	34	Analog input
HSOL	Analog	1	35	Analog input
AUXO	Analog	1	36	Analog input
EARN	Analog	1	37	Analog input
EARP	Analog	1	38	Analog input
AUVMID	Analog	1	39	Analog input
AUDR	Digital	1	40	Digital input
AUCK	Digital	1	41	Digital output
VCK	Digital	1	42	Digital output
VFS	Digital	1	43	Digital output

CELL	TYPE	NB SCAN CELL	ORDER	SIGNAL NAME
VDX	Digital	1	44	Digital output
VDR	Digital	1	45	Digital input
BFSX	Digital	1	46	Digital output
BDR	Digital	1	47	Digital input
BDX	Digital	1	48	Digital output
BFSR	Digital	1	49	Digital input
AUFS	Digital	1	50	Digital output
CK13M	Digital	1	51	Digital input
TDR	Digital	1	52	Digital input
TEN	Digital	1	53	Digital input
UEN	Digital	1	54	Digital input
UDX	Digital	2	55	Digital output
			56	Output disable
UDR	Digital	1	57	Digital input

5 Principles of Operation

5.1 Data and Address Format

Writing or reading registers via a serial interface is performed by transferring 16-bit words through the serial interface. Each word is split into three fields as follows:

- Data
- Address
- Read/Write

5.2 Internal Register Operations

DATA										ADDRESS					R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A4	A3	A2	A1	A0	1/0

Bits (15:6)   10 bits of data to be written or read

Bits (5:1)   5-bit address to be used in conjunction with the page register (see Section 5.3.8.3, *Page Select Register*)

Bit (0)   Cleared to 0 for a write, set to 1 for a read

5.2.1 Writing to Internal Register (Baseband Serial or Microcontroller Serial Port)

Bits (15:6)   This field contains the data to be written into the internal register

Bits (5:1)   This field contains the address to the register to be accessed

Bit (0)   Cleared to 0 indicates a write operation

5.2.2 Reading From Internal Register (Baseband Serial or Microcontroller Serial Port)

Bits (15:6)   This field is a don't care in a read request operation

Bits (5:1)   This field contains the address of the register to be accessed

Bit (0)   Set to 1 indicates a read operation

5.2.3 Baseband Burst Operations

During reception of a burst, transfer of radio data from the downlink baseband codec is accomplished by the TX part of the BSP serial interface in the following 16-bit word format.

DATA										ADDRESS					R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

As the I/Q samples are coded with 16-bit words, the data rate is 8.66 Mbps (or 270833 * 16 * 2). Since the digital clock CK13M is 13 MHz, the transfer is performed at 13 Mbps in burst mode. During burst reception, the DSP serial interface is idled about 33% of the time. Two adjacent transmissions are separated by a delay of about one 16-bit word transfer time.

Table 5–1. Register Cross Reference Listing

REGISTER	NAME	SECTION	REGISTER	NAME	SECTION
ADIN1REG	Analog 1 voltage conversion register	5.3.2.7	CHGVREG	Main battery voltage charging register	5.3.7.1
ADIN2REG	Analog 2 voltage conversion register	5.3.2.8	ICHGREG	Battery current charger conversion register	5.3.2.5
ADIN3REG	Analog 3 voltage conversion register	5.3.2.9	ITMASK	Interrupt mask register	5.3.8.1
ADIN4REG	Analog 4 voltage conversion register	5.3.2.10	ITSTATREG	Interrupt status register	5.3.8.2
ADIN5REG	Analog 5 voltage conversion register	5.3.2.11	MADCCTRL	Monitoring ADC control registers	5.3.2.1
AFCCTLADD	AFC working frequency register	5.3.4.3	MADCSTAT	Monitoring ADC status register	5.3.2.2
AFCOUT	AFC digital output register	5.3.4.4	PAGEREG	Page select register	5.3.8.3
APCDEL1	APC ramp delay 1 register	5.3.5.1	PWDNRG	Power down register	5.3.3.3
APCDEL2	APC ramp delay 2 register	5.3.5.2	TAPCTRL	Test access port control register	5.3.3.4
APCOFF	DAC input offset and gain register	5.3.5.5	TAPREG	Test access port instruction register	5.3.3.5
APCOUT	APC output register	5.3.5.6	TOGBR1	Toggle bits register 1	5.3.3.1
APCRAM	Automatic power control RAM register	5.3.5.4	TOGBR2	Toggle bits register 2	5.3.3.2
AUXAFC1	Automatic frequency control register 1	5.3.4.1	VAUDCTRL	Audio control register	5.3.10.6
AUXAFC2	Automatic frequency control register 2	5.3.4.2	VAUDPLL	Audio PLL register	5.3.10.9
AUXAPC	Automatic power control register	5.3.5.3	VAUOCTRL	Audio outputs control register	5.3.10.7
AUXDAC	Auxiliary DAC control register	5.3.6	VAUSCTRL	Audio stereo path control register	5.3.10.8
BBCFG	Baseband codec configuration register	5.3.9.9	VBATREG	Battery voltage conversion register	5.3.2.3
BBCTRL	Baseband codec control register	5.3.9.8	VBCTRL1	Voiceband control register 1	5.3.10.1
BCICONF	Battery charging configuration register	5.3.7.5	VBCTRL2	Voiceband control register 2	5.3.10.2
BCICTL1	Battery control 1 register	5.3.7.3	VBDCTRL	Voiceband downlink control register	5.3.10.5
BCICTL2	Battery control 2 register	5.3.7.4	VBKPREG	Backup battery voltage conversion register	5.3.2.6
BCIWDOG	Battery charging watchdog register	5.3.7.6	VBPOP	Voiceband pop reduction register	5.3.10.3
BULDATA1	Baseband uplink data buffer 1 register	5.3.9.6	VBUCTRL	Voiceband uplink register	5.3.10.4
BULDATA2	Baseband uplink data buffer 2 register	5.3.9.7	VCHGREG	Battery voltage charger conversion register	5.3.2.4
BULGCAL	Baseband uplink absolute gain calibration register	5.3.9.5	VRPCCFG	VPRC configuration register	5.3.1.1
BULIDAC	Baseband uplink I DAC register	5.3.9.3	VRPCDEV	VPRC device mode register	5.3.1.2
BULIOFF	Baseband uplink I offset register	5.3.9.1	VRPCMSKSLP	VPRC sleep mode mask register	5.3.1.3
BULQDAC	Baseband uplink Q DAC register	5.3.9.4	VRPCMSKOFF	VPRC off mode mask register	5.3.1.4
BULQOFF	Baseband uplink Q offset register	5.3.9.2	VRPCSIMR	VRPC SIM card and regulators control register	5.3.1.6
CHGIREG	Main battery current charging register	5.3.7.2	VRPCSTS	VRPC status register	5.3.1.5

Table 5–2. Register Map

PG	ADD	REGISTER	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	–	Reserved									
0	1	PAGEREG	Reserved						BSPP1	BSPP0	UCP1	UCP0
0	2	APCDEL1	DELD(4:0)					DELU(4:0)				
0	3	BULDATA1	bit 0	//	//	//	//	//	//	//	//	bit 159
0	3	BULDATA2	bit 0	//	//	//	//	//	//	//	//	bit 159
0	4	TOGBR1	MADCS	MADCR	AFCS	AFCR	ADACS	ADACR	VDLS	VDLR	VULS	VULR
0	5	TOGBR2	Reserved	AUDS	AUDR	IAPCTR	IBUFPTR2	IBUFPTR1	ACTS	ACTR	KEEPS	KEEPR
0	6	VBDCTRL	Reserved		VOLCTL(2:0)			VDLPG(3:0)				
0	7	AUXAFC1	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	8	AUXAFC2	–							bit 12	bit 11	bit 10
0	9	AUXAPC	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	10	APCRAM	DWN–0 to DWN–15					UP–0 to UP–15				
0	11	APCOFF	Reserved		SEL256128	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	12	AUXDAC	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	13	MADCCTRL	Reserved	ADIN5CV	ADIN4CV	ADIN3CV	ADIN2CV	ADIN1CV	VBKPCV	ICHGCV	VCHGCV	VBATCV
0	14	CHGIREG	PROCTL(1:0)		CHGI(7:0)							
0	15	VBATREG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	16	VCHGREG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	17	ICHGREG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	18	VBKPREG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	19	ADIN1REG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	20	ADIN2REG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	21	ADIN3REG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	22	ADIN4REG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	23	ADIN5REG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	24	MADCSTAT	Reserved									ADCBUSY
0	25	CHGVREG	CHGV(9:0)									
0	26	ITMASK	Reserved			BCICOMP _IT_MSK	ADCEND _IT_MSK	USB_IT _MSK	CHRGER_ IT_MSK	PUSHOFF _IT_MSK	REMOTE _IT_MSK	REMOTE2 _IT_MSK
0	27	ITSTATREG	Reserved			BCICOMP	ADCEND	USB	CHRGER	PUSHOFF	REMOTE	REMOTE2
0	28	BCICTL1	OFFEN	THENSA	TYPEN	THEN	THSENS(2:0)			OFFSN(1:0)		MESBAT
0	29	BCICTL2	PROEN	RSVD	PREOFF	CGAIN4	LEDC	CHDISPA	CLIB	CHBPASS PA	CHIV	CHEN
0	30	VRPCDEV	Reserved						RP2DLEV	RPDLEV	DEVSLP	DEVOFF
0	31	VRPCSTS	R2PSTS	RPSTS	USBSTS	CHGSTS	PWONSTS	ITWSTS	DEVOLD	RSTINT1	MSKBINT1	MSKINT1

Table 5–2. Register Map (continued)

PG	ADD	REGISTER	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	0	–	Reserved									
1	1	PAGEREG	Reserved						BSPP1	BSPP0	UCP1	UCP0
1	2	BULIOFF	Reserved	ULIOFF(8:0)								
1	3	BULQOFF	Reserved	ULQOFF(8:0)								
1	4	BULQDAC	ULQDAC(9:0)									
1	5	BULIDAC	ULIDAC(9:0)									
1	6	BBCTRL	EXTCAL	OUTLEV(2:0)			MSLOT	Reserved	BALOOP	SELVMID(2:0)		
1	7	VBUCTRL	DXEN	VDLST(3:0)				VULPG(4:0)				
1	8	VBCTRL1	VFBYP	VBDF AUXG	VSYNC	VCLK MODE	VALOOP	MICBIAS	VUL SWITCH	Reserved		
1	9	PWDNRG	Reserved		AUDON	ACTIV MCLK	KEEPON	MADCON	AFCON	ADACON	VDLON	VULON
1	10	VBPOP	AUXFBYP	Reserved	AUXAUTO	AUXFDIS	EARAUTO	EARCHG	EARDIS	HSOAUTO	HSOCHG	HSODIS
1	11	VBCTRL2	Reserved	VMIDSEL	VMIDFBYP	WBA	HSDIF	HSOVMID	SPKG	MICBIASEL	Reserved	HSMICSEL
1	12	APCOUT	APC(9:0)									
1	13	BCICONF	BATSTS	BBSEL(1:0)		MESBB	BBCHGEN	VBATCHK EN	RRTC(1:0)		RDBB(1:0)	
1	14	BULGCAL	Reserved	QAG(3:0)			Reserved	IAG(3:0)				
1	15	VAUDCTRL	VSPCK	AUGA	SRW(2:0)			VULBST	HPFBYP	MONOL	MONOR	Reserved
1	16	VAUSCTRL	AURGA(4:0)					AULGA(4:0)				
1	17	VAUOCTRL	EAR(1:0)		AUX(1:0)		SPK(1:0)		HSOL(1:0)		HSOR(1:0)	
1	18	VAUDPLL	Reserved	I2SON	SFTVOL(1:0)		BYPSFTV	Reserved			AUPLLON	TPLLON
1	19	TAPCTRL	Reserved									WRTEN
1	20	TAPREG	VER(3:0)				IR(5:0)					
1	21	AFCCTLADD	Reserved							AFCBYP	AFCCK(1:0)	
1	22	AFCOUT	Reserved		DOUT(7:0)							
1	23	VRPCSIMR	MSKBAT CHK	RAMRSU	RRAMEN	USBRSU	RUSBEN	REGEN	SIMLEN	SIMRSU	RSIMEN	SIMSEL
1	24	BCIWDOG	WOVF	WEN	KEY(7:0)							
1	25	–	Reserved									
1	26	APCDEL2	DELD(9:5)					DELU(9:5)				
1	27	ITSTATREG	Reserved			BCICOMP	ADCEND	USB	CHRGER	PUSHOFF	REMOTE	REMOTE2
1	28	BBCFG	Reserved		SKIPCT(4:0)					BBMODE(1:0)		OFFSEN
1	29	VRPCMSK OFF	MSKOFFR	Reserved	MSKOFF REN	MSKOFF USB	MSKOFF ABB	MSKOFF SIM	MSKOFF DBB	MSKOFF RAM	MSKOFF MEM	MSKOFF IO
1	30	VRPCCFG	R2PWOND	RPWOND	USBPRES	CHGPRES	PWOND	SLPDLY(4:0)				
1	31	VRPCMSK SLP	MSKSLPR	MSKSLPV	MSKSLP REN	MSKSLP USB	MSKSLP ABB	MSKSLP SIM	MSKSLP DBB	MSKSLP RAM	MSKSLP MEM	MSKSLP IO

5.3 Register Description

5.3.1 Voltage Reference and Power Control (VRPC) Registers

5.3.1.1 VRPC Configuration Register

Register: **VRPCCFG**
Page: 1
Address: 30 (11110b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	R2PWOND	RPWOND	USBPRES	CHGPRES	PWOND	SLPDLY(4:0)				
Access Type	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W
Value At Reset	1 †	1 †	0 †	0 †	1 †	1	1	1	1	1
Value At Por	1	1	0	0	1	1	1	1	1	1

† Value depends on the corresponding TWL3016 terminal value.

Table 5–3. VRPC Configuration Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	R2PWOND	RPWON2 terminal status after debouncing.
8	RPWOND	RPWON terminal status after debouncing.
7	USBPRES	When this bit is set to 1, it indicates the presence of an unregulated USB supply.
6	CHGPRES	When this bit is set to 1, it indicates the presence of a battery charger.
5	PWOND	PWON terminal status after debouncing.
4–0	SLPDLY(4:0)	Delay before going into sleep mode is SLPDLY(4..0)*(16+4)*TCK32K.

5.3.1.2 VRPC Device Mode Register

Register: **VRPCDEV**
Page: 0
Address: 30 (11110b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD						RP2DLEV	RPDLEV	DEVSLP	DEVOFF
Access Type	R	R	R	R	R	R	R	R	R/W/U †	R/W/U †
Value At Reset	0	0	0	0	0	0	1	1	0	0

† Value may be updated by the VRPC state machine.

Table 5–4. VPRC Device Mode Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–5	RSVD	Reserved.
4	RP2DLEV	RPWON2 terminal event detect mode: 0 = Rising/falling edge detect 1 = High/low detect
2	RPDLEV	RPWON terminal event detect mode: 0 = Rising/falling edge detect 1 = High/low detect
1	DEVSLP	When this bit is set to 1, start the SLT to switch the voltage regulators into SLEEP mode.
0	DEVOFF	When this bit is set to 1, start the WDT to switch the voltage regulators into OFF mode.

5.3.1.3 VRPC Sleep Mode Mask Register

Register: **VRPCMSKSLP**
Page: 1
Address: 31 (11111b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	MSKSLPR	MSKSLPV	MSKSLP REN	MSKSLP USB	MSKSLP ABB	MSKSLP SIM	MSKSLP DBB	MSKSLP RAM	MSKSLP MEM	MSKSLP IO
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	1	1	0	0	0	0	0 †

† Value of this control bit must be set to 1 only when bit 5 (MSKSLPABB) = 0.

Table 5–5. VRPC Mask Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	MSKSLPR	When this bit is set to 1 and the ABB device is in SLEEP mode, bits RRTC[1:0] = 01 and RDBB[1:0] = 01 in the battery charging configuration register (see Section 5.3.7.5).
8	MSKSLPV	When this bit is set to 1 and the ABB device is in SLEEP mode, the main bandgap (accurate) is kept on.
7	MSKSLPREN	When this bit is cleared and the ABB device is in SLEEP mode, the REGEN signal keeps its previous value. When this bit is set to 1 and the ABB device is in SLEEP mode, the REGEN signal is cleared to 0.
6	MSKSLPUSB	When this bit is set to 1 and the ABB device is in SLEEP mode, the VRUSB regulator is in OFF mode (instead of SLEEP mode).
5	MSKSLPABB	When this bit is set to 1 and the ABB device is in SLEEP mode, the VRABB regulator is in OFF mode (instead of SLEEP mode).
4	MSKSLPSIM	When this bit is set to 1 and the ABB device is in SLEEP mode, the VRSIM regulator is in OFF mode (instead of SLEEP mode).
3	MSKSLPDBB	When this bit is set to 1 and the ABB device is in SLEEP mode, the VRDBB regulator is in OFF mode (instead of SLEEP mode).
2	MSKSLPRAM	When this bit is set to 1 and the ABB device is in SLEEP mode, the VRRAM regulator is in OFF mode (instead of SLEEP mode).
1	MSKSLPMEM	When this bit is set to 1 and the ABB device is in SLEEP mode, the VRMEM regulator is in OFF mode (instead of SLEEP mode).
0	MSKSLPIO	When this bit is set to 1, bit 5 (MSKSLPABB) is set to 0, and the ABB device is in SLEEP mode, the VRIO regulator keeps its full load current capability (ACTIVE mode).

5.3.1.4 VRPC Off Mode Mask Register

Register: **VRPCMSKOFF**
Page: 1
Address: 29 (11101b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	MSKOFFR	RSVD	MSKOFF REN	MSKOFF USB	MSKOFF ABB	MSKOFF SIM	MSKOFF DBB	MSKOFF RAM	MSKOFF MEM	MSKOFF IO
Access Type	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–6. VRPC Mask VRABB Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	MSKOFFR	When this bit is set to 1 and the ABB device is in OFF mode, bits RRTC[1:0] = 01 and RDBB[1:0] = 01 in the battery charging configuration register (see Section 5.3.7.5).
8	RSVD	Reserved.
7	MSKOFFREN	When this bit is set to 1 and the ABB device is in OFF mode, the REGEN signal keeps its previous value. When this bit is cleared and the ABB device is in OFF mode, the REGEN signal is set to 0.
6	MSKOFFUSB	When this bit is set to 1 and the ABB device is in OFF mode, the VRUSB regulator is in SLEEP mode.
5	MSKOFFABB	When this bit is set to 1 and the ABB device is in OFF mode, the VRABB regulator is in SLEEP mode.
4	MSKOFFSIM	When this bit is set to 1 and the ABB device is in OFF mode, the VRSIM regulator is in SLEEP mode.
3	MSKOFFDBB	When this bit is set to 1 and the ABB device is in OFF mode, the VRDBB regulator is in SLEEP mode.
2	MSKOFFRAM	When this bit is set to 1 and the ABB device is in OFF mode, the VRRAM regulator is in SLEEP mode.
1	MSKOFFMEM	When this bit is set to 1 and the ABB device is in OFF mode, the VRMEM regulator is in SLEEP mode.
0	MSKOFFIO	When this bit is set to 1 and the ABB device is in OFF mode, the VRIO regulator is in SLEEP mode.

5.3.1.5 VRPC Status Register

Register: **VRPCSTS**
Page: 0
Address: 31 (11111b)
Read/Write: 0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RP2STS	RPSTS	USBSTS	CHGSTS	PWONSTS	ITWSTS	DEVOLD	RSTINT1	MSKBINT1§	MSKINT1§
Access Type	R	R	R	R	R	R	R	R/W	R/W	R/W
Value At Reset	1/0 ‡	1/0 ‡	1/0 ‡	1/0 ‡	1/0 ‡	1/0 ‡	1/0 ‡	0	0	0/1 †

† Value is 1 for a TESTRST start-up.
‡ Value is 0 for a TESTRST start-up.
§ Value of these control bits must be set to 0 before programming a SLEEP state.

Table 5–7. VRPC Status Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	RP2STS	This bit is set to 1 when an RPWON2 signal transition from 0 to 1 initiates a switch-on condition or an exit from the SLEEP mode. This bit is not cleared when the ABB device changes its mode from ACTIVE to SLEEP.
8	RPSTS	This bit is set to 1 when an RPWON signal transition from 0 to 1 initiates a switch-on condition or an exit from the SLEEP mode. This bit is not cleared when the ABB device changes its mode from ACTIVE to SLEEP.
7	USBSTS	This bit is set to 1 when an USB plug initiates a switch-on condition or an exit from the SLEEP mode. This bit is not cleared when the ABB device changes its mode from ACTIVE to SLEEP.
6	CHGSTS	This bit is set to 1 when a charger IC plug initiates a switch-on condition or an exit from the SLEEP mode. This bit is not cleared when the ABB device changes its mode from ACTIVE to SLEEP.
5	PWONSTS	This bit is set to 1 when an ON button push initiates a switch-on condition or an exit from the SLEEP mode. This bit is not cleared when the ABB device changes its mode from ACTIVE to SLEEP.
4	ITWSTS	This bit is set to 1 when an IT_WAKEUP initiates a switch-on condition or an exit from SLEEP mode. This bit is not cleared when the ABB device changes its mode from ACTIVE to SLEEP.
3	DEVOLD	OFF state trigger: 1 = Current OFF state is due to an emergency condition (VBAT < 2.8 V) 0 = Current OFF state is due to bit 0 (DEVOFF) of the VRPC device mode register being set to 1 (see Section 5.3.1.2).
2	RSTINT1	When this bit is set to 1, the INT1 interrupt transmit is aborted.
1	MSKBINT1	When this bit is set to 1, the mask INT1 interrupt during a baseband transmit operation (during BULENA = 1) is enabled.
0	MSKINT1	When this bit is set to 1, the mask INT1 emergency switch off interrupt is enabled.

5.3.1.6 VRPC SIM Card and Regulators Control Register

Register: **VRPCSIMR**
Page: 1
Address: 23 (10111b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	MSKBATCHK	RAMRSU	RRAMEN	USBRSU	RUSBEN	REGEN	SIMLEN	SIMRSU	RSIMEN	SIMSEL
Access Type	R/W	R	R/W/U †	R	R/W	R/W/U †	R/W	R	R/W	R/W
Value At Reset	1	1	1	0	0	1	0	0	0	0

† Value may be updated by the VRPC state machine.

Table 5–8. SIM Card and Regulators Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	MSKBATCHK	Setting this bit to 1 bypasses the main battery presence check during the VRPC STM switch-on sequence.

8	RAMRSU	VRRAM regulator output status:
		    0 = The regulator is not in regulation mode.
		    1 = Regulated voltage is available.

7	RRAMEN	When this bit is set to 1, the VRRAM regulator is enabled.

6	USBRSU	VRUSB regulator output status:
		    0 = The regulator is not in regulation mode.
		    1 = Regulated voltage is available.

5	RUSBPEN	When this bit is set to 1, the VRUSB regulator is enabled.
4	REGEN	Set the value of the REGEN terminal.
3	SIMLEN	When this bit is set to 1, the SIM card level shifter is enabled (SIMCK, SIMIO, and SIMRST are enabled).

2	SIMRSU	VRSIM regulator output status:
		    0 = The regulator is not in regulation mode.
		    1 = The regulator is on, the SIM card is correctly supplied.

1	RSIMEN	When this bit is set to 1, the VRSIM regulator is enabled.

0	SIMSEL	Select the VRSIM output voltage:
		    0 = 1.8 V
		    1 = 2.9 V

5.3.2 Monitoring ADC Registers

A buffer register is used for the monitoring ADC control register. A write in the register accesses the buffer register. Upon a request for conversion, the master register is updated with the contents of the buffer register. A read from either register accesses the master register. If the read occurs before a conversion request, then the configuration of the last conversion is read. If the read occurs after a conversion request and before the interrupt signaling the end of conversion, then the configuration of the current conversion is read. A write to these registers during a conversion sequence has no effect on the current conversion (see Table 5–8). The user need not be concerned with the distinction between the two registers, only the behavior of the register accessed by the address.

5.3.2.1 Monitoring ADC Control Register

Register: **MADCCTRL**
Page: 0
Address: 13 (01101b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	ADIN5CV	ADIN4CV	ADIN3CV	ADIN2CV	ADIN1CV	VBKPCV	ICHGCV	VCHGCV	VBATCV
Access Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Register: **MADCCTRL Buffer**
Write: 0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	ADIN5CV	ADIN4CV	ADIN3CV	ADIN2CV	ADIN1CV	VBKPCV	ICHGCV	VCHGCV	VBATCV
Access Type	–	W	W	W	W	W	W	W	W	W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Register: **MADCCTRL Master**
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	ADIN5CV	ADIN4CV	ADIN3CV	ADIN2CV	ADIN1CV	VBKPCV	ICHGCV	VCHGCV	VBATCV
Access Type	R	R	R	R	R	R	R	R	R	R
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–9. Monitoring ADC Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	RSVD	Reserved.
8	ADIN5CV	This bit selects a conversion of the ADIN5 input. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
7	ADIN4CV	This bit selects a conversion of the ADIN4 input. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
6	ADIN3CV	This bit selects a conversion of the ADIN3 input. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
5	ADIN2CV	This bit selects a conversion of the ADIN2 input. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
4	ADIN1CV	This bit selects a conversion of the ADIN1 input. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
3	VBKPCV	This bit selects a conversion of the backup battery voltage. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
2	ICHGCV	This bit selects a conversion of the charger battery current. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
1	VCHGCV	This bit selects a conversion of the charger battery voltage. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
0	VBATCV	This bit selects a conversion of the battery voltage. When it is set to 1, a conversion of this input is expected during the next conversion sequence.

5.3.2.2 Monitoring ADC Status Register

Register: **MADCSTAT**
Page: 0
Address: 24 (11000b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Name					RSVD					ADCBUSY
Access Type	–	–	–	–	–	–	–	–	–	R
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–10. Monitoring ADC Status Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–1	RSVD	Reserved.
0	ADCBUSY	If this bit is set to 1, a conversion is currently on-going.

5.3.2.3 Battery Voltage Conversion Register

Register: **VBATREG**
Page: 0
Address: 15 (01111b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value At Reset	1	1	1	1	1	1	1	1	1	1

Table 5–11. Battery Voltage Conversion Register Description

DATA BIT	DESCRIPTION
9–0	Output of the 10-bit monitoring ADC for the voltage of the battery. This register is read only.[†]

[†] A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC status register is 0 (see Section 5.3.2.2) and the MADC module is powered on.

5.3.2.4 Battery Voltage Charger Conversion Register

Register: **VCHGREG**
Page: 0
Address: 16 (10000b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value At Reset	1	1	1	1	1	1	1	1	1	1

Table 5–12. Battery Voltage Charger Conversion Register Description

DATA BIT	DESCRIPTION
9–0	Output of the 10-bit monitoring ADC for the voltage of the battery charger. This register is read only.[†]

[†] A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC status register is 0 (see Section 5.3.2.2) and the MADC module is powered on.

5.3.2.5 Battery Current Charger Conversion Register

Register: **ICHGREG**
Page: 0
Address: 17 (10001b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value At Reset	1	1	1	1	1	1	1	1	1	1

Table 5–13. Battery Current Charger Conversion Register Description

DATA BIT	DESCRIPTION
9–0	Output of the 10-bit monitoring ADC for the current of the battery charger. This register is read only.[†]

[†] A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC status register is 0 (see Section 5.3.2.2) and the MADC module is powered on.

5.3.2.6 Backup Battery Voltage Conversion Register

Register: **VBKPREG**
Page: 0
Address: 18 (10010b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value At Reset	1	1	1	1	1	1	1	1	1	1

Table 5–14. Backup Battery Voltage Conversion Register Description

DATA BIT	DESCRIPTION
9–0	Output of the 10-bit monitoring ADC for the voltage of the backup battery. This register is read only.[†]

[†] A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC status register is 0 (see Section 5.3.2.2) and the MADC module is powered on.

5.3.2.7 Analog 1 Voltage Conversion Register

Register: **ADIN1REG**
Page: 0
Address: 19 (10011b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value At Reset	1	1	1	1	1	1	1	1	1	1

Table 5–15. Analog 1 Voltage Conversion Register Description

DATA BIT	DESCRIPTION
9–0	Output of the 10-bit monitoring ADC for the ADIN1 input. This register is read only.[†]

[†] A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC status register is 0 (see Section 5.3.2.2) and the MADC module is powered on.

5.3.2.8 Analog 2 Voltage Conversion Register

Register: **ADIN2REG**
Page: 0
Address: 20 (10100b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value At Reset	1	1	1	1	1	1	1	1	1	1

Table 5–16. Analog 2 Voltage Conversion Register Description

DATA BIT	DESCRIPTION
9–0	Output of the 10-bit monitoring ADC for the ADIN2 input. This register is read only.[†]

[†] A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC status register is 0 (see Section 5.3.2.2) and the MADC module is powered on.

5.3.2.9 Analog 3 Voltage Conversion Register

Register: **ADIN3REG**
Page: 0
Address: 21 (10101b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value At Reset	1	1	1	1	1	1	1	1	1	1

Table 5–17. Analog 3 Voltage Conversion Register Description

DATA BIT	DESCRIPTION
9–0	Output of the 10-bit monitoring ADC for the ADIN3 input. This register is read only.[†]

[†] A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC status register is 0 (see Section 5.3.2.2) and the MADC module is powered on.

5.3.2.10 Analog 4 Voltage Conversion Register

Register: **ADIN4REG**
Page: 0
Address: 22 (10110b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value At Reset	1	1	1	1	1	1	1	1	1	1

Table 5–18. Analog 4 Voltage Conversion Register Description

DATA BIT	DESCRIPTION
9–0	Output of the 10-bit monitoring ADC for the ADIN4 input. This register is read only.[†]

[†] A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC status register is 0 (see Section 5.3.2.2) and the MADC module is powered on.

5.3.2.11 Analog 5 Voltage Conversion Register

Register: **ADIN5REG**
Page: 0
Address: 23 (10111b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value At Reset	1	1	1	1	1	1	1	1	1	1

Table 5–19. Analog 5 Voltage Conversion Register Description

DATA BIT	DESCRIPTION
9–0	Output of the 10-bit monitoring ADC for the ADIN5 input. This register is read only.[†]

[†] A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC status register is 0 (see Section 5.3.2.2) and the MADC module is powered on.

5.3.3   Clock Generator (CKG) Registers

5.3.3.1 Toggle Bits Register 1

The bits in this register are not memory cells. They only set or reset internal latches. Writing 0 to any of these bits has no action. If both the reset toggle and set toggle are written to at the same time, then it is interpreted as a reset toggle.

Register: **TOGBR1**
Page: 0
Address: 4 (00100b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	MADCS	MADCR	AFCS	AFCR	ADACS	ADACR	VDLS	VDLR	VULS	VULR
Access Type	W	W	W	W	W	W	W	W	W	W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–20. Toggle Bits Register 1 Description

DATA BIT	FIELD NAME	DESCRIPTION
9	MADCS	Writing a 1 to this bit sets bit 4 (MADCON) of the power down register to 1 (see Section 5.3.3.3).
8	MADCR	Writing a 1 to this bit clears bit 4 (MADCON) of the power down register to 0 (see Section 5.3.3.3).
7	AFCS	Writing a 1 to this bit sets bit 3 (AFCON) of the power down register to 1 (see Section 5.3.3.3).
6	AFCR	Writing a 1 to this bit clears bit 3 (AFCON) of the power down register to 0 (see Section 5.3.3.3).
5	ADACS	Writing a 1 to this bit sets bit 2 (ADACON) of the power down register to 1 (see Section 5.3.3.3).
4	ADACR	Writing a 1 to this bit clears bit 2 (ADACON) of the power down register to 0 (see Section 5.3.3.3).
3	VDLS	Writing a 1 to this bit sets bit 1 (VDLON) of the power down register to 1 (see Section 5.3.3.3).
2	VDLR	Writing a 1 to this bit clears bit 1 (VDLON) of the power down register to 0 (see Section 5.3.3.3).
1	VULS	Writing a 1 to this bit sets bit 0 (VULON) of the power down register to 1 (see Section 5.3.3.3).
0	VULR	Writing a 1 to this bit clears bit 0 (VULON) of the power down register to 0 (see Section 5.3.3.3).

[†] The VUL and VDL paths share the same digital filter. In order to ensure a perfect initialization of this digital filter, bits 0 (VULON) and 1 (VDLON) of the power down register have to be set on at the same time for at least 125 μs after turning the VRIO regulator from OFF to ON (see Section 5.3.3.3).

5.3.3.2 Toggle Bits Register 2

The bits in this register are not memory cells. They only set or reset internal latches. Writing 0 to any of these bits has no action. If both the reset toggle and set toggle are written to at the same time, then it is interpreted as a reset toggle.

Register: **TOGBR2**
Page: 0
Address: 5 (00101b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	AUDS	AUDR	IAPCTR	IBUFPTR2	IBUFPTR1	ACTS	ACTR	KEEPS	KEEPR
Access Type	W	W	W	W	W	W	W	W	W	W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–21. Toggle Bits Register 2 Description

DATA BIT	FIELD NAME	DESCRIPTION
9	RSVD	Reserved
8	AUDS	Writing a 1 to this bit sets bit 7 (AUDON) of the power down register to 1 (see Section 5.3.3.3).
7	AUDR	Writing a 1 to this bit clears bit 7 (AUDON) of the power down register to 0 (see Section 5.3.3.3).
6	IAPCTR	Writing a 1 to this bit initializes the pointer of the APC RAM.
5	IBUFPTR2	Writing a 1 to this bit initializes the pointer of burst buffer 2.[†]
4	IBUFPTR1	Writing a 1 to this bit initializes the pointer of burst buffer 1.[†]
3	ACTS	Writing a 1 to this bit sets bit 6 (ACTIVMCLK) of the power down register to 1 (see Section 5.3.3.3).
2	ACTR	Writing a 1 to this bit clears bit 6 (ACTIVMCLK) of the power down register to 0 (see Section 5.3.3.3).
1	KEEPS	Writing a 1 to this bit sets bit 5 (KEEPON) of the power down register to 1 (see Section 5.3.3.3).
0	KEEPR	Writing a 1 to this bit clears bit 5 (KEEPON) of the power down register to 0 (see Section 5.3.3.3).

[†] Setting bit 4 (IBUFPTR1) or 5 (IBUFPTR2) to 1 is not permitted during the baseband uplink burst (BULENA signal is set to 1).

5.3.3.3 Power Down Register

Register: **PWDNRG**
Page: 1
Address: 9 (01001b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD		AUDON	ACTIVMCLK	KEEPON	MADCON	AFCON	ADACON	VDLON	VULON
Access Type	R	R	R	R	R	R	R	R	R	R
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–22. Power Down Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–8	RSVD	Reserved
7	AUDON	When this bit is cleared to 0, the audio stereo path is in power-down mode. This bit is set to 1 by bit 8 (AUDS) and reset by bit 7 (AUDR) of toggle bits register 2 (see Section 5.3.3.2).
6	ACTIVMCLK	When this bit is cleared to 0, the MADC, IBIC, and SIMS are in low power mode, using the CK32K clock. This bit is set to 1 by bit 3 (ACTS) and reset by bit 2 (ACTR) of toggle bits register 2 (see Section 5.3.3.2).
5	KEEPON	When this bit is set to 1, the ADC of the MADC block is always ON even after a conversion. When this bit is cleared to 0, the ADC of the MADC block sets itself automatically OFF after a conversion. This bit is set to 1 by bit 1 (KEEPS) and reset by bit 0 (KEEPR) of toggle bits register 2 (see Section 5.3.3.2).
4	MADCON	When this bit is cleared to 0, the MADC is in power-down mode. This bit is set to 1 by bit 9 (MADCS) and reset by bit 8 (MADCR) of toggle bits register 1 (see Section 5.3.3.1).
3	AFCON	When this bit is cleared to 0, the AFC is in power-down mode. This bit is set to 1 by bit 7 (AFCS) and reset by bit 6 (AFCR) of toggle bits register 1 (see Section 5.3.3.1).
2	ADACON	When this bit is cleared to 0, the auxiliary DAC is in power-down mode. This bit is set to 1 by bit 5 (ADACS) and reset by bit 4 (ADACR) of toggle bits register 1 (see Section 5.3.3.1).
1	VDLON	When this bit is cleared to 0, the voiceband downlink path is in power-down mode. This bit is set to 1 by bit 3 (VDLS) and reset by bit 2 (VDLR) of toggle bits register 1 (see Section 5.3.3.1).
0	VULON	When this bit is cleared to 0, the voiceband uplink path is in power-down mode. This bit is set to 1 by bit 1 (VULS) and reset by bit 0 (VULR) of toggle bits register 1 (see Section 5.3.3.1).

5.3.3.4 Test Access Port Control Register

Register: **TAPCTRL**
Page: 1
Address: 19 (10011b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD									WRTEN
Access Type	–	–	–	–	–	–	–	–	–	W
Value At Reset	–	–	–	–	–	–	–	–	–	0

Table 5–23. Test Access Port Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–1	RSVD	Reserved
0	WRTEN	If this bit is set to 1, then the test mode is selected by writing in the test access port instruction register (see Section 5.3.3.5). If this bit is cleared to 0, then the test mode is selected by loading the shift register (use of TMS, TDI).

5.3.3.5 Test Access Port Instruction Register

Register: **TAPREG**
Page: 1
Address: 20 (10100b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	VER3	VER2	VER1	VER0	IR5	IR4	IR3	IR2	IR1	IR0
Access Type	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0/1	0/1	0/1	0/1	0	0	0	0	0	1

Table 5–24. Test Access Port Instruction Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–6	VER(3:0)	Version number (version part of ABB IDCODE)
5–0	IR(5:0)	JTAG instruction register data

5.3.4   Automatic Frequency Control (AFC) Registers

5.3.4.1 Automatic Frequency Control Register 1

Register: **AUXAFC1**
Page: 0
Address: 7 (00111b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–25. Automatic Frequency Control Register 1 Description

DATA BIT	DESCRIPTION
9–0	LSB input of the 13-bit AFC DAC in twos complement

5.3.4.2 Automatic Frequency Control Register 2

Register: **AUXAFC2**
Page: 0
Address: 8 (01000b)
Read/Write: 1/0

Data Bit	–	–	–	–	–	–	–	12	11	10
Access Type	–	–	–	–	–	–	–	R/W	R/W	R/W
Value At Reset	–	–	–	–	–	–	–	0	0	0

Table 5–26. Automatic Frequency Control Register 2 Description

DATA BIT	DESCRIPTION
12–10	MSB input of the 13-bit AFC DAC in twos complement. The AFC value is loaded after successive write of the AFC–MSB and AFC–LSB.

5.3.4.3 AFC Working Frequency Register

Register: **AFCCTLADD**
Page: 1
Address: 21 (10101b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD							AFCBYP	AFCCK(1:0)	
Access Type	–	–	–	–	–	–	–	R/W	R/W	R/W
Value At Reset	–	–	–	–	–	–	–	0	0	0

Table 5–27. AFC Working Frequency Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–3	RSVD	Reserved
2	AFCBYP	Disable write access in the AFC digital output register by the Σ-Δ modulator. Enable write access in the AFC digital output register by the USP or BSP access.
1–0	AFCCK(1:0)	<u>AFCCK1</u> <u>AFCCK0</u> <u>AFC Clock Frequency</u> 0 0 CKIN 0 1 CKIN/2 1 0 CKIN/4 1 1 CKIN/8 Where: CKIN = CK13M/3 = 4.32 MHz

5.3.4.4 AFC Digital Output Register

Register: **AFCOUT**
Page: 1
Address: 22 (10110b)
Read/Write: 1/0

Data Bit	–	–	7	6	5	4	3	2	1	0
Name	RSVD		DOUT(7:0)							
Access Type	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	–	–	0	0	0	0	0	0	0	0

Table 5–28. AFC Digital Output Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–8	RSVD	Reserved
7–0	DOUT(7:0)	The serial-to-parallel output of the AFC modulator (for test purposes)

5.3.5 Automatic Power Control (APC) Registers

In all cases, the values of DELU(9:0) and DELD(9:0) must be set to avoid any ramp-up or ramp-down start delays after the BULENA falling edge.

5.3.5.1 APC Ramp Delay 1 Register

Register: **APCDEL1**
Page: 0
Address: 2 (00010b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name			DELD(4:0)					DELU(4:0)		
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–29. APC Ramp Delay 1 Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–5	DELD(4:0)	LSB part of ramp-down start delay relative to the falling edge of BENA. See Section 4.8 for a description of the adjustment delay.
4–0	DELU(4:0)	LSB part of ramp-up start delay relative to the rising edge of BENA. See Section 4.8 for a description of the adjustment delay.

5.3.5.2 APC Ramp Delay 2 Register

Register: **APCDEL2**
Page: 1
Address: 26 (11010b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name			DELD(9:5)					DELU(9:5)		
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–30. APC Ramp Delay 2 Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–5	DELD(9:5)	MSB ramp-down start delay relative to the falling edge of BULENA. See Section 4.8, *Automatic Power Control* for a description of the adjustment delay.
4–0	DELU(9:5)	MSB ramp-up start delay relative to the rising edge of BULENA. See Section 4.8, *Automatic Power Control* for a description of the adjustment delay.

5.3.5.3 Automatic Power Control Register

Register: **AUXAPC**
Page: 0
Address: 9 (01001b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–31. Automatic Power Control Register Description

DATA BIT	DESCRIPTION
9–0	10-bit APC power level

5.3.5.4 Automatic Power Control RAM Register

The contents of the APC RAM register are the coefficients of the ramp-up and ramp-down shaping filters.

Register: **APCRAM**
Page: 0
Address: 10 (01010b)
Write: 0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name			DWN–0 (5-bit)					UP–0 (5-bit)		
			DWN–1 (5-bit)					UP–1 (5-bit)		
			…					…		
			DWN–14 (5-bit)					UP–14 (5-bit)		
			DWN–15 (5-bit)					UP–15 (5-bit)		
Access Type	W	W	W	W	W	W	W	W	W	W
Value At Reset	0	0	0	0	0	0	0	0	0	0

5.3.5.5 DAC Input Offset and Gain Register

Register: **APCOFF**
Page: 0
Address: 11 (01011b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name		RSVD		SEL256128				Bits (5:0)		
Access Type	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–32. Offset DAC Input Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–7	RSVD	Reserved.
6	SEL256128	0 = Selects normal slope for ramp-up and ramp-down 1 = Selects 2X slope for ramp-up and ramp-down
5–0	Bits (5:0)	Input of the 6-bit offset DAC

5.3.5.6 APC Output Register

Register: **APCOUT**
Page: 1
Address: 12 (01100b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name					APC(9:0)					
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–33. APC Output Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–0	APC(9:0)	Value of data to APC DAC 10

5.3.6 Auxiliary DAC Control Register

Register: **AUXDAC**
Page: 0
Address: 12 (01100b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–34. Auxiliary DAC Control Register Description

DATA BIT	DESCRIPTION
9–0	Input of the 10-bit ADAC

5.3.7 Battery Charger (BCI) Registers

Controlling the operation of the BCI requires the exchange of two types of programming signals between the BCI itself and the rest of the system, that is, the power control state machine contained in the VRPCD block of the TLW3016 device, and the microcontroller contained in the DBB device.

1. Some programming signals are sent or received by the microcontroller exclusively, when it is fully awake; the path for these signals includes the microcontroller interface registers only.

2. Other programming signals are also sent or received by the power control state machine located in the VRPCD block, before the microcontroller gets awakened; the path for these signals includes a multiplexing operation between the microcontroller interface registers (VRIO supply domain) and the power control state machine. A signal driving the direction of the multiplex decides which device, the power control state machine or the microcontroller, sends or receives programming data to or from the BCI.

5.3.7.1 Main Battery Charging Voltage Register

Register: **CHGVREG**
Page: 0
Address: 25 (11001b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	CHGV(9:0)									
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–35. Main Battery Charging Voltage Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–0	CHGV(9:0)	10-bit DAC register for setting a voltage for main battery charging.

5.3.7.2 Main Battery Charging Current Register

Register: **CHGIREG**
Page: 0
Address: 14 (01110b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	PROCTL(1:0)		CHGI(7:0)							
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–36. Main Battery Charging Current Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–8	PROCTL(1:0)	BCI comparator configuration: 00 = Comparator power down, with bit 9 (PROEN) of the battery control 2 register equal 0 (see Section 5.3.7.4) 01 = Battery temperature sensing, with bit 9 (PROEN) of the battery control 2 register equal 1 (see Section 5.3.7.4) 10 = End-of-charge current sensing, with bit 9 (PROEN) of the battery control 2 register equal 1 (see Section 5.3.7.4) 11 = Battery voltage sensing, with bit 9 (PROEN) of the battery control 2 register equal 1 (see Section 5.3.7.4)
7–0	CHGI(7:0)	8-bit DAC register for setting a current for main battery charging.

5.3.7.3 Battery Control 1 Register

Register: **BCICTL1**
Page: 0
Address: 28 (11100b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	OFFEN	THENSA	TYPEN	THEN	THSENS(2:0)			OFFSN(1:0)		MESBAT†
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

† Disable during SLEEP mode.

Table 5–37. Battery Control 1 Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	OFFEN	Enables offset settings for I-to-V conversion.
8	THENSA	Selects ADIN2 (THENSA = 0) or ADIN3 (THENSA = 1) for main battery temperature sensing.
7	TYPEN	Enables bias current for main battery type reading.
6	THEN	Enables bias current for main battery temperature sensing.
5–3	THSENS(2:0)	Sets eight possible values for thermal sensor bias current.
2–1	OFFSN(1:0)	Sets four possible values for I-to-V conversion offset (CGAIN4 = 0): 00 = 100 mV 10 = 200 mV 01 = 300 mV 11 = 400 mV
0	MESBAT	Connects a resistive divider to the main battery.

5.3.7.4 Battery Control 2 Register

Register: **BCICTL2**
Page: 0
Address: 29 (11101b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	PROEN	RSVD	PREOFF	CGAIN4	LEDC	CHDISPA	CLIB	CHBPASSPA	CHIV	CHEN
Access Type	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W/U [†]
Value At Reset	0	0	0	0	0	0	0	0	0	0

[†] Value may be reset by a BCI watchdog overflow or the BCI comparator trigger.

Table 5–38. Battery Control 2 Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	PROEN	When this bit is set to 1, it enables the overtemperature, overvoltage, or end-of-charge current comparator.
8	RSVD	Reserved.
7	PREOFF	When this bit is set to 1, it disables the main battery precharge.
6	CGAIN4	Reduces the gain of the I-to-V converter from 10 (CGAIN4 = 0) to 4 (CGAIN4 = 1).
5	LEDC	Switch control of the LED C driver, used to indicate a battery precharge.
4	CHDISPA	When this bit is set to 1, it disables the external charge transistor, setting the ICTL terminal to VCHG.
3	CLIB	When this bit is set to 1, it allows a zero calibration routine to the I-to-V converter (must be used when bit 4 (CHDISPA) equals 1)
2	CHBPASSPA	When this bit is set to 1, it turns the external charge transistor on (closed switch), setting the ICTL terminal to GND.
1	CHIV	Selects constant current (CHIV = 1) or constant voltage charging mode (CHIV = 0).
0	CHEN	Enables the charger.

5.3.7.5 Battery Charging Configuration Register

Register: **BCICONF**
Page: 1
Address: 13 (01101b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	BATSTS	BBSEL(1:0)		MESBB†	BBCHGEN	VBATCHKEN	RRTC(1:0)		RDBB(1:0)	
Access Type	R/U ‡	R/W	R/W	R/W	R/W	R/W/U ‡	R/W	R/W	R/W	R/W
Value At Reset	1	Keep Value	Keep value	0	Keep value	Keep value	Keep value	Keep value	Keep value	Keep value
Value At Por	1	0	0	0	0	0	VLRTC	VLRTC0	VLRTC	VLRTC0

† Disable during SLEEP mode.
‡ Value may be updated by the VRPC STM.

Table 5–39. Battery Charging Configuration Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	BATSTS	Status of main battery presence check (BATSTS = 0: no battery detected) with VBATCHKEN = 1.
8–7	BBSEL(1:0)	Select the end of backup battery charging voltage. 00 = VBBCHGEND + 0 mV 01 = VBBCHGEND + 100 mV 10 = VBBCHGEND – 100 mV 11 = VBACKUP = VBAT
6	MESBB	Connect the resistor bridge to the backup battery
5	BBCHGEN	Enable backup battery charger.
4	VBATCHKEN	Enable main battery presence check.
3–2	RRTC(1:0)	Configure VRRTC output voltage 01 = 1.3 V 00 = 1.5 V 10 = 1.8 V
1–0	RDBB(1:0)	Configure VRDBB output voltage 01 = 1.3 V 00 = 1.5 V 10 = 1.8 V

5.3.7.6 Battery Charger Watchdog Register

Register: **BCIWDOG**
Page: 1
Address: 24 (11000b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	WOVF	WEN	KEY(7:0)							
Access Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–40. Battery Charging Configuration Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	WOVF	When this bit is set to 1, it enables the watchdog overflow.
8	WEN	When this bit is set to 1, it enables and starts the watchdog timer.
7–0	KEY(7:0)	Key code of the watchdog timer, the following key values must be written before their corresponding delay is reached: 10101010 = 1 s 01010101 = 2 s 11011011 = 4 s 10111101 = 8 s

5.3.8 Interrupt And Bus Control Registers (IBIC)

5.3.8.1 Interrupt Mask Register

Register: **ITMASK**
Page: 0
Address: 26 (11010b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD			BCICOMP_IT_MSK	ADCEND_IT_MSK	USB_IT_MSK	CHRGER_IT_MSK	PUSHOFF_IT_MSK	REMOTE_IT_MSK	REMOTE2_IT_MSK
Access Type	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–41. Interrupt Mask Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–7	RSVD	Reserved.
6	BCICOMP_IT_MSK	If this bit is set to 1, the BCI end-of-charge, overvoltage or overtemperature interrupt is not generated.
5	ADCEND_IT_MSK	If this bit is set to 1, the ADC end-of-conversion interrupt is not generated.
4	USB_IT_MSK	If this bit is set to 1, the USB plug IN or OUT interrupt is not generated.
3	CHRGER_IT_MSK	If this bit is set to 1, the charger plug IN or OUT interrupt is not generated.
2	PUSHOFF_IT_MSK	If this bit is set to 1, the push button from ON to OFF interrupt is not generated.
1	REMOTE_IT_MSK	If this bit is set to 1, the remote power from ON to OFF interrupt is not generated.
0	REMOTE2_IT_MSK	If this bit is set to 1, the remote power 2 from ON to OFF interrupt is not generated.

5.3.8.2 Interrupt Status Register

Register: **ITSTATREG** †
Pages: 0 and 1
Address: 27 (11011b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD			BCICOMP	ADCEND	USB	CHRGER	PUSHOFF	REMOTE	REMOTE2
Access Type	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	–	–	–	0	0	0	0	0	0	0

† Status reset of a nonmasked interrupt is performed through a read or a write access of the interrupt status register. Status bit reset of a masked interrupt (corresponding mask bit is set to 1 in the interrupt mask register) is performed only through a write access of the interrupt status register and through a read or write access if the event related to this interrupt is arising before a falling edge of the INT2 terminal.

Table 5–42. Interrupt Status Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–7	RSVD	Reserved
6	BCICOMP	The BCI end-of-charge, overvoltage, or overtemperature interrupt bit
5	ADCEND	ADC end-of-conversion interrupt bit
4	USB	USB plug IN or OUT interrupt bit
3	CHRGER	Charger plug IN or OUT interrupt bit
2	PUSHOFF	Push button (terminal PWON) from ON to OFF interrupt bit
1	REMOTE	Remote power (terminal RPWON) from ON to OFF interrupt bit
0	REMOTE2	Remote power (terminal RPWON2) from ON to OFF interrupt bit

5.3.8.3 Page Select Register

This register is a read/write register. It can be accessed through both the USP and BSP serial interfaces. USP access to this register does not affect the current page selected by the BSP. The BSP access to this register does not affect the current page selected by the USP. Therefore, the users' software must know the last page that was selected by the serial interface that is being used. Furthermore, if the last page selected by the BSP/USP differs from the last page selected by the USP/BSP, there is no need to rewrite to the page register as the device knows which serial port is accessing registers and uses the current page setting for that port.

Register: **PAGEREG**
Pages: 0 and 1
Address: 1 (00001b)
Write: 0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD						BSPP1	BSPP0	UCP1	UCP0
Access Type	–	–	–	–	–	–	R/W	R/W	R/W	R/W
Value At Reset	–	–	–	–	–	–	0	1	0	1

Table 5–43. Page Select Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–4	RSVD	Reserved
3	BSPP1	Writing a 1 sets page 1 for BSP access. Only accessible by the BSP.
2	BSPP0	Writing a 1 sets page 0 for BSP access. Only accessible by the BSP.
1	UCP1	Writing a 1 sets page 1 for USP access. Only accessible by the USP.
0	UCP0	Writing a 1 sets page 0 for USP access. Only accessible by the USP.

5.3.9 Baseband Codec (BBC) Registers

5.3.9.1 Baseband Uplink I Offset Register

Write access to this register is disabled during offset calibration (BULCAL high).

Register: **BULIOFF**
Page: 1
Address: 2 (00010b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	ULIOFF(8:0)								
Access Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	1	1	1	1	1	1	1	1

Table 5–44. Baseband Uplink I Offset Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	RSVD	Reserved
8–0	ULIOFF(8:0)	I channel offset value

5.3.9.2 Baseband Uplink Q Offset Register

Write access to this register is disabled during offset calibration (BULCAL high).

Register: **BULQOFF**
Page: 1
Address: 3 (00011b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	ULQOFF(8:0)								
Access Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	1	1	1	1	1	1	1	1

Table 5–45. Baseband Uplink Q Offset Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	RSVD	Reserved
8–0	ULQOFF(8:0)	Q channel offset value

5.3.9.3 Baseband Uplink I DAC Register

Register: **BULIDAC**
Page: 1
Address: 5 (00101b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	ULIDAC(9:0)									
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	1	1	1	1	1	1	1	1	1

Table 5–46. Baseband Uplink I DAC Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–0	ULIDAC(9:0)	Data applied to the I channel DAC. Write is disabled during modulation.

5.3.9.4 Baseband Uplink Q DAC Register

Register: **BULQDAC**
Page: 1
Address: 4 (00100b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name										
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	ULQDAC(9:0)									
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–47. Baseband Uplink Q DAC Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–0	ULQDAC(9:0)	Data applied to the Q channel DAC. Write is disabled during modulation.

5.3.9.5 Baseband Uplink Absolute Gain Calibration Register

Register: **BULGCAL**
Page: 1
Address: 14 (01110b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	QAG(3:0)				RSVD	IAG(3:0)			
Access Type	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–48. Baseband Uplink Absolute Gain Calibration Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	RSVD	Reserved
8–5	QAG(3:0)	Absolute gain calibration for the Q DAC QAG(3:0) — Relative Gain — QAG(3:0) — Relative Gain 0000 — 0 db — 0000 — 0 db 0001 — 0.27 db — 1111 — −0.27 db 0010 — 0.53 db — 1110 — −0.56 db 0011 — 0.78 db — 1101 — −0.85 db 0100 — 1.02 db — 1100 — −1.16 db 0101 — 1.26 db — 1011 — −1.48 db 0110 — 1.49 db — 1010 — −1.80 db
4	RSVD	Reserved
3–0	IAG(3:0)	Absolute gain calibration for the I DAC IAG(3:0) — Relative Gain — IAG(3:0) — Relative Gain 0000 — 0 db — 0000 — 0 db 0001 — 0.27 db — 1111 — −0.27 db 0010 — 0.53 db — 1110 — −0.56 db 0011 — 0.78 db — 1101 — −0.85 db 0100 — 1.02 db — 1100 — −1.16 db 0101 — 1.26 db — 1011 — −1.48 db 0110 — 1.49 db — 1010 — −1.80 db

5.3.9.6 Baseband Uplink Data Buffer 1 Register

Register: **BULDATA1**
Page: 0 (16 words)
Address: 3 (00011b)
Write: 0

Data Bit	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8	bit 9
	bit 10	bit 11	bit 12	bit 13	bit 14	bit 15	bit 16	bit 17	bit 18	bit 19
	bit 20	bit 21	bit 22	bit 23	bit 24	bit 25	bit 26	bit 27	bit 28	bit 29
	bit 30	bit 31	bit 32	bit 33	bit 34	bit 35	bit 36	bit 37	bit 38	bit 39
	bit 40	bit 41	bit 42	bit 43	bit 44	bit 45	bit 46	bit 47	bit 48	bit 49
	bit 50	bit 51	bit 52	bit 53	bit 54	bit 55	bit 56	bit 57	bit 58	bit 59
	bit 60	bit 61	bit 62	bit 63	bit 64	bit 65	bit 66	bit 67	bit 68	bit 69
	bit 70	bit 71	bit 72	bit 73	bit 74	bit 75	bit 76	bit 77	bit 78	bit 79
	bit 80	bit 81	bit 82	bit 83	bit 84	bit 85	bit 86	bit 87	bit 88	bit 89
	bit 90	bit 91	bit 92	bit 93	bit 94	bit 95	bit 96	bit 97	bit 98	bit 99
	bit 100	bit 101	bit 102	bit 103	bit 104	bit 105	bit 106	bit 107	bit 108	bit 109
	bit 110	bit 111	bit 112	bit 113	bit 114	bit 115	bit 116	bit 117	bit 118	bit 119
	bit 120	bit 121	bit 122	bit 123	bit 124	bit 125	bit 126	bit 127	bit 128	bit 129
	bit 130	bit 131	bit 132	bit 133	bit 134	bit 135	bit 136	bit 137	bit 138	bit 139
	bit 140	bit 141	bit 142	bit 143	bit 144	bit 145	bit 146	bit 147	bit 148	bit 149
	bit 150	bit 151	bit 152	bit 153	bit 154	bit 155	bit 156	bit 157	bit 158	bit 159
Access Type	W	W	W	W	W	W	W	W	W	W

Table 5–49. Baseband Uplink Data Buffer 1 Register Description

DATA BIT	DESCRIPTION
0:3	4 guard bits
4:6	3 tail bits
7:64	58 data bits
65:90	26 training sequence bits
91:148	58 data bits
149:151	3 tail bits
152:159	8 guard bits

NOTE 1:   Bit 0 is transmitted first. At reset and after each transmission the burst buffer is not reinitialized.

5.3.9.7 Baseband Uplink Data Buffer 2 Register

Register: **BULDATA2**
Page: 0 (16 words)
Address: 3 (00011b)
Write: 0

Data Bit										
	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8	bit 9
	bit 10	bit 11	bit 12	bit 13	bit 14	bit 15	bit 16	bit 17	bit 18	bit 19
	bit 20	bit 21	bit 22	bit 23	bit 24	bit 25	bit 26	bit 27	bit 28	bit 29
	bit 30	bit 31	bit 32	bit 33	bit 34	bit 35	bit 36	bit 37	bit 38	bit 39
	bit 40	bit 41	bit 42	bit 43	bit 44	bit 45	bit 46	bit 47	bit 48	bit 49
	bit 50	bit 51	bit 52	bit 53	bit 54	bit 55	bit 56	bit 57	bit 58	bit 59
	bit 60	bit 61	bit 62	bit 63	bit 64	bit 65	bit 66	bit 67	bit 68	bit 69
	bit 70	bit 71	bit 72	bit 73	bit 74	bit 75	bit 76	bit 77	bit 78	bit 79
	bit 80	bit 81	bit 82	bit 83	bit 84	bit 85	bit 86	bit 87	bit 88	bit 89
	bit 90	bit 91	bit 92	bit 93	bit 94	bit 95	bit 96	bit 97	bit 98	bit 99
	bit 100	bit 101	bit 102	bit 103	bit 104	bit 105	bit 106	bit 107	bit 108	bit 109
	bit 110	bit 111	bit 112	bit 113	bit 114	bit 115	bit 116	bit 117	bit 118	bit 119
	bit 120	bit 121	bit 122	bit 123	bit 124	bit 125	bit 126	bit 127	bit 128	bit 129
	bit 130	bit 131	bit 132	bit 133	bit 134	bit 135	bit 136	bit 137	bit 138	bit 139
	bit 140	bit 141	bit 142	bit 143	bit 144	bit 145	bit 146	bit 147	bit 148	bit 149
	bit 150	bit 151	bit 152	bit 153	bit 154	bit 155	bit 156	bit 157	bit 158	bit 159
Access Type	W	W	W	W	W	W	W	W	W	W

Table 5–50. Baseband Uplink Data Buffer 2 Register Description

DATA BIT	DESCRIPTION
0:3	4 guard bits
4:6	3 tail bits
7:64	58 data bits
65:90	26 training sequence bits
91:148	58 data bits
149:151	3 tail bits
152:159	8 guard bits

NOTE 2:   Bit 0 is transmitted first. At reset and after each transmission the burst buffer is not reinitialized.

5.3.9.8 Baseband Codec Control Register

Register: **BBCTRL**
Page: 1
Address: 6 (00110b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	EXTCAL	OUTLEV(2:0)			MSLOT	RSVD	BALOOP	SELVMID(2:0)		
Access Type	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–51. Baseband Codec Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	EXTCAL	Downlink auto calibration mode: 0 = Auto calibration 1 = External calibration
8–6	OUTLEV(2:0)	Selects the value of the baseband output level (V_{DD}): 000 = 2 x VREF 001 = (16/15) x VREF 010 = (22/15) x VREF 011 = (8/15) x VREF 10x = (18/15) x VREF 11x = (20/15) x VREF
5	MSLOT	When this bit is cleared to 0, it enables single-slot modulation (only burst buffer 1 is used). When this bit is set to 1, it enables multislot mode modulation (burst buffer 0 and burst buffer 1 are used alternately).
4	RSVD	Reserved
3	BALOOP	When this bit is set to 1, internal analog loop of I/Q uplink terminals to the I/Q downlink.
2–0	SELVMID(2:0)	Selects the value of output common mode of baseband uplink. 000 = VRABB/2 001 = 1.35 V 010 = 1.45 V 011 = 1.18 V 1xx = 1.25 V

5.3.9.9 Baseband Codec Configuration Register

Register: **BBCFG**
Pages: 1
Address: 28 (11000b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD		SKIPCT(4:0)					BBMODE(1:0)		OFFSEN
Access Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	1	0	0	0	1	0	1

Table 5–52. Baseband Configuration Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–8	RSVD	Reserved
7–3	SKIPCT(4:0)	Number of output samples skipped (not sent to DSP via BSP) once digital baseband downlink is on (BDLENA = 1)
2–1	BBMODE(1:0)	Baseband downlink digital filter reset control: 00 = Digital filter reset is applied at the falling edge of BDLCAL 10 = Digital filter reset is not applied at the falling edge of BDLCAL
0	OFFSEN	When this bit is set to 1, the baseband downlink dc offset calibration result is applied and the offset register is subtracted from the BDL digital filter output. When this bit is cleared to 0, the baseband downlink dc offset calibration result is not applied.

5.3.10 Voiceband Codec Registers (VBC)

5.3.10.1 Voiceband Control Register 1

Register: **VBCTRL1**
Page: 1
Address: 8 (01000b)
Read/Write   1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	VFBYP	VBDFAUXG	VSYNC	VCLKMODE	VALOOP	MICBIAS	VULSWITCH	RSVD		
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–53. Voiceband Control Register 1 Description

DATA BIT	FIELD NAME	DESCRIPTION
9	VFBYP	When this bit is set to 1, the voice downlink path filter is bypassed.
8	VBDFAUXG	When this bit is cleared to 0, the gain of the AUXIN amplifier is 4.6 dB. When this bit is set to 1, the gain of the AUXIN amplifier is 28.2 dB.
7	VSYNC	When this bit is set to 1, the digital modulator, the digital voice serial port, and the digital filter are reset. At the reset using VDR, the filter sets VSYNC to 0.
6	VCLKMODE	When this bit is cleared to 0, this bit allows selection of the VCK in burst mode. When this bit is set to 1, this bit allows selection of the VCK in continuous mode.
5	VALOOP	When this bit is set to 1, the internal analog loop of the output samples is sent to the input of the audio ADC. To avoid saturation of the analog path in this mode you must set: PGA downlink = –6 dB PGA uplink = 0 dB Volume = 0 dB SideTone = MUTE
4	MICBIAS	When this bit is cleared to 0, the analog bias for the electric microphone and external decoupling is driven to 2 V. When this bit is set to 1, the analog bias is driven to 2.5 V.
3	VULSWITCH	Enables the auxiliary input if this bit is cleared to 0. Enables MICIN if this bit and bit 0 (VULON) of the power down register (see Section 5.3.3.3) are set to 1.
2–0	RSVD	Reserved

5.3.10.2 Voiceband Control Register 2

Register: **VBCTRL2**
Page: 1
Address: 11 (01011b)
Read/Write 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	VMIDSEL	VMIDFBYP	WBA†	HSDIF	HSOVMID	SPKG	MICBIASEL	RSVD	HSMICSEL
Access Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

† The value of this control bit must not be changed when bit 0 (VULON) or bit 1 (VDLON) of the power down register equals 1 (see Section 5.3.3.3).

Table 5–54. Voiceband Control Register 2 Description

DATA BIT	FIELD NAME	DESCRIPTION
9	RSVD	Reserved
8	VMIDSEL	When this bit is set to 1, audio output VMID is set to 1.5 V.
7	VMIDFBYP	When this bit is cleared to 0, the AUVMID filter is bypassed.
6	WBA	Voice speech path: 1 = Operating with wide band (8-kHz bandwidth) 0 = Narrow band (4-kHz bandwidth)
5	HSDIF	When this bit is set to 1, HSMICP and AUXI terminals are connected to the differential microphone amplifier.
4	HSOVMID	When this bit is set to 1, HSOVMID is active if bit 1 (VDLON) or bit 7 (AUDON) of the power down register equals 1 (see Section 5.3.3.3). When this bit is cleared to 0, HSOVMID is powered down.
3	SPKG	When this bit is set to 1, SPKAMP gain is 8.5 dB. When this bit is cleared to 0, SPKAMP gain is 2.5 dB.
2	MICBIASEL	When this bit is set to 1, HSMICBIAS is active. When this bit is cleared to 0, MICBIAS is active.
1	RSVD	Reserved
0	HSMICSEL	When this bit is set to 1, the HSMIC input is used. When this bit is cleared to 0, the AUXI input is used (these inputs are multiplexed in the ABB device).

5.3.10.3 Voiceband Pop Reduction Register

Register: **VBPOP**
Page: 1
Address: 10 (01010b)
Read/Write   1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	AUXFBYP	RSVD	AUXAUTO	AUXFDIS	EARAUTO	EARCHG	EARDIS	HSOAUTO	HSOCHG	HSODIS
Access Type	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–55. Voiceband Pop Reduction Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	AUXFBYP	Enables the charge of the external capacitor (up to VRABB/2) when bit 7 (VMIDFBYP) of the voiceband control register 2 equals 1 (see Section 5.3.10.2). This bit has no effect when bit 1 (VDLON) of the power down register is cleared to 0 (see Section 5.3.3.3).
8	RSVD	Reserved.
7,5,2	xAUTO[†]	1 = means that xCHG or AUXFBYP functionality runs in AUTOMATIC mode 0 = in NORMAL mode <u>AUTOMATIC Mode</u>: The xCHG or AUXFBYP (with VMIDFBYP = 1) control bit is set automatically to 1 when VDLON rise. This bit is cleared automatically to 0 when the corresponding audio output is set on. <u>NORMAL Mode</u>: The xCHG or AUXFBYP control bit bit has no effect when the corresponding audio output is set on.
4,1	xCHG[†]	Enables the charge of the external capacitor (up to VRABB/2) This bit has no effect when bit 1 (VDLON) of the power down register is cleared to 0 (see Section 5.3.3.3) or when AUTOMATIC MODE is running.

6,3,0	xDIS[†]	Enables the discharge of the external capacitor
		
		This bit has no effect when xCHG or bit 9 (AUXFBYP) is set to 1.
		    or when bit 1 (VDLON) of the power down register is cleared to 0 (see Section 5.3.3.3)
		    or when corresponding audio output is set on

[†] x is AUX for AUXO outputs, EAR for earphone EAR outputs or HSOL and HSOR for head set outputs.

5.3.10.4 Voiceband Uplink Control Register

Register: **VBUCTRL**
Page: 1
Address: 7 (00111b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	DXEN	VDLST(3:0)				VULPG(4:0)				
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–56. Voiceband Uplink Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	DXEN	When this bit is set to 1, the VDX signal is in mute mode. If this bit is cleared, the VDX signal is in normal mode.
8–5	VDSLT(3:0)	Side tone levels. VDSLT3 VDSLT2 VDSLT1 VDSLT0 Relative Gain 1 1 0 1 −23 dB 1 1 0 0 −20 dB 0 1 1 0 −17 dB 0 0 1 0 −14 dB 0 1 1 1 −11 dB 0 0 1 1 −8 dB 0 0 0 0 −5 dB 0 1 0 0 −2 dB 0 0 0 1 1 dB 0 1 0 1 1 dB 1 0 0 0 Mute 1 0 0 1 Mute 1 0 1 0 Mute 1 0 1 1 Mute 1 1 1 0 Mute 1 1 1 1 Mute
4–0	VULPG(4:0)	Voice uplink digital programmable gain (−12 dB to +12 dB in 1–dB steps). VULPG4 VULPG3 VULPG2 VULPG1 VULPG0 Relative Gain 1 0 0 0 0 −12 dB 1 0 1 1 1 −11 dB 1 1 0 0 0 −10 dB 1 1 0 0 1 −9 dB 1 1 0 1 0 −8 dB 1 1 0 1 1 −7 dB 0 0 0 0 0 −6 dB 0 0 0 0 1 −5 dB 0 0 0 1 0 −4 dB 0 0 0 1 1 −3 dB 0 0 1 0 0 −2 dB 0 0 1 0 1 −1 dB 0 0 1 1 0 0 dB 0 0 1 1 1 1 dB 0 1 0 0 0 2 dB 0 1 0 0 1 3 dB 0 1 0 1 0 4 dB 0 1 0 1 1 5 dB 0 1 1 0 0 6 dB 1 0 0 0 1 7 dB 1 0 0 1 0 8 dB 1 0 0 1 1 9 dB 1 0 1 0 0 10 dB 1 0 1 0 1 11 dB 1 0 1 1 0 12 dB

5.3.10.5 Voiceband Downlink Control Register

Register: **VBDCTRL**
Page: 0
Address: 6 (00110b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD			VOLCTL(2:0)			VDLPG(3:0)			
Access Type	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–57. Voiceband Downlink Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–7	RSVD	Reserved
6–4	VOLCTL(2–0)	Volume control VOLCTL2 VOLCTL1 VOLCTL0 Relative Gain 0 1 0 0 dB 1 1 0 −6 dB 0 0 0 −12 dB 1 0 0 −18 dB 0 1 1 −24 dB 1 0 1 Mute 0 0 1 Mute 1 1 1 Mute
3–0	VDLPG(3–0)	Voice downlink digital programmable gain VDLPG3 VDLPG2 VDLPG1 VDLPG0 Relative Gain 0 0 0 0 −6 dB 0 0 0 1 −5 dB 0 0 1 0 −4 dB 0 0 1 1 −3 dB 0 1 0 0 −2 dB 0 1 0 1 −1 dB 0 1 1 0 0 dB 0 1 1 1 1 dB 1 0 0 0 2 dB 1 0 0 1 3 dB 1 0 1 0 4 dB 1 0 1 1 5 dB 1 1 0 0 6 dB 1 1 0 1 −6 dB 1 1 1 0 −6 dB 1 1 1 1 −6 dB

5.3.10.6 Audio Control Register

Register: **VAUDCTRL**
Page: 1
Address: 15 (01111b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	VSPCK	AUGA †	SRW2 †	SRW1 †	SRW0 †	VULBST	HPFBYP	MONOL †	MONOR †	RSVD
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Value At Reset	0	0	0	0	0	0	0	0	0	0

† The value of this control bit must not be changed when bit 7 (AUDON) of the power down register equals 1 (see Section 5.3.3.3).

Table 5–58. Audio Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	VSPCK	VSPCK = 0: Set the VCK frequency to 500 kHz VSPCK = 1, WBA = 0: Set the VCK frequency to 1 MHz VSPCK = 1, WBA = 1: Set the VCK frequency to 2 MHz
8	AUGA	Audio stereo left and right channel volume control: 0 = Relative gain of 0 dB 1 = Relative gain of 6 dB
7–5	SRW(2–0)	Stereo audio sampling rate frequency SRW2 SRW1 SRW0 Sampling frequency (AUCK frequency = 40*FS) 0 0 0 48 kHz 0 1 0 44.1 kHz 0 1 1 32 kHz 1 0 0 22.05 kHz 1 0 1 16 kHz 1 1 0 11.025 kHz 1 1 1 8 kHz others Not used
4	VULBST	When this bit is set to 1, the drive capability of voice uplink input amplifier stages is increased.
3	HPFBYP	Speech digital high pass filter bypass (HPFBYP = 1)
2	MONOL	Converts stereo signal to mono signal and transmits on left channel (MONOL = 1)
1	MONOR	Converts stereo signal to mono signal and transmits on right channel (MONOR = 1)
0	RSVD	Reserved

5.3.10.7 Audio Outputs Control Register

Register: **VAUOCTRL**
Page: 1
Address: 17 (10001b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	EAR(1:0)		AUX(1:0)		SPK(1:0)		HSOL(1:0)		HSOR(1:0)	
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

Table 5–59. Audio Outputs Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9–8	EAR(1–0)	EARAMP audio output control: EAR 1 / EAR 0 / Output Signal 0 / 0 / None (power down) 0 / 1 / Voice speech 1 / 0 / Audio mono 1 / 1 / Voice speech + audio mono
7–6	AUX(1–0)	AUXAMP audio output control: AUX1 / AUX0 / Output Signal 0 / 0 / None (power down) 0 / 1 / Voice speech 1 / 0 / Audio mono 1 / 1 / Voice speech + audio mono
5–4	SPK(1–0)	SPKAMP audio output control: SPK 1 / SPK 0 / Output Signal 0 / 0 / None (power down) 0 / 1 / Voice speech 1 / 0 / Audio mono 1 / 1 / Voice speech + audio mono
3–2	HSOL(1–0)	HSOLAMP audio output control: HSOL 1 / HSOL0 / Output Signal 0 / 0 / None (power down) 0 / 1 / Voice speech 1 / 0 / Audio stereo left / mono 1 / 1 / Voice speech + audio stereo left / mono
1–0	HSOR(1–0)	HSORAMP audio output control: HSOR 1 / HSOR 0 / Output Signal 0 / 0 / None (power down) 0 / 1 / Voice speech 1 / 0 / Audio stereo right / mono 1 / 1 / Voice speech + stereo right / mono

5.3.10.8 Audio Stereo Path Control Register

Register: **VAUSCTRL**
Page: 1
Address: 16 (10000b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	AURGA(4:0)					AULGA(4:0)				
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value At Reset	1	1	1	1	1	1	1	1	1	1

Table 5–60. Audio Stereo Path Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION					
9–5	AURGA(4–0)	Audio stereo right/left channel volume control					
4–0	AULGA(4–0)	AURGA4/ AULGA4	AURGA3/ AULGA3	AURGA2/ AULGA2	AURGA1/ AULGA1	AURGA0/ AULGA0	Relative Gain
		0	0	0	0	0	0 dB
		0	0	0	0	1	−1 dB
		0	0	0	1	0	−2 dB
		0	0	0	1	1	−3 dB
		0	0	1	0	0	−4 dB
		0	0	1	0	1	−5 dB
		0	0	1	1	0	−6 dB
		0	0	1	1	1	−7 dB
		0	1	0	0	0	−8 dB
		0	1	0	0	1	−9 dB
		0	1	0	1	0	−10 dB
		0	1	0	1	1	−11 dB
		0	1	1	0	0	−12 dB
		0	1	1	0	1	−13 dB
		0	1	1	1	0	−14 dB
		0	1	1	1	1	−15 dB
		1	0	0	0	0	−16 dB
		1	0	0	0	1	−17 dB
		1	0	0	1	0	−18 dB
		1	0	0	1	1	−19 dB
		1	0	1	0	0	−20 dB
		1	0	1	0	1	−21 dB
		1	0	1	1	0	−22 dB
		1	0	1	1	1	−23 dB
		1	1	0	0	0	−24 dB
		1	1	0	0	1	−25 dB
		1	1	0	1	0	−26 dB
		1	1	0	1	1	−27 dB
		1	1	1	0	0	−28 dB
		1	1	1	0	1	−29 dB
		1	1	1	1	0	−30 dB
		1	1	1	1	1	Mute

5.3.10.9 Audio PLL Register

Register: **VAUDPLL**
Page: 1
Address: 18 (10010b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	I2SON	SFTVOL1†	SFTVOL0†	BYPSFTV†	RSVD			AUPLLON	TPLLON
Access Type	R	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W
Value At Reset	0	0	0	0	0	0	0	0	0	0

† The value of this control bit must not be changed when bit 7 (AUDON) of the power down register equals 1 (see Section 5.3.3.3).

Table 5–61. Audio Stereo Path Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	RSVD	Reserved
8	I2SON	Set the power on of the I2S serial interface (I2SON = 1)
7–6	SFTVOL(1:0)	Audio stereo/mono soft volume control: SFTVOL1 SFTVOL0 Data Format 0 0 1/FS*512 0 1 1/FS*128 1 0 1/FS*8 1 1 1/FS*1/2
5	BYPSFTV	Audio stereo/mono soft volume bypass (active high)
4–2	RSVD	Reserved
1	AUPLLON	Audio PLL power up (active high)
0	TPLLON	Telephone PLL power up (active high)

6 Electrical Characteristics

6.1 Absolute Maximum Ratings Over Operating Free-Air Temperature (unless otherwise noted) †

Supply voltage range VCUSB, VCDBB, VCIO, VCMEM, VCRAM, VCABB . . . . −0.3 V to 7 V
Supply voltage range VCHG . . . . −0.3 V to 20 V
Voltage on any input (Note 1) . . . . −0.3 V to V_{DD} +0.3 V
Peak output current at terminal A3 (VRDBB) . . . . 240 mA
Peak output current at terminal D1 (VRMEM) . . . . 100 mA
Peak output current at terminals [M1, L2] (VRIO) . . . . 240 mA
Peak output current at terminal F1 (VRRAM) . . . . 100 mA
Peak output current at terminal D12 (VRABB) . . . . 150 mA
Peak output current at terminal M3 (VRSIM) . . . . 50 mA
Peak output current at terminal M12 (VRUSB) . . . . 50 mA
Peak output current on all other terminals . . . . −5 to 5 mA
Free-air temperature range . . . . −30°C to 85°C
Maximum junction temperature T_j . . . . 150°C
Storage temperature range . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: V_{DD} is the supply specified in Table 2–3 for each terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 80°C POWER RATING
GQW	1 W	36 mW/°C	1 W	1 W

6.2 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
Main battery supply voltage VCDBB, VCIO1, VCIO2, VCMEM, VCRAM, VCABB	In regulation	3.2	3.6	5.5	V
Backup battery supply voltage VBACKUP	Allowable range (−25°C to 85°C)	3.0	3.2	5.5	V
Battery charger supply voltage VCHG		4.8		20	V
USB supply voltage	In regulation	4		5.5	V

6.3 Electrical Characteristics

Digital ouputs (SIM card level shifter excepted)

PARAMETER	MIN	TYP	MAX	UNIT
Low-level output voltage for ONnOFF, RESPWONz, V_{OL} (I_{OL} = 10 μA) (Note 1)			0.2 VRRTC	V
High-level output voltage for ONnOFF, RESPWONz, V_{OH} (I_{OH} = 10 μA) (Note 1)	0.8 VRRTC			V
Low-level voltage for outputs related to VRIO, V_{OL} (I_{OL} = 1 mA) (Note 1)			0.2 VRIO	V
High-level voltage for outputs related to VRIO, V_{OH} (I_{OH} = 1 mA) (Note 1)	0.8 VRIO			V
Output current on 3-state outputs	−15		15	μA

Digital inputs (SIM card level shifter excepted)

PARAMETER		MIN	TYP	MAX	UNIT
High-level input voltage for ITWAKEUP, CK32K, V_{IH}		0.7 VRRTC			V
Low-level input voltage for ITWAKEUP, CK32K, V_{IL}				0.3 VRRTC	V
High-level voltage for all inputs related to VRIO, V_{IH}		0.7 VRIO			V
Low-level voltage for all inputs related to VRIO, V_{IL}				0.3 VRIO	V
High-level input voltage for TESTRST, VLRTC, VLMEM, V_{IH}		0.7 UPR			V
Low-level input voltage for TESTRST, VLRTC, VLMEM, V_{IL}				0.3 UPR	V
High-level input voltage for PWON, RPWON, RPWON2, V_{IH}		0.7 VBAT			V
Low-level input voltage for PWON, RPWON, RPWON2, V_{IL}				0.3 VBAT	V
Low-level input current @ 0 V	Standard and pulldown inputs	−1			µA
High-level input current @ 2.9 V (all inputs related to VRIO)	Standard and pullup inputs			1	µA
High-level input current @ 3.6 V (all inputs related to VBAT or UPR)	Standard and pullup inputs			1	µA
Low-level input current @ 0 V (TEST3, TEST4, TMS, TDI, RPWON, RPWON2, PWON)	Pullup inputs	−20		−2	µA
Low-level input current @ 0 V (TESTRST)	Pullup inputs	−40		−2	µA
High-level input current @ 2.9 V (TCK)	Pulldown inputs	2		20	µA

SIM card level shifters

PARAMETER		MIN	TYP	MAX	UNIT
SIMCK	Low-level output voltage V_{OL} (I_{OL} = 20 µA), SIMEN = 1			0.2 VRSIM	V
SIMCK	High-level output voltage V_{OH} (I_{OH} = 20 µA), SIMEN = 1	0.7 VRSIM			V
SIMRST	Low-level output voltage V_{OL} (I_{OL} = 200 µA), SIMEN = 1			0.2 VRSIM	V
SIMRST	High-level output voltage V_{OH} (I_{OH} = 200 µA), SIMEN = 1	0.7 VRSIM			V
SIMIO	Low-level output voltage V_{OL} (I_{OL} = 1 mA), DBBSIO = 0.150 V			0.3	V
SIMCK	Low-level output voltage V_{OL} (I_{OL} = 1 mA), SIMEN = 0			0.2 VRSIM	V
SIMRST	Low-level output voltage V_{OL} (I_{OL} = 1 mA), SIMEN = 0			0.2 VRSIM	V

6.4 Electrical Characteristics Over Recommended Ranges Of Supply Voltage and Free-Air Temperature (unless otherwise noted)

Voltage regulators integrated in the TWL3016 device are intended to use low ESR ceramic decoupling capacitors (±10%). The load current capability of the regulators (except VRABB) may be pushed 30% higher if their input voltage range is limited to 3.1 V to 4.5 V.

6.4.1 Voltage Regulator RDBB (Under Active Mode)

Voltage regulator RDBB needs a 10-µF decoupling capacitor[†] connected between the A3 (VRDBB) and GNDD terminals. The sense input feedback terminal A1 (VSDBB) must be connected to the A3 (VRDBB) terminal.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage VCDBB		3.00	VBAT	5.5	V
Output voltage VRDBB	VDBB0 = 0 and VDBB1 = 1 (default if VLRTC0 = 0 and VLRTC = 1)	1.65	1.80	1.95	V
	VDBB0 = 0 and VDBB1 = 0 (default if VLRTC0 = 0 and VLRTC = 0)	1.35	1.50	1.65	
	VDBB0 = 1 and VDBB1 = 0 (default if VLRTC0 = 1 and VLRTC = 1)	1.25	1.30	1.45	
Rated output current I_{OUT}				170	mA
Load regulation	I_{OUT} = maximum to 0			100	mV
Line regulation	Input voltage = 3 V to 5.5 V @ I_{OUT} = maximum VDBB0 = 0 and VDBB1 = 0			50	mV
Response time	I_{OUT} steps from I_{OUT} maximum/2 to I_{OUT} maximum in 5 µs I_{OUT} steps from I_{OUT} maximum to I_{OUT} maximum/2 in 5 µs @ VRDBB = final ±3%		10		µs
Turnon time	From RDBBEN = 0 to 1 @ I_{OUT} = maximum, VRDBB = final ±3%		0.2		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		

[†] 0.01 Ω < ESR < 0.3 Ω

6.4.2 Voltage Regulator RDBB (Under Sleep Mode)

The switch between active/sleep mode is under the control of the VRPC device mode register.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage VCDBB		3.00	VBAT	5.5	V
Output voltage VRDBB	VDBB0 = 0 and VDBB1 = 1	1.65	1.83	1.95	V
	VDBB0 = 0 and VDBB1 = 0	1.35	1.50	1.65	
	VDBB0 = 1 and VDBB1 = 0	1.25	1.30	1.45	
Rated output current				1	mA

6.4.3 Voltage Regulator RIO (Under Active Mode)

Voltage regulator RIO needs a 4.7-μF decoupling capacitor[†] connected between the GNDD terminal and either the M1 (VRIO1) or L2 (VRIO2) terminal. The M1 (VRIO1) and L2 (VRIO2) terminals must be connected together externally. The L1 (VCIO1) and K1 (VCIO2) terminals must also be connected together externally.

> **NOTE:** Voltage regulator RIO supplies the TWL3016 digital I/O and digital core.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage VCIO1 and VCIO2		3.00	VBAT	5.5	V
Output voltage VRIO1 and VRIO2		2.70	2.80	2.90	V
Rated output current I_{OUT}				100	mA
Load regulation	I_{OUT} = maximum to 0			100	mV
Line regulation	Input voltage = 3 V to 5.5 V @ I_{OUT} = maximum			50	mV
Response time	I_{OUT} steps from I_{OUT} max/2 to I_{OUT} max in 5 μs I_{OUT} steps from I_{OUT} max to I_{OUT} max/2 in 5 μs @ VRIO = final ±3%		10		μs
Turnon time	From RIOEN = 0 to 1 @ I_{OUT} = maximum, VRIO = final ±3%		0.2		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		

[†] 0.01 Ω < ESR < 0.3 Ω

6.4.4 Voltage Regulator RIO (Under Sleep Mode)

The switch between active/sleep mode is under the control of the VRPC device mode register.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage VCIO1, VCIO2		3.00	VBAT	5.5	V
Output voltage VRIO1, VRIO2		2.70	2.85	3.00	V
Rated output current	MSKSLPIO = 0 MSKSLPIO = 1 and MSKSLPABB = 0			1 100	mA

6.4.5 Voltage Regulator RRAM (Under Active Mode)

Voltage regulator RRAM needs a 2.2-μF decoupling capacitor[†] connected between the F1 (VRRAM) and GNDD terminals.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage VCRAM		3.00	VBAT	5.5	V
Output voltage VRRAM	VLMEM = 1	2.70	2.80	2.90	V
	VLMEM = 0	1.65	1.80	1.95	
Rated output current I_{OUT}				50	mA
Load regulation	I_{OUT} = maximum to 0			100	mV
Line regulation	Input voltage = 3 V to 5.5 V @ I_{OUT} = maximum VLMEM = 0			50	mV
Response time	I_{OUT} steps from I_{OUT} maximum/2 to I_{OUT} maximum in 5 μs @ V_{OUT} = final ±3% I_{OUT} steps from I_{OUT} maximum to I_{OUT} maximum/2 in 5 μs @ V_{OUT} = final ±3%		10		μs
Turnon time	From RRAMEN = 0 to 1 @ I_{OUT} = maximum, V_{OUT} = final ±3%		0.2		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		

[†] 0.01 Ω < ESR < 0.3 Ω

6.4.6 Voltage Regulator RRAM (Under Sleep Mode)

The switch between active/sleep mode is under the control of the VRPC device mode register.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage VCRAM		3.00	VBAT	5.5	V
Output voltage VRRAM	VLMEM = 1	2.70	2.85	3.00	V
	VLMEM = 0	1.65	1.83	1.95	
Rated output current				1	mA

6.4.7 Voltage Regulator RRAM Reverse Leakage Current Protection (Under Off Mode)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reverse leakage current	VRRAM = 2.6 V, VCRAM = 0–5.5 V, VBACKUP = 3.2 V	−1		0	μA

6.4.8 Voltage Regulator RMEM (Under Active Mode)

Voltage regulator RMEM needs a 2.2-μF decoupling capacitor[†] connected between the D1 (VRMEM) and GNDD terminals.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage VCMEM		3.00	VBAT	5.5	V
Output voltage VRMEM	VLMEM = 1	2.70	2.80	2.90	V
	VLMEM = 0	1.65	1.80	1.95	
Rated output current I_{OUT}				60	mA
Load regulation	I_{OUT} = maximum to 0			100	mV
Line regulation	Input voltage = 3 V to 5.5 V @ I_{OUT} = maximum VLMEM = 0			50	mV
Response time	I_{OUT} steps from I_{OUT} maximum/2 to I_{OUT} maximum in 5 μs I_{OUT} steps from I_{OUT} maximum to I_{OUT} maximum/2 in 5 μs @ VRMEM = final ±3%		10		μs
Turnon time	From RMEMEN = 0 to 1 @ I_{OUT} = maximum, VRMEM = final ±3%		0.2		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		

[†] 0.01 Ω < ESR < 0.3 Ω

6.4.9 Voltage Regulator RMEM (Under Sleep Mode)

The switch between active/sleep mode is under the control of the VRPC device mode register.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage VCMEM		3.00	VBAT	5.5	V
Output voltage VRMEM	VLMEM = 1	2.70	2.85	3.00	V
	VLMEM = 0	1.65	1.83	1.95	
Rated output current				1	mA

6.4.10 Voltage Regulator RSIM (Under Active Mode)

Voltage regulator RSIM needs a 1-μF decoupling capacitor[†] connected between the M3 (VRSIM) and GNDD terminals.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage VCSIM		3.00	VBAT	5.5	V
Output voltage VRSIM	SIMSEL = 1	2.75	2.85	3.0	V
	SIMSEL = 0	1.7	1.80	1.95	
Rated output current I_{OUT}				20	mA
Load regulation	I_{OUT} = maximum to 0			100	mV
Line regulation	Input voltage = 3 V to 5.5 V @ I_{OUT} = maximum VLSIM = 0			50	mV
Response time	I_{OUT} steps from I_{OUT} maximum/2 to I_{OUT} maximum in 5 μs I_{OUT} steps from I_{OUT} maximum to I_{OUT} maximum/2 in 5 μs @ VRSIM = final ±3%		10		μs
Turnon time	From RSIMEN = 0 to 1 @ I_{OUT} = maximum, VRSIM = final ±3%		0.2		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		

[†] 0.01 Ω < ESR < 0.3 Ω

6.4.11 Voltage Regulator RSIM (Under Sleep Mode)

The switch between active/sleep mode is under the control of the VRPC device mode register.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage VCSIM		3.00	VBAT	5.5	V
Output voltage VRSIM	SIMSEL = 1	2.75	2.9	3.1	V
	SIMSEL = 0	1.7	1.83	1.95	
Rated output current				1	mA

6.4.12 Voltage Regulator RABB (Under Active Mode)

Voltage regulator RABB needs a 4.7-μF decoupling capacitor[‡] connected between the D12 (VRABB) and GNDA terminals. This voltage regulator is intended to supply the TWL3016 analog part only. Connecting any external device to the D12 (VRABB) terminal may decrease device performance.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage VCABB		3.0	3.6	5.5	V
Output voltage VRABB		2.7	2.8	2.9	V
Rated output current I_{OUT}				80	mA
Load regulation	From I_{OUT} = maximum to I_{OUT} = 0			100	mV
Line regulation	Input voltage = 3.0 V to 5.5 V @ I_{OUT} = maximum			50	mV
Response time	I_{OUT} steps from I_{OUT} maximum/2 to I_{OUT} maximum in 5 μs I_{OUT} steps from I_{OUT} maximum to I_{OUT} maximum/2 in 5 μs @ VRABB = final ± 3%		10		μs
Turnon time	I_{OUT} steps from 0 to I_{OUT} maximum I_{OUT} steps from I_{OUT} maximum to 0 @ VRABB = final ± 3%		0.5		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		

[†] 0.01 Ω < ESR < 0.3 Ω

6.4.13 Voltage Regulator RABB (Under Sleep Mode)

The switch between active/sleep mode is under the control of the VRPC device mode register.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage VCABB		3.00	VBAT	5.5	V
Output voltage VRABB		2.70	2.85	3.0	
Rated output current				1	mA

6.4.14 Voltage Regulator RRTC

Voltage regulator RRTC needs a 1-μF decoupling capacitor[†] connected between the H1 (VRRTC) and GNDD teminals.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage		2.70	UPR	5.5	V
Output voltage VRRTC	VRRTC0 = 0 and VRRTC1 = 1 (default if VLRTC0 = 0 and VLRTC = 1)	1.65	1.80	1.95	V
	VRRTC0 = 0 and VRRTC1 = 0 (default if VLRTC0 = 0 and VLRRTC1 = 0)	1.35	1.50	1.65	
	VRRTC0 = 1 and VRRTC1 = 0 (default if VLRTC0 = 1 and VLRRTC1 = 0)	1.24	1.30	1.36	
Rated output current I_{OUT}				30	μA
Load regulation	I_{OUT} = maximum to 0			100	mV
Line regulation	Input voltage = 3 V to 5.5 V @ I_{OUT} = maximum VDBB0 = 0 and VDBB1 = 0			50	mV
Response time	I_{OUT} steps from I_{OUT} maximum/2 to I_{OUT} maximum in 5 μs I_{OUT} steps from I_{OUT} maximum to I_{OUT} maximum/2 in 5 μs @ VRRTC = final ±3%		100		μs
Turnon time	From VBAT = 0 V to 3.6 V @ I_{OUT} = maximum, VRRTC = final ±3%		100		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		
Quiescent current			2	4	μA

[†] 0.01 Ω < ESR < 0.3 Ω

6.4.15 Voltage Regulator RUSB

Voltage regulator RUSB needs a 1-μF decoupling capacitor[†] connected between the M12 (VRUSB) and GNDD terminals.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage		4.0	5	5.5	V
Output voltage VRUSB		3.1	3.30	3.5	V
Rated output current I_{OUT}				15	mA
Load regulation	I_{OUT} = maximum to 0			100	mV
Line regulation	Input voltage = 4.0 V to 5.5 V @ I_{OUT} = maximum			50	mV
Response time	I_{OUT} steps from I_{OUT} maximum/2 to I_{OUT} maximum in 5 μs I_{OUT} steps from I_{OUT} maximum to I_{OUT} maximum/2 in 5 μs @ VRUSB = final ±3%		10		μs
Turnon time	From VCUSB = 0 V to 5.0 V @ I_{OUT} = maximum, VRUSB = final ±3%		0.2		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		

[†] 0.01 Ω < ESR < 0.3 Ω

6.4.16 Bandgap Reference

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage on VREF	ACTIVE mode SLEEP mode, MSKSLPV = 0 SLEEP mode, MSKSLPV = 1	1.16	1.18 1.2 1.18	1.20	V
Output voltage on IBIAS	ACTIVE mode, RBIAS = 120 kΩ SLEEP mode, MSKSLPABB = 1 SLEEP mode, MSKSLPABB = 0	1.14	VREF 0 VREF	1.21	V

6.5 VRPC State Machine Characteristics

6.5.1 Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wait after a bandgap enable: NBGSL*T NBGOFF*T	Previous state was SLEEP (Note 3) Previous state was OFF (Note 3)		131*T 1019*T		Note 2
Wait after VRDBB regulator enable: NDL1SL*T NLD1OFF*T	Previous state was SLEEP (Note 3) Previous state was OFF (Note 3)		0*T 80*T		
Wait after VRIO regulator enable: NDL2SL*T NLD2OFF*T	Previous state was SLEEP (Note 3) Previous state was OFF (Note 3)		17*T 14*T		
PWON, RPWON, RPWON2 debouncing delay: NDEBB*T	RPWON = 1, measure between falling edge of PWON and INT2. (Note 3)		1028*T		
VCHG, VCUSB, VBATLOW debouncing delay: NDEBV*T			1*T		
SLEEP delay: SLPDLY*20*T	SLPDLY[4:0] = 1F SLPDLY[4:0] = 00		620*T 0*T		
System reset delay: PORSTD*T	RPWON = 1, measure between falling edge PWON and RESPWONz.		2^{20}*T		

NOTES: 2. T = 1/CK32K clock
           3. A TESTRST activation (TESTRST set to 1) cancels the delays described above (debug purpose).

6.5.2 Power On/Power Off and Backup Conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Battery voltage to enter the active mode from the off mode ONnOFF high level	Measured on the VBAT terminal		3.2		V
Battery voltage to enter the backup mode from the active mode, ONnOFF low level	VBACKUP = 3.2 V, measured on the VBAT terminal (monitored on ONnOFF terminal)	2.6	2.75	2.9	V
Battery voltage to enter the off mode from the nobat mode RESPWONz high level	Measured on the VBAT terminal (monitored on the RESPWONz terminal)	2.5		3.2	V
Battery voltage to enter the nobat mode from the backup mode, RESPWONz low level	Measured on the VBACKUP terminal) (monitored on the RESPWONz terminal)	1.9	2.1	2.3	V

6.5.3 Switch On Conditions/Accessories Plugged/Unplugged Interrupt Threshold

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Battery charger plugged	Measured on VCHG terminal, VBAT = 3.6 V (monitored on the INT2 terminal)		VBAT+0.4		V
Battery charger unplugged	Measured on VCHG terminal, VBAT = 3.6 V (monitored on the INT2 terminal)		0		V
USB supply plugged/unplugged	Measured on VCUSB terminal, VBAT = 3.6 V (monitored on the INT2 terminal)		3.8		V

6.6 Current Consumption

All current consumption measurements are performed with: RBIAS = 120 kΩ.

6.6.1 Device Off Modes

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Off mode	Battery 5.5 V, CK13M clock off, no load on any LDO, BBCHGEN = 0, MSKOFFxxx = 0, measured on main battery, MESBB = 0, MESBAT = 0		17	35	µA
Sleep mode	Main battery 5.5 V, CK13M clock off, no load, BBCHGEN = 0, measured on main battery, MSKSLPABB = 1		80		µA
	Main battery 5.5 V, CK13M clock off, no load, BBCHGEN = 0, measured on main battery, MSKSLPABB = 0		140	150	
	Main battery 5.5 V, CK13M clock off, no load, BBCHGEN = 0, measured on main battery, MSKSLPABB = 0 and MSKSLPIO = 1		220		
Backup mode on backup battery	Backup battery 3.2 V, main battery 0 V, CK13M clock off, no load, (measured on backup battery), RESPWONz = 1		3.0	6	µA

6.6.2 Device On Modes

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Active mode: idle	Battery 5.5 V, CK13M clock is off, CK32K clock is on. No external loads are on LDO.		0.7	1	mA
Activ mode: power on	Battery 5.5 V, CK13M clock is on. All blocks are in power down, power management is excepted. No external loads are on LDO.		1.3	2.0	mA

6.6.3 Blocks Power Consumption

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio voiceband codec (VBC)	WBA = 0, MICAMP and EARAMP on, see Note 4 WBA = 1, MICAMP and EARAMP on WBA = 1, MICAMP and SPKAMP @ 2.5 dB on		4.1 6.2 10.5		mA
Audio stereo codec (AUSC)	SRW = 010, AUFS = 44.1 kHz, HSOAMPL and HSOAMPR are on		5.6		mA
Baseband codec (BBC)	BULON = 1, BULENA = 1		7.5		mA
	BDLON = 1, BDLENA = 1		16		
Frequency control (AFC)			0.6		mA
Auxiliary DAC (ADAC)			0.2		mA
Monitoring ADC (MADC)			0.5		mA
SIM interface			0.15		mA

NOTE 4: Measurements are for blocks in power up mode without transmit or receive activity. System clock is running on 13 MHz.

The consumption is given for a standalone block. To have the total consumption, add the current described in Section 6.6.2, *Device ON Modes*.

6.7 SIM Card Interface Switching Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock frequency DBBSCK/SIMCK	C_L = 30 pF	1.0		5.0	MHz
Rise and fall time at SIMCK	C_L = 30 pF			20	ns
Rise and fall time at DBBSIO/SIMIO	C_L = 30 pF			1	µs
Rise and fall time at SIMRST	C_L = 30 pF			400	µs
Data rate on DBBSIO/SIMIO				CK13M/32	MHz

6.8   Battery Charger Interface

6.8.1   Backup Battery Charger

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBACKUP to MADC input attenuation	VBACKUP from 2.4 V to 5.5 V	0.2	0.25	0.35	V/V
Backup battery charging current	VBACKUP = 2.8 V, BBCHEN = 1	350	500	900	μA
	VBACKUP = 0 V, BBCHEN = 1	350	500	900	
End backup battery charging voltage: VBBCHGEND	$I_{VBACKUP}$ = −10 μA, BBSEL = 00	3.0	3.1	3.2	V
	$I_{VBACKUP}$ = −10 μA, BBSEL = 01	3.1	3.2	3.3	
	$I_{VBACKUP}$ = −10 μA, BBSEL = 10	2.9	3.0	3.1	
	$I_{VBACKUP}$ = −10 μA, BBSEL = 11	VBAT−0.2	VBAT		

6.8.2 Main Battery Charger

VBAT = 3.6 V, R_S = 0.22 Ω, unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCHG input voltage range (Note 5)		4.8		20	V
Precharge power dissipation	V(VCHG – PCHG)* I_{PRECH}			700	mW
Precharge Ron	Measured between VCHG and PCHG, VBAT = 0.5 V VCHG = 6.8 V and 20 V, I_{PRECH} = 100 mA	1	4	10	Ω
Battery voltage at precharge end	VBAT input, maximum current depends on external resistor	3.6	3.8	4.0	V
VCHG to MADC input attenuation	VCHG from 4.8 V to 6.8 V	0.15	0.20	0.30	V/V
VBAT to MADC input attenuation	VBAT from 3.0 V to 5.5 V	0.2	0.25	0.35	V/V
ICTL output voltage swing	I_{ICTL} = –10 μA, CHEN = 0 or CHEN = 1 and CHDISPA = 1	VCHG–0.3			V
	I_{ICTL} = +10 μA, CHEN = 1 and CHBPASSPA = 1			0.35	
	I_{ICTL} = –5 μA, CHEN = 1, MESBAT = 1, CHGVREG = 0x000	VCHG–0.3			
	I_{ICTL} = +5 μA, CHEN = 1, MESBAT = 1, CHGVREG = 0x3FF			0.8	
I-to-V conversion slope (see Note 6)	(VCCS–VBATS) rising from 0.1 V to 0.17 V: CGAIN4 = 0 (VCCS–VBATS) rising from 0.25 V to 0.425 V: CGAIN4 = 1	1.76 0.704	2.2 0.88	2.64 1.056	mV/mA
I-to-V conversion offset	OFFEN = 1, OFFSN(1:0) = 00, CGAIN4 = 0		100		mV
I-to-V conversion offset shift	OFFEN = 1, OFFSN(1:0) = 11, CGAIN4 = 0	300	400	500	mV
Charge voltage DAC linear range	CHIV = 0	0AF		3FF	hex
Charge current DAC linear range	CHIV = 1	2C		FF	hex
ADIN2 or ADIN3 dc current source for temperature measurement	R(IBIAS) = 120 kΩ, ADIN2 = ADIN3 = 1 V, THENSA = 0/1 THSENS[2–0] = 000	8		12	μA
	THSENS[2–0] = 001	16		24	
	THSENS[2–0] = 010	26		34	
	THSENS[2–0] = 011	36		44	
	THSENS[2–0] = 100	46		54	
	THSENS[2–0] = 101	55.5		64.5	
	THSENS[2–0] = 110	65.5		74.5	
	THSENS[2–0] = 111	75		85	
ADIN1 dc current source for battery identification	R_{IBIAS} = 120 kΩ, ADIN1 = 1 V, TYPEN = 1	8		12	μA
Main battery presence detect threshold	VBATCHKEN = 1, CHEN = 0, measured through ADIN2 rising voltage and sourced current, monitoring BATSTS value, VCHG = 4.8 V and 20 V	0		100	kΩ

NOTES: 5. The maximum voltage value of the charging device is 20 V (process limitation). The minimum voltage value of the charging device is:
VBATMAX + diode drop + 0.2 Ω resistor drop + VDC drop.
Where VBATMAX is the maximum voltage value of the battery (4.2 V for Li-ion battery). For example to charge Li–ion battery with 1-A fast current charge, the minimum voltage value of the charging device must be 5.1 V.

6. MADC output code = (VCCS – VBATS) * 10 + offset with CGAIN4 = 0
MADC output code = (VCCS – VBATS) * 4 with CGAIN4 = 1, OFFSEN = 0

6.8.3 BCI Protection Comparator

VBAT = 3.6 V, VCHG = 4.8 V unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overtemperature threshold	PROCTL(1:0) = 01, CHVREG(9:0) = 0x3FF	1.65	1.75	1.85	V
	PROCTL(1:0) = 01, CHVREG(9:0) = 0x0AF	0.2	0.3	0.4	
	CHIV = 1, CGAIN4 = 1, CHIREG(7:0) = 0xFF, VCCS = VBATS = VBAT, measured through ADIN2 rising voltage, monitoring ICTL				
Falling end-of-charge current threshold (see Note 6)	PROCTL(1:0) = 10, OFFEN = 0, CHIREG(7:0) = 0xFF, CGAIN4 = 0, CHEN = 1, MESBAT = 1, CHIV = 0, CHGVREG = 0x3FF, measured through MADC, (VCCS–VBATS) falling voltage, monitoring ICTL	165	175	185	mV
Overvoltage threshold (see Note 7)	PROCTL(1:0) = 11, CHVREG(9:0) = 0x200, MESBAT = 1, CHIV = 1, CGAIN4 = 1, CHIREG(7:0) = 0xFF, VCCS = VBATS = VBAT measured through MADC, VBAT rising voltage, monitoring ICTL	3.4	3.5	3.6	V

NOTE 7:   MADC output code = VBAT * 0.25

6.8.4 BCI LED Driver

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LEDC maximum voltage				VCHG	V
LEDC driven current	Current sink			10	mA
LEDC drop	ILEDC = 10 mA, measure vs GNDD, LEDC ON			400	mV

6.8.5 BCI Watchdog Timer

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Watchdog delay	KEY[7:0] = 10101010 01010101 11011011 10111101		32000*T 64000*T 128000*T 256000*T		Note 8

NOTES: 8.   T = 1/CK32K clock

6.9 ADC Characteristics

6.9.1 Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			10		Bit
MADC voltage reference			1.75		V
Input leakage current ADINx				1	µA
Differential nonlinearity		–2		2	LSB
Integral nonlinearity	Best fitting	–2		2	LSB
Input range		0		1.75	V

6.9.2 Switching Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Running frequency F		1		MHz
Clock period t = 1/F		1		µs
Conversion time (N: number of analog input to convert)		2.5 t + N*25 t		µs

6.9.3 Global Characteristics

PARAMETER	MIN	TYP	MAX	UNITS
Input capacitor (maximum settling time for the input signal is 16*t)		12		pF

6.10 Automatic Power Control (APC)

6.10.1 DAC 10 Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			10		Bit
Integral nonlinearity	Best fitting line	−1		+1	LSB
Differential nonlinearity		−1		+1	LSB
Settling time			5		µs

6.10.2 Output Stage Characteristics

The recommended load on the C11 (APC) terminal is a 50-pF capacitor (maximum value) in parallel with a 10-kΩ resistor (minimum value).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage with code maximum		2	2.2	2.4	V
Offset voltage	AUXAPC = 0 APCOFF = 0		120	200	mV
Offset voltage adjustment			128	150	mV
Offset voltage adjustment step			2	2.3	mV
Output impedance in power down				150	Ω
Output voltage in power down				50	mV

6.10.3 Timings

PARAMETER		MIN	TYP	MAX	UNITS
t_{DELUP}	Delay BULEN ↑ to ramp-up start	2		1025	1/4-bit
t_{DELCHG}	Delay SLOT N modulation to SLOT N ramp-up start	2		1025	1/4-bit
t_{DELDWN}	Delay BULEN ↓ to ramp-down start	2		1025	1/4-bit
t_{RUP}	Ramp-up duration	5		16	1/2-bit
t_{RDWN}	Ramp-down duration	5		16	1/2-bit
t_{TAIL}	Modulation after BULEN ↓		32		1/4-bit
T_{SLOT}	Delay SLOT N ramp-up to SLOT N+1 ramp-up start (same DELUP settings)		156.25		bit

† Bit is relative to GSM bit = 1/270.833 kHz.
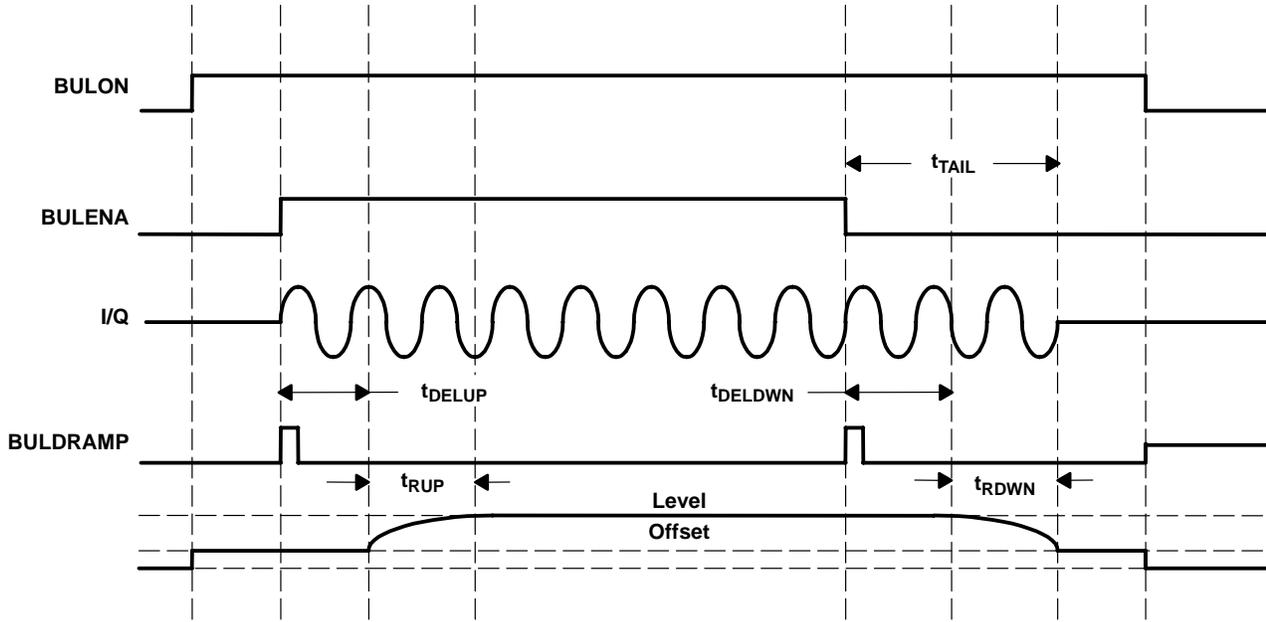
Figure 6–1. APC Single Slot Timing
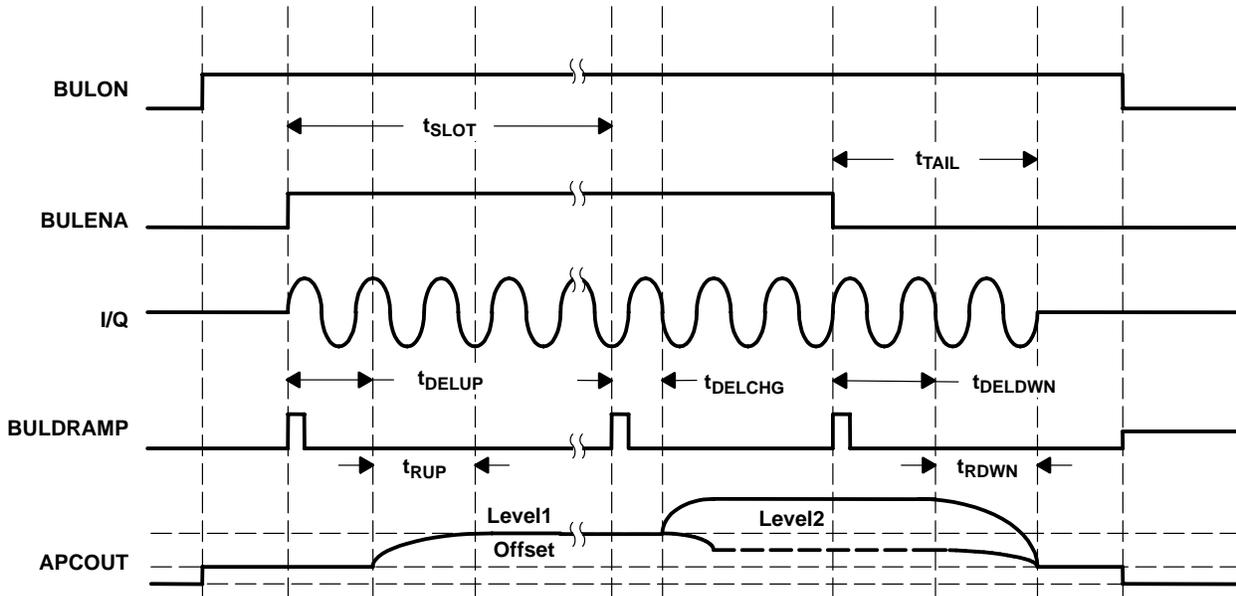
Figure 6–2. APC Multislot Timing

6.11 Clocks And Interrupts

PARAMETER	MIN	TYP	MAX	UNIT
Master clock signal frequency CK13M		13		MHz
Master clock duty-cycle CK13M	45	50	55	%
Real time clock signal frequency CK32K		32.668		kHz
Real time clock duty-cycle CK32K	45	50	55	%
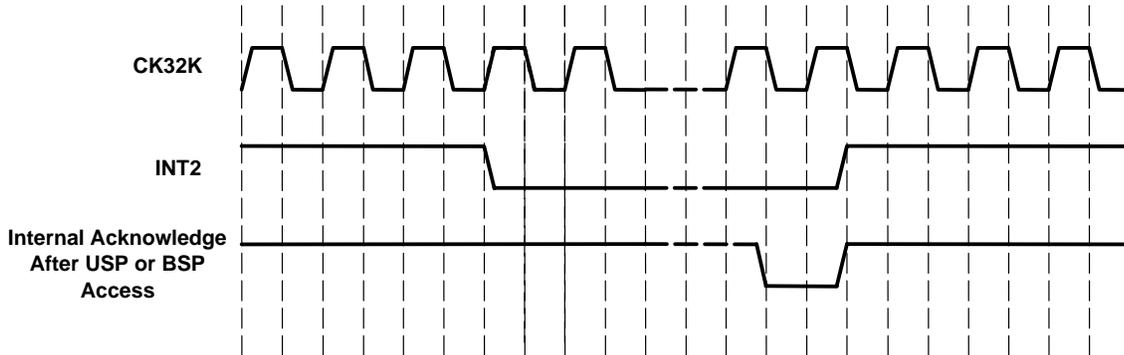
Figure 6–3. Interrupt 2 Timing

6.12 USP Interface Timings Requirements

PARAMETER		MIN	TYP	MAX	UNITS
t_{SU1}	UEN setup delay before CK13M ↑	15			ns
t_{H1}	UEN hold after CK13M ↑	15			ns
t_{SU2}	UDR setup delay before CK13M low	15			ns
t_{H2}	UDR hold after CK13M ↓	15			ns
t_{D1}	UDX delay after CK13M ↑			28	ns
Time between continuous words		8			t

t = CK13M clock period = 77 ns (ATIVMCLK = 1)
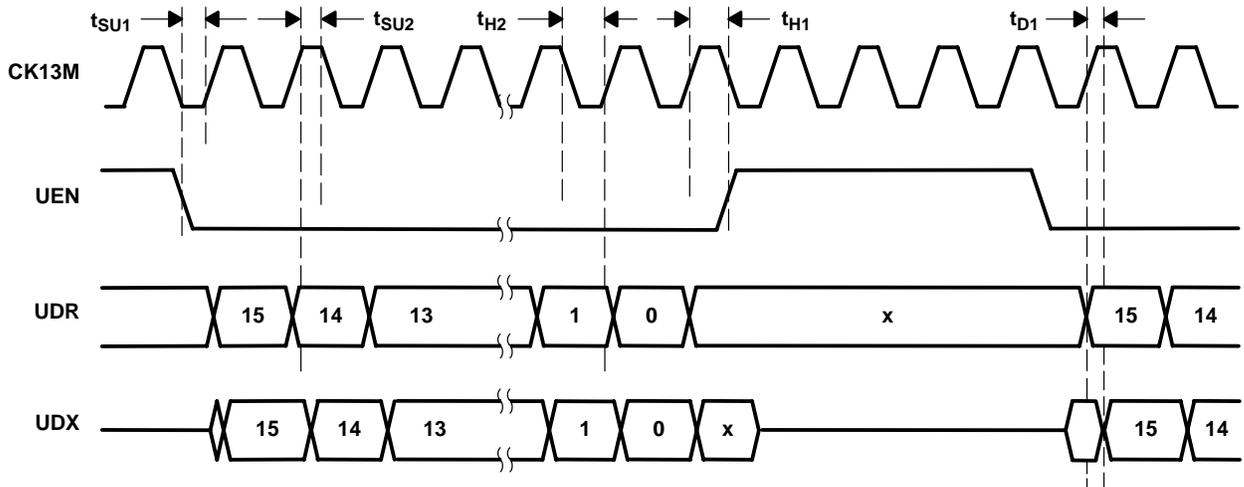
Figure 6–4. Receive and Transmit USP Operations

6.13 TSP Interface Timings Requirements

PARAMETER		MIN	TYP	MAX	UNIT
t1	TEN ↓ setup time before CK13M ↑	0	65		ns
t2	TDR valid after TEN ↓		t		ns
t3	Bit duration		2t		ns
t4	Data duration		14t		ns
t5	TEN low hold time after last bit		T		ns
t6	TEN setup time (low to high) before CK13M high		65		ns

t = CK13M clock period = 77 ns
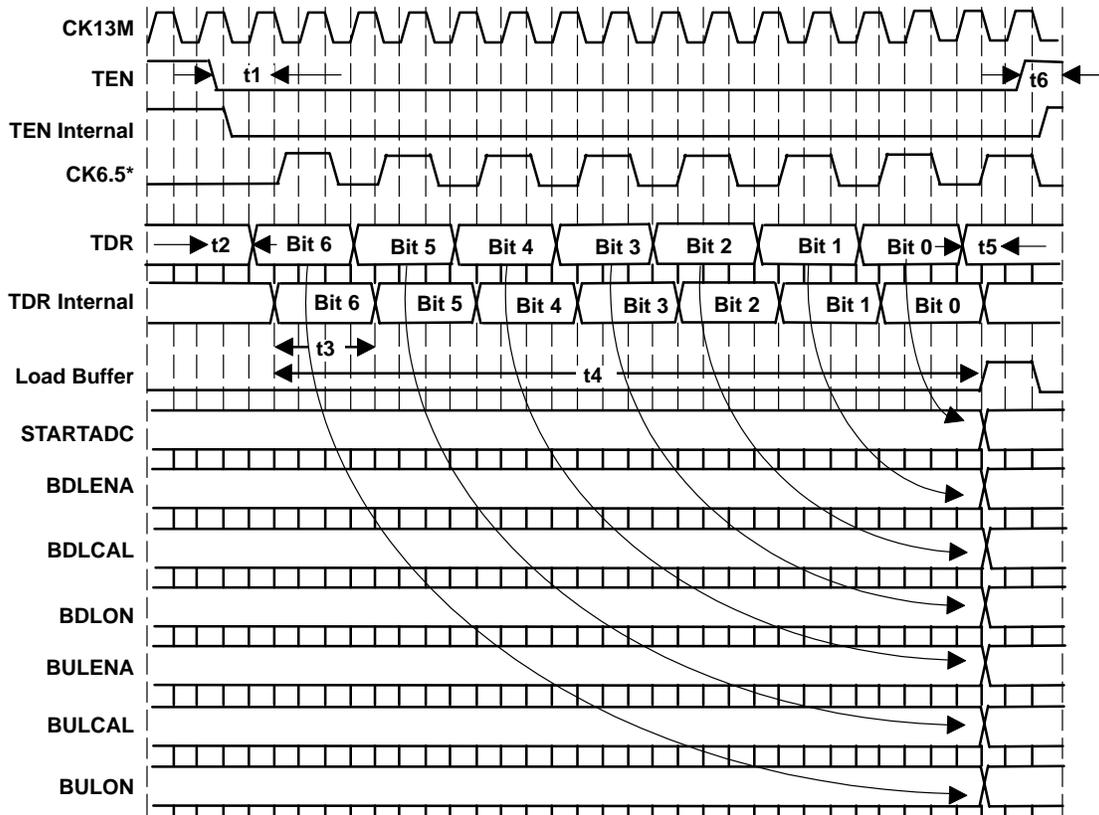
Figure 6–5. TSP Interface Timing Diagram

6.14 VSP Interface Timings Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCK signal frequency		VSPCK = 0 VSPCK = 1, WBA = 0 VSPCK = 1, WBA = 1		CK13M/26 CK13M/13 2		MHz
VCK signal jitter		VSPCK = 0 VSPCK = 1, WBA = 0 VSPCK = 1, WBA = 1	−2 −2 −2		+2 +2 +2	1 µs
VCK duty cycle		VSPCK = 0 VSPCK = 1, WBA = 0 VSPCK = 1, WBA = 1	40	50	60	%
VFS signal frequency		WBA = 0 WBA = 1		8 16		kHz
t_{RDS}	VFS ↑ delay after VCK ↑	CL = 10 pF, VCK = 0.3*V_{DD}, VFS = 0.3*V_{DD}	−7		2	ns
t_{FDS}	VFS ↓ delay after VCK ↑	CL = 10 pF, VCK = 0.3*V_{DD}, VFS = 0.3*V_{DD}	−7		2	ns
t_{DX}	VDX delay after VCK ↑		0		100	ns
t_{RSD}	VDR setup time before VCK ↓		100			ns
t_{RHD}	VDR hold time after VCK ↓		100			ns
Tel PLL lock time		WBA = 1		50		µs
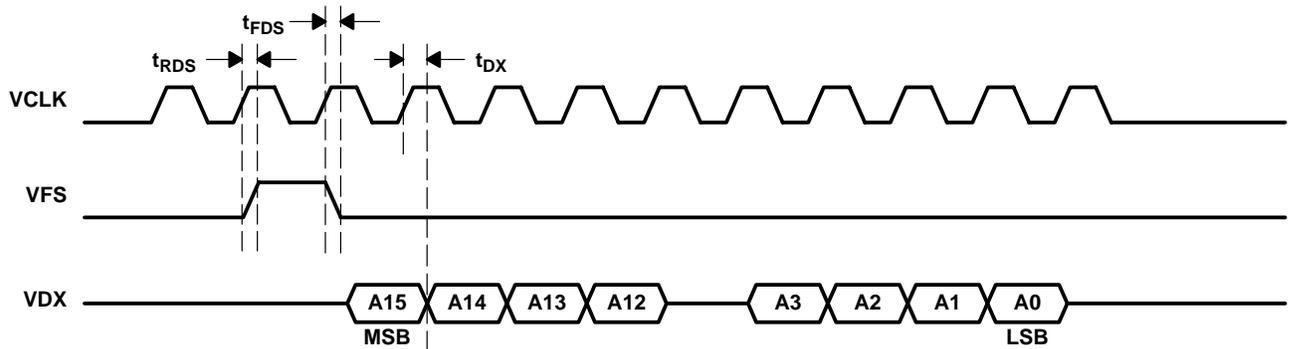
Transmit Operation
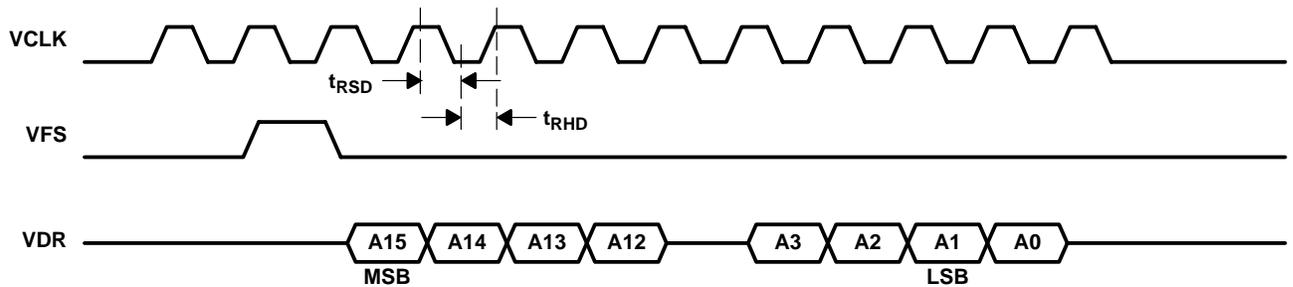
Receive Operation

Figure 6–6. Voice Serial Port Operations

6.15 Audio Interface Timings Requirements

The TWL3016 device supports I2S audio interface mode. The MSB is available on the second rising edge of AUCK, after the falling edge of AUFS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Left/right N bits to receive				16	16	Bit
Total data to receive (left + right) = 2x(N+4)				40	40	Bit
AUCK signal frequency (see Section 5.3.10.6)				40*AUFS		kHz
AUCK duty cycle			40	50	60	%
Stereo audio PLL lock time				10		ms
AUFS signal frequency		SRW[2:0] = 000 (default)		48		kHz
		SRW[2:0] = 010		44.1		
		SRW[2:0] = 011		32		
		SRW[2:0] = 100		22.05		
		SRW[2:0] = 101		16		
		SRW[2:0] = 110		11.025		
		SRW[2:0] = 111		8		
AUFS duty cycle				50		%
t_{DS}	AUFS delay after AUCK ↓				30	ns
t_{RSD}	AUDR setup time before AUCK ↑		30			ns
t_{RHD}	AUDR hold time after AUCK ↑		30			ns
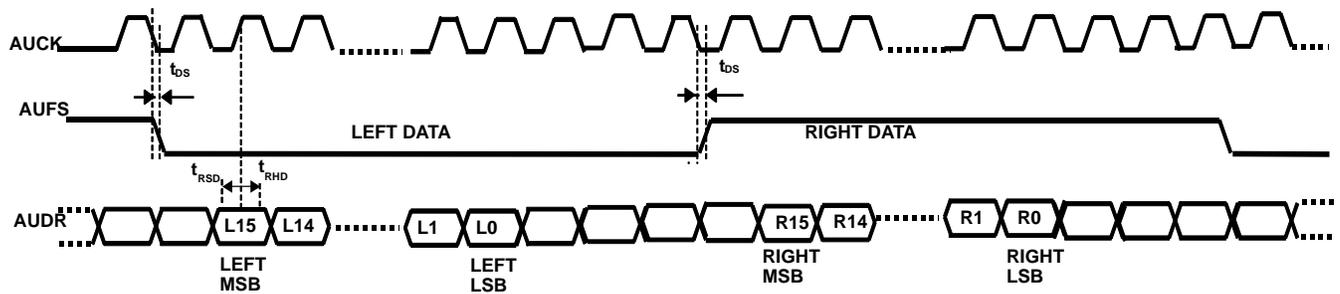
Figure 6–7. I2S Audio Serial Port Operations
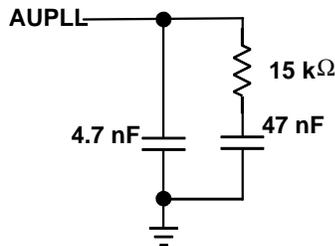
Figure 6–8. Stereo Audio PLL External Filter

6.16 BSP Interface Timings Requirements

PARAMETER		MIN	TYP	MAX	UNIT
t_{SU3}	BFSR setup time before CK13M $\downarrow$	15			ns
t_{H3}	BFSR hold time after CK13M $\downarrow$	15			ns
t_{SU4}	BDR setup time before CK13M $\downarrow$	15			ns
t_{H4}	BDR hold time after CK13M $\downarrow$	15			ns
t_{D2}	BFSX delay from CK13M $\uparrow$			28	ns
t_{D3}	BDX delay after CK13M $\uparrow$			28	ns

t = CK13M clock period = 77 ns
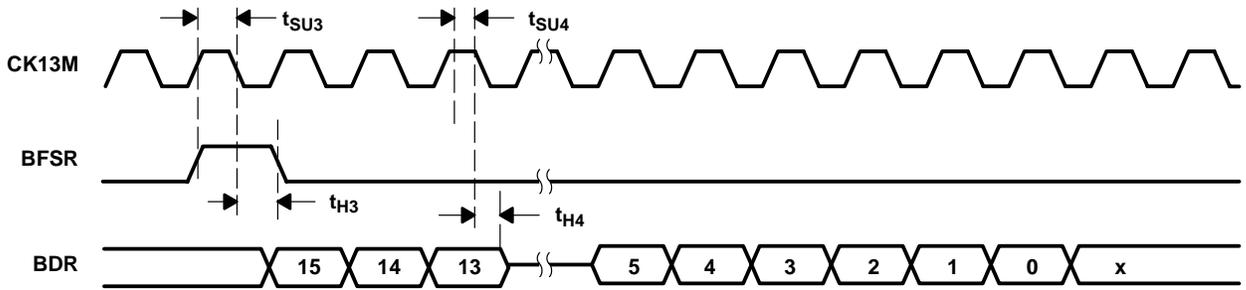
Receive Operation
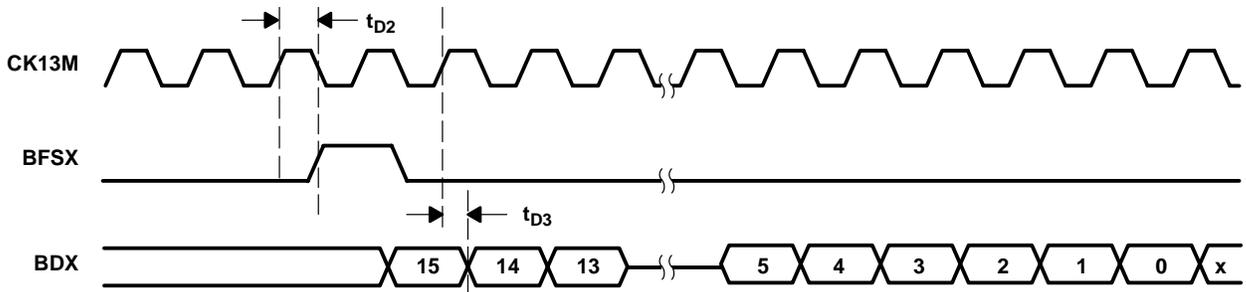
Transmit Operation

Figure 6–9. Single BSP Operations
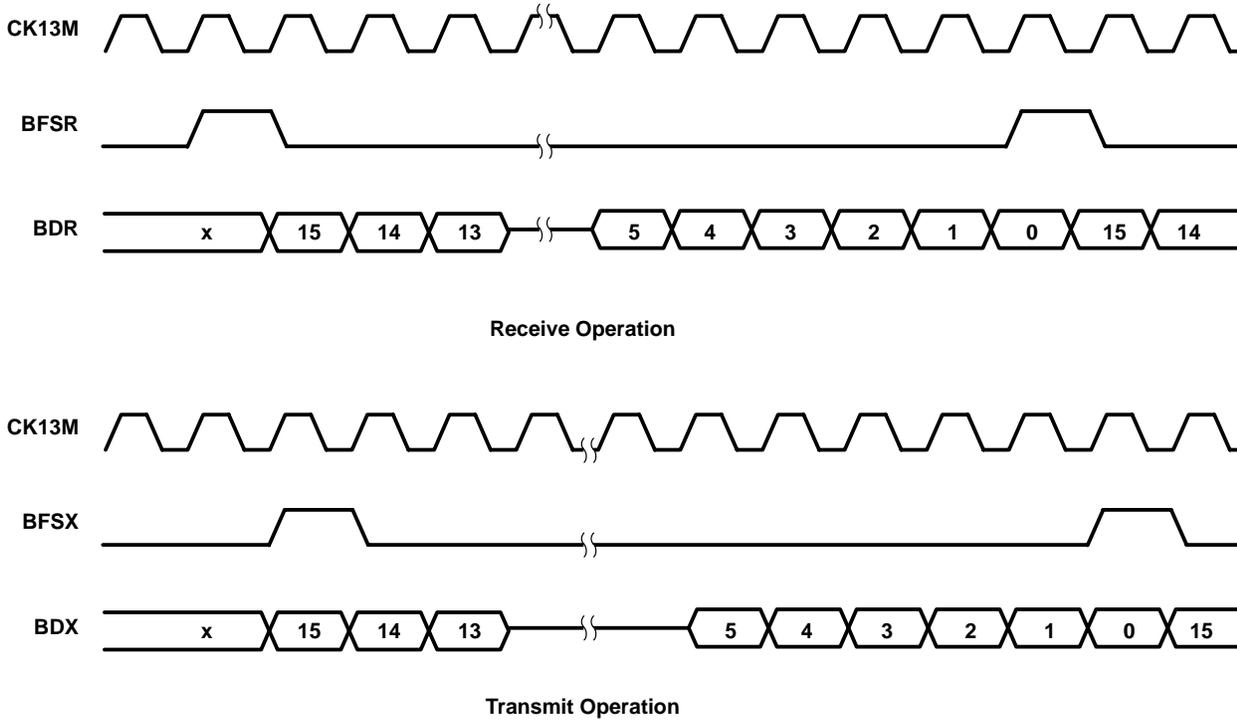
Figure 6–10. Adjacent BSP Operations

6.17 JTAG Interface Timings Requirements

PARAMETER		MIN	TYP	MAX	UNIT
TCK frequency			6.5		MHz
t_{SUMS}	Setup time TMS to TCK ↑	15			ns
t_{SUDI}	Setup time TDI to TCK ↑	15			ns
t_{DDO}	Delay time TDO from TCK ↓			30	ns
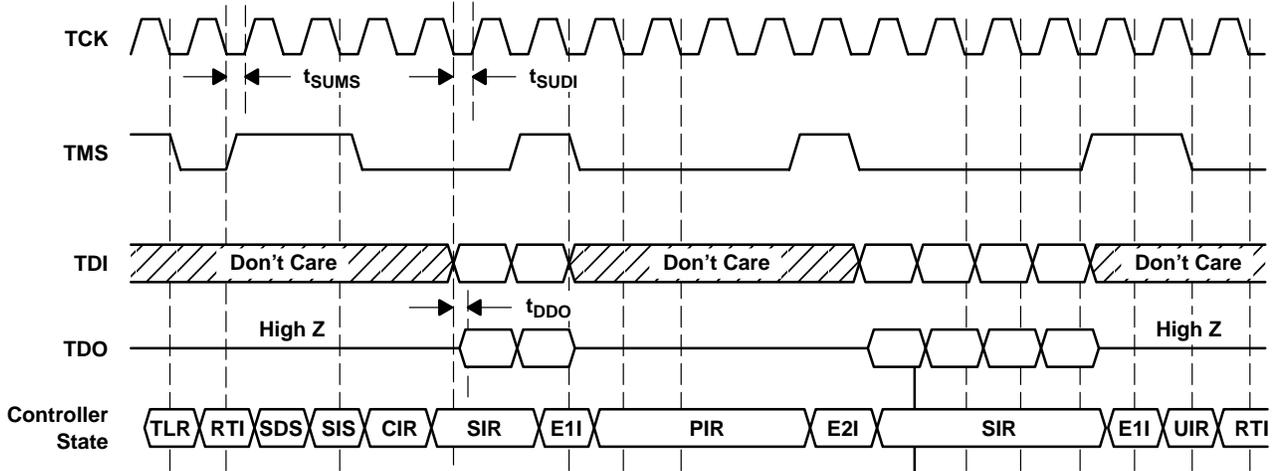
Figure 6–11. Controller State

6.18 Operating Characteristics

6.18.1 Audio Codec

6.18.1.1 Audio Inputs

Global characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum input range (MICIP−MICIN)	Inputs 3 dBm0 (maximum digital sample amplitude with PGA gain set to 0 dB)		32.5		mVrms
Maximum input range (AUXI)	Inputs 3 dBm0 (maximum digital sample amplitude with PGA gain set to 0 dB), MICAMP gain = 4.6 dB		365		mVrms
	Inputs 3 dBm0 (maximum digital sample amplitude with PGA gain set to 0 dB), MICAMP gain = 28.2 dB		24		
Maximum input range (HSMIC)	Inputs 3 dBm0 (maximum digital sample amplitude with PGA gain set to 0 dB)		78		mVrms
Maximum input range (HSMIC−AUXI)	Inputs 3 dBm0 (maximum digital sample amplitude with PGA gain set to 0 dB), HSDIF = 1		32.5		mVrms
Nominal reference level (MICIP−MICIN)			−10		dBm0
Nominal reference level at (AUXI)			−10		dBm0
Nominal reference level at (HSMIC)			−10		dBm0
Nominal reference level at (HSMIC−AUXI)	HSDIF = 1		−10		dBm0
Differential input resistance (MICIP−MICIN)	HSDIF = 0		36		kΩ
Differential input resistance (HSMIC−AUXI)	HSDIF = 1		36		kΩ
Microamplifier gain (MICIP−MICIN)	HSDIF = 0		25.6		dB
Microamplifier gain (HSMIC−AUXI)	HSDIF = 1		25.6		dB
Auxiliary gain amplifier (AUXI)	VBDFAUXG = 0		4.6		dB
	VBDFAUXG = 1		28.2		
Headset microamplifier gain (HSMIC)			18		dB
Input resistance at AUXI	VBDFAUXG = 0		180		kΩ
	VBDFAUXG = 1 or HSDIFF = 1		18		
Input resistance at HSMICIP	HSDIFF = 0		55		kΩ
DC level at MICBIAS	MICBIAS bit = 0, $I_{MICBIAS}$ = 0 to 2 mA	1.9		2.1	V
	MICBIAS bit = 1, $I_{MICBIAS}$ = 0 to 2 mA	2.4		2.6	
DC level at HSMICBIAS	MICBIAS bit = 0, $I_{MICBIAS}$ = 0 to 2 mA	1.9		2.1	V
	MICBIAS bit = 1, $I_{MICBIAS}$ = 0 to 2 mA	2.4		2.6	
Current capability at MICBIAS		0		2	mA
Current capability at HSMICBIAS		0		2	mA

6.18.1.2 Voiceband: Uplink Path

Global characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
PGA absolute gain	VULPGA code 10000	−12 dB	−12.5	−12	−11.5	dB
	VULPGA code 10111	−11 dB	−11.5	−11	−10.5	
	VULPGA code 11000	−10 dB	−10.5	−10	−9.5	
	VULPGA code 11001	−9 dB	−9.5	−9	−8.5	
	VULPGA code 11010	−8 dB	−8.5	−8	−7.5	
	VULPGA code 11011	−7 dB	−7.5	−7	−6.5	
	VULPGA code 00000	−6 dB	−6.5	−6	−5.5	
	VULPGA code 00001	−5 dB	−5.5	−5	−4.5	
	VULPGA code 00010	−4 dB	−4.5	−4	−3.5	
	VULPGA code 00011	−3 dB	−3.5	−3	−2.5	
	VULPGA code 00100	−2 dB	−2.5	−2	−1.5	
	VULPGA code 00101	−1 dB	−1.5	−1	−0.5	
	VULPGA code 00110	0 dB	−0.5	0	0.5	
	VULPGA code 00111	1 dB	0.5	1	1.5	
	VULPGA code 01000	2 dB	1.5	2	2.5	
	VULPGA code 01001	3 dB	2.5	3	3.5	
	VULPGA code 01010	4 dB	3.5	4	4.5	
	VULPGA code 01011	5 dB	4.5	5	5.5	
	VULPGA code 01100	6 dB	5.5	6	6.5	
	VULPGA code 10001	7 dB	6.5	7	7.5	
	VULPGA code 10010	8 dB	7.5	8	8.5	
	VULPGA code 10011	9 dB	8.5	9	9.5	
	VULPGA code 10100	10 dB	9.5	10	10.5	
	VULPGA code 10101	11 dB	10.5	11	11.5	
	VULPGA code 10110	12 dB	11.5	12	12.5	
	Others cases		−6.5	−6	−5.5	
Power supply rejection	0 Hz to 100 kHz		40			dB

Frequency response 4-kHz bandwidth

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response relative to reference gain at 1.015 kHz	≤ 100 Hz			−20	dB
	100 Hz to 200 Hz			−10	
	300 Hz to 400 Hz	−2	0	+1	
	400 Hz to 3300 Hz	−1	0	+1	
	3300 Hz to 3400 Hz	−2	0	+1	
	4000 Hz to 4600 Hz			−17	
	4600 Hz to 6000 Hz			−40	
	≥ 6000 Hz			−45	

Frequency response 8-kHz bandwidth (wideband)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response relative to reference gain at 2.031 kHz	≤ 100 Hz			−11	dB
	200 Hz to 300 Hz			−3	
	300 Hz to 400 Hz	−7	0	+1	
	800 Hz to 1000 Hz	−3	0	+1	
	1400 Hz to 6600 Hz	−1	0	+1	
	6600 Hz to 6800 Hz	−2	0	+1	
	8000 Hz to 9200 Hz			−17	
	9200 Hz to 12000 Hz			−40	
	≥ 12000 Hz			−45	

Psophometric TSNR 4-kHz and 8-kHz bandwidth

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Psophometric TSNR (harmonic distortion + SNR) 1.015-kHz or 2.031-kHz tone (WBA = 1)	3 dBm0 (maximum digital code)	35	48		dB
	0 dBm0	40	66		
	−5 dBm0	42	70		
	−10 dBm0	45	67		
	−20 dBm0	42	56		
	−30 dBm0	40	46		
	−40 dBm0	30	36		
	−50 dBm0	20	26		
	−60 dBm0		15		
Maximum idle channel noise				−72	dBm0
Crosstalk with the downlink path	Downlink path loaded at 33 Ω			−66	dB

Gain characteristics 4-kHz and 8-kHz bandwidth

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Absolute gain error 1.015-kHz or 2.031-kHz tone (WBA = 1)	At 0 dBm0	−1		1	dB
	At −10 dBm0	−11		−9	
Gain tracking error	3 dBm0	−0.25		0.25	dB
	0 dBm0	−0.25		0.25	
	−5 dBm0	−0.25		0.25	
	−10 dBm0 (reference)		0		
	−20 dBm0	−0.25		0.25	
	−30 dBm0	−0.25		0.25	
	−40 dBm0	−0.35		0.35	
	−50 dBm0	−0.50		0.50	
Number of meaningful output bits	PGA set to 0 dB		13		Bit

6.18.1.3 Audio Outputs

Output load conditions (see Figure 6−13)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential minimum resistive load between EARP and EARN: R//	Output swing 3.9 V_{PP}		120		Ω
	Output swing 1.5 V_{PP}		33		
Differential maximum capacitor load between EARP and EARN: C//				100	pF
Common mode minimum resistive load at EARP or EARN			200		$k\Omega$
Common mode maximum capacitor load at EARP or EARN				10	pF
Minimum output resistive load at AUXO:		1.0	1.2		$k\Omega$
Maximum coupling capacitor load at AUXO:				100	pF
Minimum resistive load at HSOL and HSOR: R//			32		Ω
Maximum capacitor load at HSOL and HSOR: C//				100	pF
Differential minimum resistive load between SPKP and SPKN: R//	Output swing 4.38 V_{PP}		8		Ω
Differential maximum capacitor load between SPKP and SPKN: C//				100	pF
Common mode minimum resistive load at SPKP and SPKN			200		$k\Omega$
Common mode maximum capacitor load at SPKP and SPKN				10	pF
Maximum capacitor load at HSOVMID				100	pF
Capacitor load at AUVMID			4.7		μF
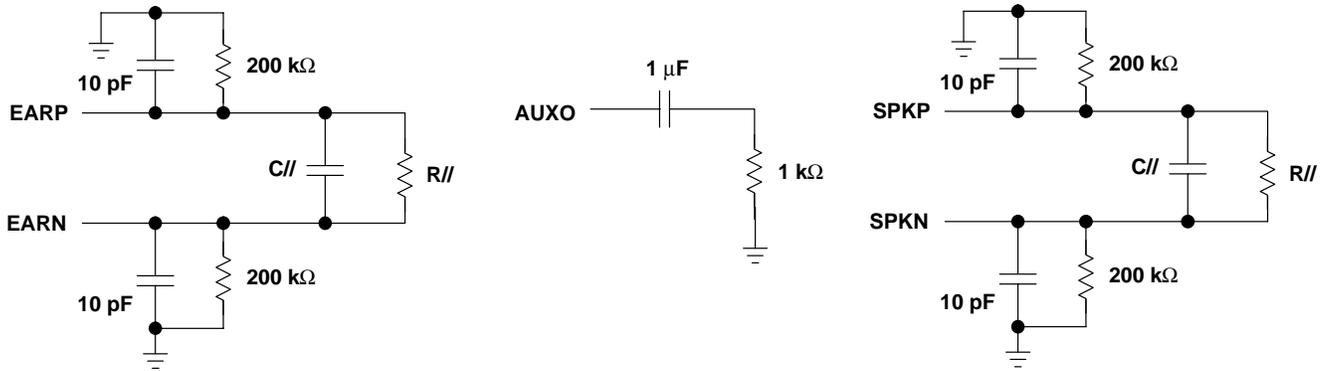
Figure 6−12. Audio Output Loading
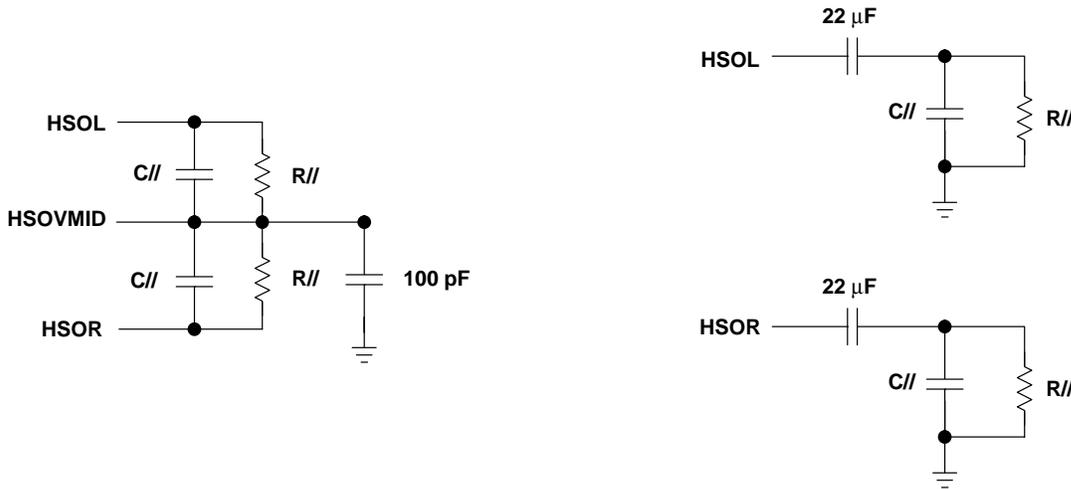
Figure 6−13. Stereo Headset Output Loading

Global characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Earphone maximum output swing at EARP–EARN	distortion ≤ 2% and 120 Ω, VSP input level = +3 dBm0	3.1	3.92		V_{PP}
	distortion ≤ 2% and 33 Ω, VSP input level = –5.34 dBm0	1.2	1.5		
	distortion ≤ 2% and 120 Ω, I2S input level = +3 dBm0	2.96	3.7		
Earphone amplifier gain			1		dB
Earphone amplifier state in power down			High Z		
Earphone amplifier power supply rejection	1 kHz, 100 mVpp		50		dB
Auxiliary output maximum output swing at AUXO	distortion ≤ 2% and 1 kΩ, VSP input level = +3 dBm0	1.6	1.96		V_{PP}
	distortion ≤ 2% and 1 kΩ, I2S input level = +3 dBm0	1.48	1.85		
Auxiliary output amplifier gain			–5		dB
AUXO amplifier state in power down			High Z		
AUXO amplifier power supply rejection	1 kHz, 100 mVpp		50		dB
Headphone maximum output swing at (HSOL/R)	distortion ≤ 2% and 32 Ω, VSP input level = +3 dBm0	1.6	1.96		V_{PP}
	distortion ≤ 2% and 32 Ω, I2S input level = +3 dBm0	1.48	1.85		
Headphone L/R amplifier gain			–5		dB
HSOL/R amplifier state in power down			High Z		
HSOL/R amplifier power supply rejection	1 kHz, 100 mVpp		50		dB
Speaker maximum output swing at SPKP–SPKN	distortion ≤ 2% and 8 Ω, VCCSPK = 3.2 V, Pout = 340 mW, SPKG = 0, VSP input level = +3 dBm0	3.73	4.66		V_{PP}
	distortion ≤ 0.5% and 8 Ω, VCCSPK = 3.2 V, Pout = 380 mW, SPKG = 1, VMIDSEL = 1, VSP input level = –2.5 dBm0	3.96	4.95		
	distortion ≤ 5% and 8 Ω, VCCSPK = 3.2 V, Pout = 430 mW, SPKG = 1, VMIDSEL = 1, VSP input level = –2 dBm0	4.2	5.24		
	distortion ≤ 2% and 8 Ω, VCCSPK = 3.2 v, SPKG = 0, I2S input level = +3 dBm0	3.52	4.4		
	distortion ≤ 0.5% and 8 Ω, VCCSPK = 3.2 v, SPKG = 1, VMIDSEL = 1, I2S input level = –2 dBm0	3.96	4.95		
Speaker amplifier gain	SPKG = 0		2.5		dB
	SPKG = 1		8.5		
Speaker amplifier state in power down			High Z		
Speaker amplifier power supply rejection	1 kHz, 100 mV$_{PP}$		80		dB
DC level at HSOVMID		1.2	1.35	1.5	V
DC level at AUVMID	VMIDSEL = 0		1.35		V
	VMIDSEL = 1		1.5		

6.18.1.4 Voiceband: Downlink Path

Volume Control Gain

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Default and reference	VOCTL code 010	–1	0	1	dB
	VOCTL code 110	–7	–6	–5	
	VOCTL code 000	–13	–12	–11	
	VOCTL code 100	–19	–18	–17	
	VOCTL code 011	–25	–24	–23	
Mute	VOCTL code 101, 001, 111			–40	dB

PGA Gain Step

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Default	VDLPGA code 0000	–6dB	–6.5	–6	–5.5	dB
	VDLPGA code 0001	–5dB	–5.5	–5	–4.5	
	VDLPGA code 0010	–4dB	–4.5	–4	–3.5	
	VDLPGA code 0011	–3dB	–3.5	–3	–2.5	
	VDLPGA code 0100	–2 dB	–2.5	–2	–1.5	
	VDLPGA code 0101	–1 dB	–1.5	–1	–0.5	
Reference	VDLPGA code 0110	0 dB	–0.5	0	0.5	dB
	VDLPGA code 0111	1 dB	0.5	1	1.5	
	VDLPGA code 1000	2 dB	1.5	2	2.5	
	VDLPGA code 1001	3 dB	2.5	3	3.5	
	VDLPGA code 1010	4 dB	3.5	4	4.5	
	VDLPGA code 1011	5 dB	4.5	5	5.5	
	VDLPGA code 1100	6 dB	5.5	6	6.5	
	Other cases		–6.5	–6	–5.5	

Sidetone Gain Step

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Reference	VDLST code 1101	–23 dB	–24	–23	–22	dB
	VDLST code 1100	–20 dB	–21	–20	–19	
	VDLST code 0110	–17 dB	–18	–17	–16	
	VDLST code 0010	–14 dB	–15	–14	–13	
	VDLST code 0111	–11 dB	–12	–11	–10	
	VDLST code 0011	–8 dB	–9	–8	–7	
	VDLST code 0000	–5 dB	–6	–5	–4	
	VDLST code 0100	–2 dB	–3	–2	–1	
	VDLST code 0001	1 dB	0	1	2	
	VDLST code 0101	1 dB	0	1	2	
	VDLST code 1000	Mute			–66	
	other cases	Mute			–66	

Frequency response 4-kHz bandwidth

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response relative to reference gain at 1 kHz	≤ 50 Hz			–10	dB
	50 Hz to 160 Hz			–3	
	300 Hz to 400 Hz	–2	0	1	
	400 Hz to 3300 Hz	–1	0	1	
	3300 Hz to 3400 Hz	–2	0	1	
	4000 Hz to 4600 Hz			–17	
	4600 Hz to 6000 Hz			–40	
	≥ 6000 Hz			–45	

Frequency response 8-kHz bandwidth (WBA = 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response relative to reference gain at 2.031 kHz	≤ 100 Hz			−11	dB
	200 Hz to 300 Hz			−3	
	300 Hz to 400 Hz	−7	0	+1	
	800 Hz to 1000 Hz	−3	0	+1	
	1400 Hz to 6600 Hz	−1	0	+1	
	6600 Hz to 6800 Hz	−2	0	+1	
	8000 Hz to 9200 Hz			−17	
	9200 Hz to 12000 Hz			−40	
	≥ 12000 Hz			−45	

Psophometric TSNR 4-kHz and 8-kHz bandwidth

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Psophometric TSNR (harmonic distortion + SNR) 1.015-kHz or 2.031-kHz tone (WBA = 1) Measured at: EARP–EARN, AUXO, SPKP–SPKN @ 2.5 dB	3 dBm0 (maximum digital code)	35			dB
	0 dBm0	45			
	−5 dBm0	52			
	−10 dBm0	57			
	−20 dBm0	54			
	−30 dBm0	52			
	−40 dBm0	42			
	−50 dBm0	32			
Maximum idle channel noise				−86	dBm0
Crosstalk with the uplink path				−66	dB

Gain characteristics 4kHz and 8kHz bandwidth

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Absolute gain error 1.015-kHz or 2.031-kHz tone (WBA = 1)	At 0 dBm0	−1	0	1	dB
	At 0 dBm0, HPFBYP = 1	0	1	2	
	At −10 dBm0	−11	−10	−9	
Gain tracking error	3 dBm0	−0.25		0.25	dB
	0 dBm0	−0.25		0.25	
	−5 dBm0	−0.25		0.25	
	−10 dBm0 (reference)		0		
	−20 dBm0	−0.25		0.25	
	−30 dBm0	−0.25		0.25	
	−40 dBm0	−0.35		0.35	
	−50 dBm0	−0.50		0.50	
Number of meaningful output bits	PGA and VOCTL set to 0 dB		15		Bit

6.18.1.5 Audio Stereo Path

Right/Left Audio Volume Control Gain Step

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Right and left gain	AUGA = 1, AULGA/AURGA = 00000	+5.5	+6	+6.5	dB
Default and reference	AUGA = 0, AULGA/AURGA = 00000	–0.5	0	0.5	dB
Right or left gain	AUGA = 0, AULGA/AURGA = 00001	–1.5	–1	–0.5	dB
	AUGA = 0, AULGA/AURGA = 00010	–2.5	–2	–1.5	
	AUGA = 0, AULGA/AURGA = 00011	–3.5	–3	–2.5	
	AUGA = 0, AULGA/AURGA = 00100	–4.5	–4	–3.5	
	AUGA = 0, AULGA/AURGA = 00101	–5.5	–5	–.5	
	AUGA = 0, AULGA/AURGA = 00110	–6.5	–6	–5.5	
	AUGA = 0, AULGA/AURGA = 00111	–6.5	–7	–7.5	
	AUGA = 0, AULGA/AURGA = 01000	–7.5	–8	–8.5	
	AUGA = 0, AULGA/AURGA = 01001	–8.5	–9	–9.5	
	AUGA = 0, AULGA/AURGA = 01010	–9.5	–10	–10.5	
	AUGA = 0, AULGA/AURGA = 01011	–10.5	–11	–11.5	
	AUGA = 0, AULGA/AURGA = 11101	–28.5	–29	29.5	
	AUGA = 0, AULGA/AURGA = 11110	–29.5	–30	–30.5	
Right or left mute	AUGA = 0, AULGA/AURGA = 11111			–40	dB

Frequency response (relative to reference gain at 1 kHz)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband			0.42*Fs [†]		Hz
Passband gain	In region 0 to 0.42*Fs	–1		1	dB
Stopband			0.65*Fs		Hz
Stopband attenuation	In region 0.65*Fs to 8*Fs	60	75		dB
Group delay			12.625/Fs		μs
–3-dB attenuation		0.47*Fs	0.48*Fs	0.49*Fs	Hz

[†] Fs is the sampling frequency (8, 11.025, 16, 22.05, 32, 44.1, 48 kHz).

Audiometric TSNR

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audiometric TSNR (harmonic distortion + SNR) (Note 9) 1.015-kHz tone measured at: HSOL/R	3 dBm0, Fs = 44.1 kHz, BW: 20 Hz–20 kHz	35			dB
	0 dBm0, Fs = 44.1 kHz, BW: 20 Hz–20 kHz	45			
	–5 dBm0	52			
	–10 dBm0	57			
	–20 dBm0	55			
	–30 dBm0	45			
	–40 dBm0	35			
	–50 dBm0	25			
Maximum idle channel noise (Note 9)			–84	–78	dBm0
Intermodulation distortion	At 0 dBm0 and 1 kHz			–60	dB
Inband spurious	At 0 dBm0 and 1 kHz, 300 to 0.4*Fs			–50	dB

NOTE 9: All performance measurements done with an Audiometric filter (A-weighted filter). Failure to use such a filter results in higher THD+N and lower SNR and dynamic range readings than shown in the electrical characteristics. The Audiometric filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Gain characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Absolute gain error	At 0 dBm0 and 1 kHz	−1	0	1	dB
	At −10 dBm0 and 1 kHz	−11	−10	−9	
L/R gain mismatch	At 0 dBm0 and 1 kHz, gain setting @ 0 dB	−1	0.2	1	dB
Gain tracking error	3 dBm0	−0.25		0.25	dB
	0 dBm0	−0.25		0.25	
	−5 dBm0	−0.25		0.25	
	−10 dBm0 (reference)		0		
	−20 dBm0	−0.25		0.25	
	−30 dBm0	−0.25		0.25	
	−40 dBm0	−0.35		0.35	
	−50 dBm0	−0.50		0.50	
Number of meaningful output bits	AUGA = 0, AULGA/AURGA = 00000, Fs = 44.1 kHz		14.5		Bit

6.18.2 Baseband Uplink General Characteristics

6.18.2.1 Baseband Uplink Path

dc characteristics

Output load is 10 kΩ in parallel with 47 pF from the BULIP terminal to the BULIN terminal and from the BULQP terminal to the BULQN terminal, and 50 kΩ in parallel with 10 pF on the BULIP, BULIN, BULQP, and BULQN terminals to the GNDA terminal.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I and Q DAC resolution			10		bit
Voltage reference BBVREF[†]			1.75		V
Dynamic range on each output	Centered on VVMID		1.75		V_{PP}
Differential output dynamic range between BULIP and BULIM or between BULQP and BULQM	OUTLEV(0:2) = 000	3.1	3.5	3.9	V_{PP}
	OUTLEV(0:2) = 010	2.3	2.56	2.9	
	OUTLEV(0:2) = 100	1.66	1.86	2.1	
	OUTLEV(0:2) = 110	0.83	0.93	1.05	
	OUTLEV(0:2) = X01		2.10		
	OUTLEV(0:2) = X11		2.33		
Output common mode voltage VVMID	SELMID(0:2) = 000	VRABB/2 − 5%	VRABB/2	VRABB/2 + 5%	V
	SELMID(0:2) = 100	1.30	1.35	1.40	
	SELMID(0:2) = 010	1.40	1.45	1.50	
	SELMID(0:2) = XX1	1.20	1.25	1.30	
	SELMID(0:2) = 110	1.12	1.180	1.25	
Offset error before calibration		−100		100	mV
Offset error after calibration		−10		10	mV
I and Q output state in power down			High Z		

[†] Internal reference

ac characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Absolute gain error relative to V_{VREF}	Measured on 67.7 kHz sine wave	−1		1	dB
Gain matching between channels I and Q	Measured on 67.7 kHz	−0.3	0.0	0.3	dB
GMSK modulation spectrum mask. Measured by average of FFTs on random modulated bursts using a flat-top window with 30-kHz bandwidth	100 kHz			0.5	dBc
	200 kHz			−34	
	250 kHz			−37	
	400 kHz			−65	
	600 kHz			−72	
	800 kHz			−72	
GMSK phase trajectory error				6	°Peak
				1.5	°Rms

Timing characteristics: these values are given for system information only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SU1}	Setup time, BULON ↑ to BULCAL ↑		15			µs
t_{W1}	Pulse duration BULCAL high		144			1/4-bit†
t_{SU2}	Setup time, BULCAL ↓ to BULENA ↑		0			1/4-bit†
t_{W2A}	Pulse duration BULENA high for GMSK	N effective duration of burst		N − 32		1/4-bit†
t_{H1A}	Modulation hold time after BULENA ↓			32		1/4-bit†
t_{H1B}	Modulation hold time after BULENA ↓			96		1/4-bit†
t_{H2A}	Hold time BULON after BULENA ↓		32			1/4-bit†
t_{H2B}	Hold time BULON after BULENA ↓		96			1/4-bit†
t_{D1}	Modulator input to output delay	From BULENA ↑ to mid of 1st bit		2.5		1/4-bit†

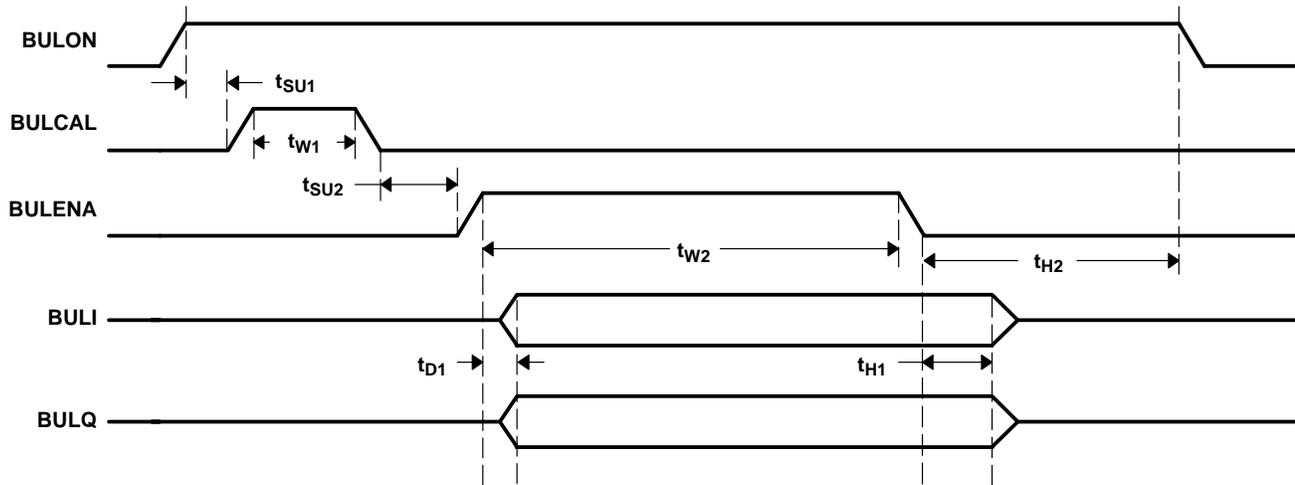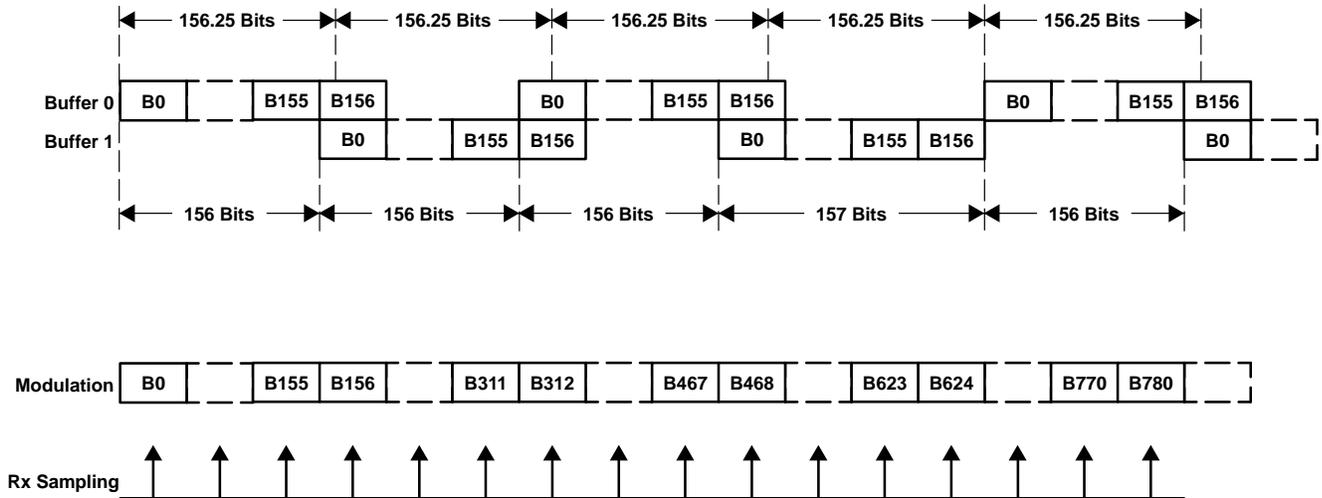† Bit is relative to GSM bit = 1/270.833 kHz.

Figure 6–14. Baseband Uplink Timing

NOTE: B0 and B156 are guard bits

Figure 6–15. GSMK Multislot Modulation Timing Scheme

6.18.2.2 Baseband Downlink Path

dc characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic range on each input			BBVREF		V_{PP}
Differential input maximum dynamic range	BDLIP – BDLIM or BDLQP – BDLQM		2 BBVREF		V_{PP}
Differential input linear dynamic range[†]	BDLIP – BDLIM or BDLQP – BDLQM		2.42		V_{PP}
Differential input resistance	BDLIP – BDLIM or BDLQP – BDLQM	130	200	270	$k\Omega$
Differential input capacitance	BDLIP – BDLIM or BDLQP – BDLQM		4		pF
Single ended input resistance to ground	BDLIP or BDLIM or BDLQP or BDLQM	70	110	150	$k\Omega$
Single ended input capacitance to ground			8		pF
External input common mode voltage		0.8	VRABB/2	1.9	V
Range of digital ouput data samples		–32768		32767	
Offset error before calibration		–812		812	LSB[‡]
Offset error after calibration	Internal calibration	–140		140	LSB[‡]
	External calibration	–140		140	
Offset error external calibration range		–0.5		0.5	V
I and Q input state in power down			High Z		

[†] Digital output code is given by $\pm 47385 * (V_{BDLIP} - V_{BDLIM})/2BBVREF$ in the linear dynamic range, outside this range digital output code is given by ± 32768.

[‡] LSB of the 16-bit word format transmitted through the BSP. The analog equivalent step at the input of the baseband downlink is 36.9 μV (using BBVREF/47385).

ac characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain matching between channels	Measured on 18 kHz	−0.5	0.0	0.5	dB
Delay matching between channels	sine wave	−16	0.0	16	ns
Frequency response of the total downlink path with values related to 18 kHz	800 Hz	0.0		0.35	dB
	18 kHz (reference)		0.0		
	35 kHz	−0.40		0.25	
	59 kHz	−0.40		0.30	
	68 kHz	−0.70		0.30	
	81 kHz	−3.00		0.00	
	97 kHz	−6.00		−3.0	
	110 kHz			−8.0	
	120 kHz			−15.0	
	135 kHz			−35	
	200 kHz			−45	
	>200 kHz			−45	
Signal–to–noise ratio on 200-kHz bandwidth	−50 dBm0	32			dB
	−40 dBm0	42			
	−30 dBm0	52			
	−20 dBm0	62			
	−10 dBm0	72			
	−6 dBm0	72			
Idle channel noise 0 to 200 kHz				−82	dBm0
Gain tracking error at 18 kHz with reference at −10 dBm	−6 dBm0	−0.25		0.25	dB
	−10 dBm0 (reference)		0		
	−20 dBm0	−0.25		0.25	
	−30 dBm0	−0.25		0.25	
	−40 dBm0	−0.25		0.25	
	−50 dBm0	−0.50		0.50	
Group delay when GMSK FIR filter is selected	0 Hz to 100 kHz		32.3		µs

NOTE: The maximum digital output code 32767 corresponds to −3.2 dBm GMSK input signal (GSM). For higher value of the input signal the 16-bit output code is maintained at 32767.

Timing characteristics: these values are given for system information only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SU3}	Setup time, BDLON ↑ to BDLCAL ↑		5			µs
t_{W3}	Pulse duration BDLCAL high		60			µs
t_{SU4}	Setup time, BDLCAL ↓ to BDLENA ↑		1			µs
t_{W4}	Pulse duration BDLENA high	N effective duration of burst		N		1/4-bit[†]
t_{D2}	Setup time after BDLENA ↑ before DATA valid				32.7	µs
t_{H3}	Hold time DATA valid after BDLENA ↓				3.7	µs
t_{H4}	Hold time BDLON high after BDLENA ↓		3.7			µs

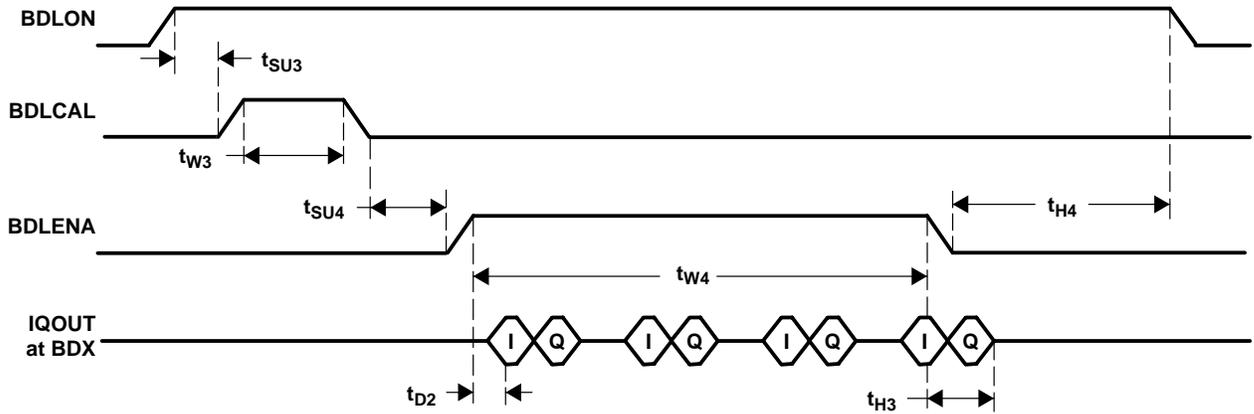† Bit is relative to GSM bit = 1/270.833 kHz.

Figure 6–16. Baseband Downlink Timing

6.18.3 Auxiliary DAC

6.18.3.1 10-Bit DAC Characteristics

The recommended load on terminal D9 (DAC) is a 50-pF capacitor (maximum value) in parallel with a 10-kΩ resistor (minimum value).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC resolution			10		bit
Integral nonlinearity	Best fitting line	−1		+1	LSB
Differential nonlinearity		−1		+1	LSB
Settling time	From code maximum to code minimum, or from code minimum to code maximum		10		μs
Output voltage with code maximum		2.0	2.2	2.4	V
Output voltage with code minimum		0.18	0.24	0.3	V
Output voltage in power down			0	50	mV
Output impedance in power down			200		Ω
DC power supply sensitivity			1		%

6.18.4 Automatic Frequency Control

6.18.4.1 AFC DAC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC resolution			13		bit
Sampling frequency	AFCCTLADD reg = 00		4.33		MHz
	AFCCTLADD reg = 01		2.16		
	AFCCTLADD reg = 10		1.082		
	AFCCTLADD reg = 11		540		kHz
LSB value		250		340	μV
DC power supply sensitivity			1		%

6.18.4.2 AFC Output Stage

The recommended load on terminal C12 (AFC) is a 33-nF capacitor.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage at code minimum				45	mV
Output voltage at code maximum		2.0	2.4	2.8	V
Output voltage in power down			0	50	mV
Output resistance		15.6	22.5	29	kΩ
Settling time	C_L = 33 nF		10		ms

6.19 ESD Performance

The TWL3016 device meets Texas Instruments standard requirements relative to the electrostatic discharge (ESD) sensitivity.

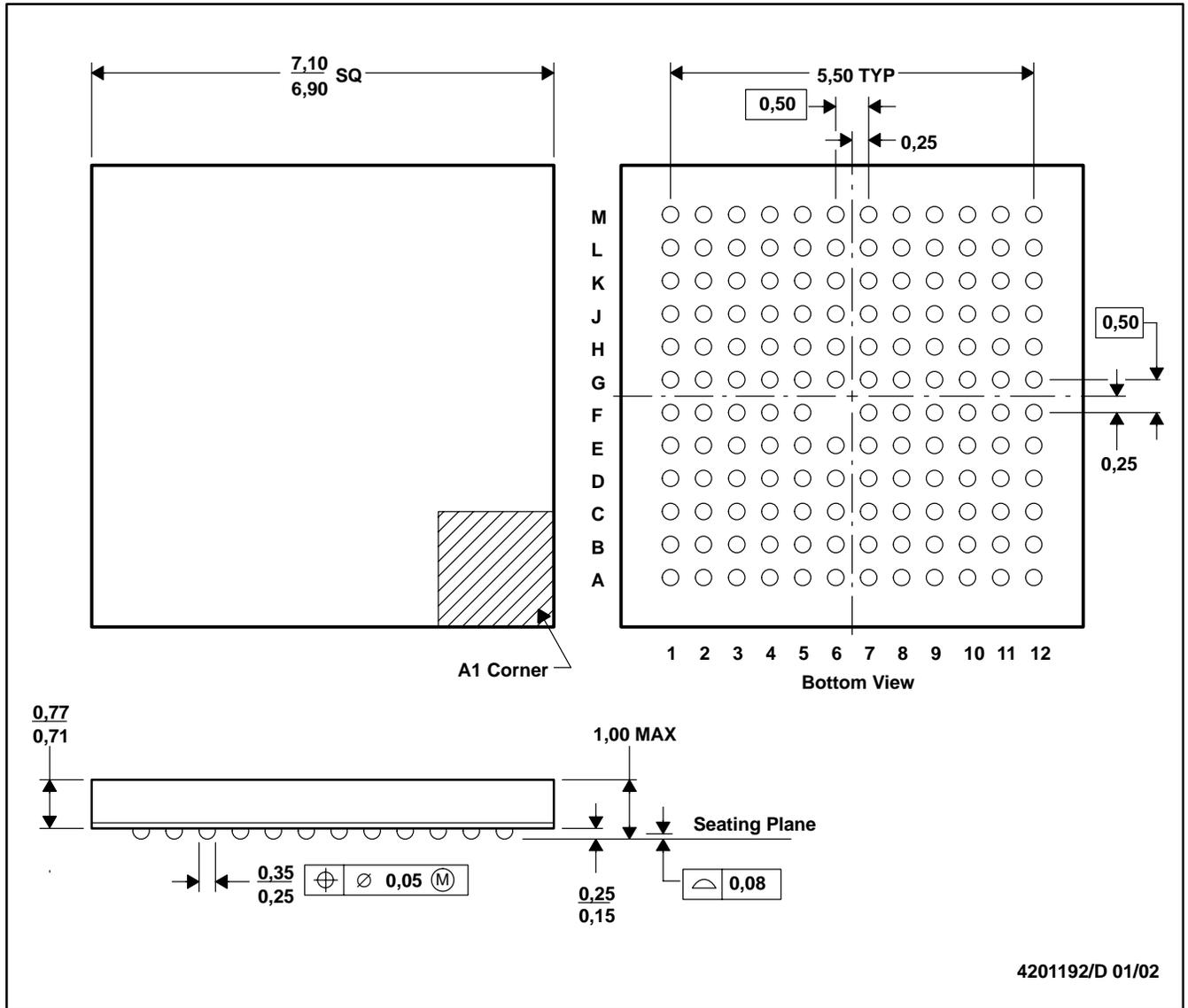The following list details the TWL3016 ESD performance relative to TI requirements:

ESD METHOD	STANDARD REFERENCE	TWL3016 PERFORMANCE	TI STANDARD REQUIREMENTS
Human body model	EIA/JEDEC22–A114–A	2000 V	2000 V
Machine model	EIA/JEDEC22–A115–A	100 V	None
Charge device model	EIA/JEDEC22–C101–A	750 V	500 V

7 Mechanical Information

The TWL3016 device is packaged in a 143-terminal GQW package. The following shows the mechanical dimensions for the GQW package.

GQW (S-PBGA-N143) **PLASTIC BALL GRID ARRAY**

7,10 / 6,90 SQ

5,50 TYP

0,50

0,25

0,50

0,25

M L K J H G F E D C B A

1 2 3 4 5 6 7 8 9 10 11 12

Bottom View

A1 Corner

0,77 / 0,71

1,00 MAX

Seating Plane

0,35 / 0,25 ⊕ ⌀ 0,05 Ⓜ

0,25 / 0,15 ◠ 0,08

4201192/D 01/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO-225

MicroStar Junior is a trademark of Texas Instruments.