

General Description

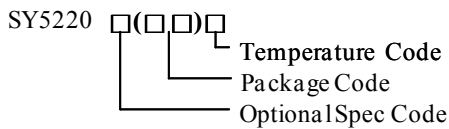
SY5220 is a high-performance controller and driver for standard and logic-level N-channel MOSFET power devices used for low-voltage secondary-side synchronous rectification.

This solution not only directly reduces power dissipation of the rectifier but also indirectly reduces primary-side losses as well, due to compounding of efficiency gains.

The Dsen pin of SY5220 can support 60V voltage stress.

SY5220 will achieve ultra-low power consumption when the circuit operates in no load.

Ordering Information



Ordering Number	Package type	Note
SY5220ABC	SOT23-6	----

Features

- Gate amplitude control technology
- Secondary-Side Controller Optimized for 5V~20V Systems
- Awaken function to cooperate with SY5004 for excellent load regulation.
- Suitable for Discontinuous Mode (DCM), Critical Conduction Mode (CrCM), Continuous Mode (CCM)
- Suitable for Primary side control(PSR), secondary side control(SSR)
- Compact package:SOT23-6

Applications

- AC/DC Adapters
- Battery Chargers
- Consumer Electronics
- Auxiliary power supplies

Typical Application

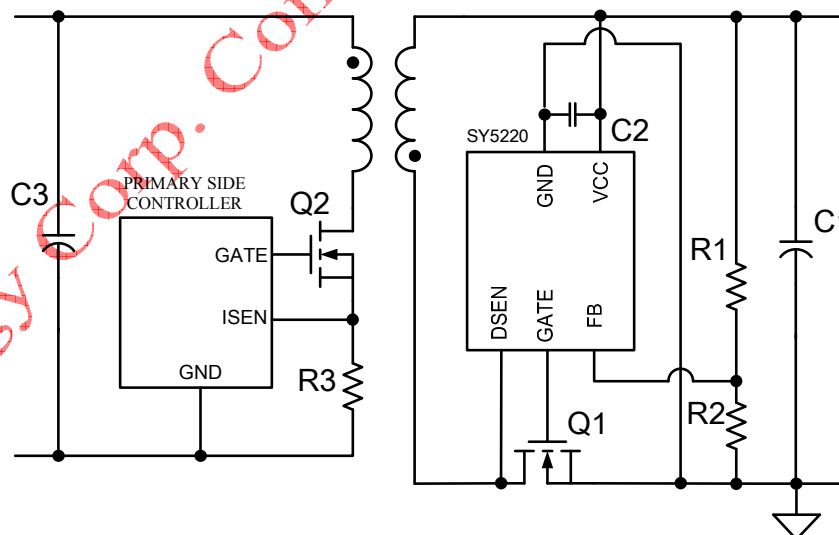


Fig.1a Rectification in 5V~7V

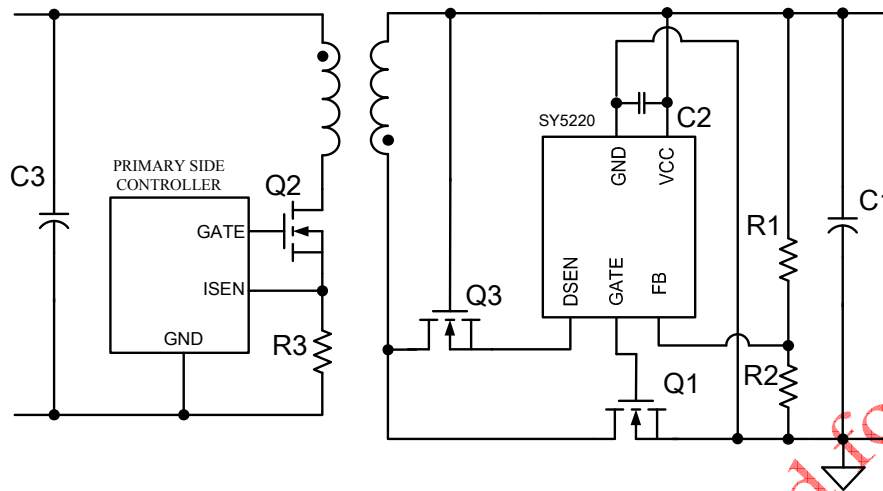
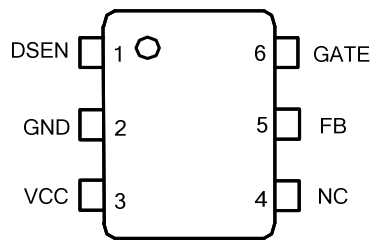


Fig.1b Rectification in 7V~20V

Silergy Corp. Confidential Prepared for PST

Pinout (top view)



SOT23-6

Top Mark: Nrxyz (device code:Nr, x=year code, y=week code, z=lot number code)

Pin number	Pin Name	Pin Description
1	DSEN	This pin connects directly to the synchronous MOSFET Drain terminal.
2	GND	Connect to the synchronous MOSFET Source terminal. And connect a 0.1μF or larger ceramic bypass capacitor from the VCC pin to the GND pin through very short board tracks.
3	VCC	This is the power supply pin. It is recommended to decouple this point to ground closely with a ceramic capacitor.
4	NC	Not connect
5	FB	Output Voltage Detection Pin. This pin is connected to the output with an external resistor divider to detect the output voltage.
6	GATE	Connect GATE to the gate of the controlled MOSFET through a short board tracks to achieve optimal switching performance.

Block Diagram

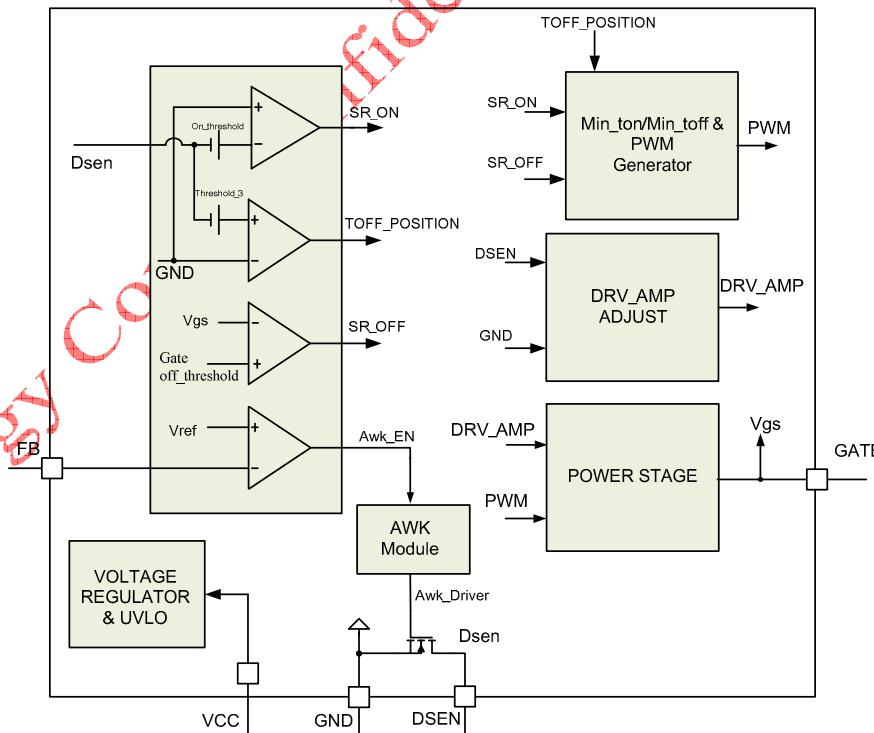


Fig.2 Block Diagram



Absolute Maximum Ratings

VCC	-0.3V~30V
GATE	-0.3V~20V
FB	-0.3V~30V
DSEN	-1V~60V
Supply Current I _{VCC}	20mA
Power Dissipation, @ T _A = 25°C SOT23-6	0.6W
Package Thermal Resistance	
SOT23-6, θ _{JA}	170°C/W
SOT23-6, θ _{JC}	130°C/W
Temperature Range	-40°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C

Recommended Operating Conditions

V _{IN}	5V~15V
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 105°C

Silergy Corp. Confidential Prepared for POST



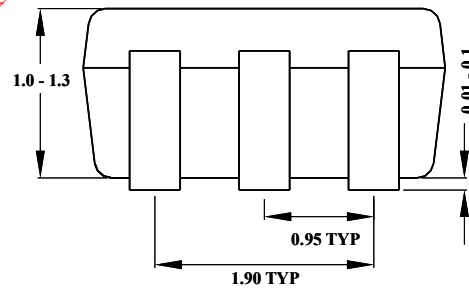
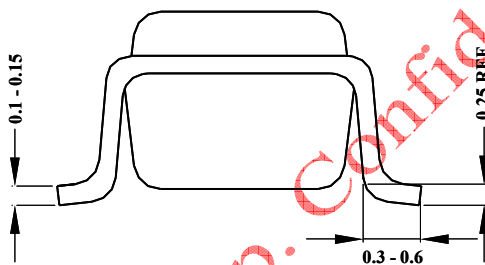
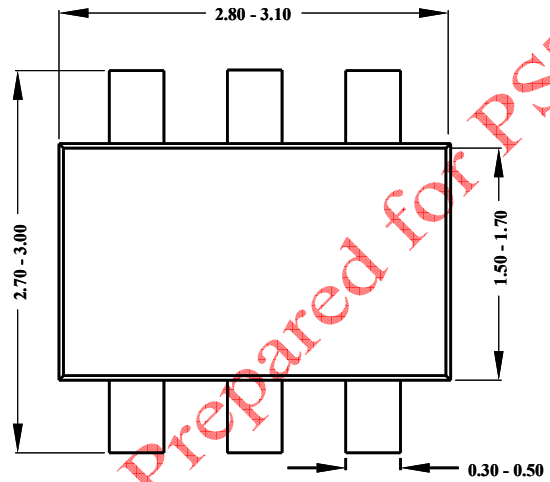
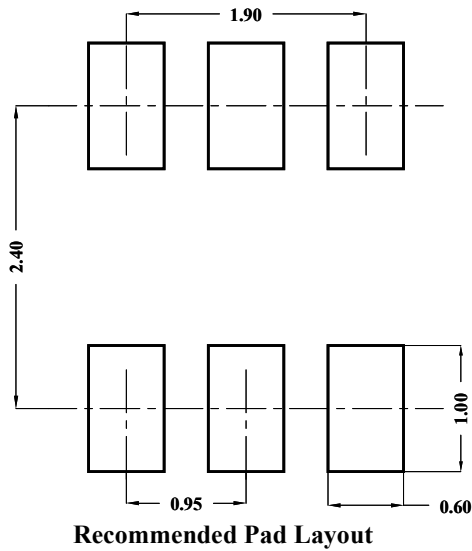
Electrical Characteristics

(V_{VCC} = 12V , T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VCC turn-on threshold	V _{VCC,ON}		3.68	3.77	3.86	V
Hysteresis Voltage	V _{Hysteresis}		95	117	140	mV
Quiescent Current		With awaken function		125		uA
Threshold Section						
On_threshold			-250	-210	-170	mV
Control_threshold			-45	-35	-25	mV
Gate_off_threshold			1.45	1.5	1.55	V
Position_threshold				1		V
FB_Reference	Vref		1.1	1.125	1.15	V
Min_Ton/ Min_Toff section						
Min Ton	ON_BLANK		500	700	900	ns
Min Ton(CCM inflection)				2100		ns
Min Toff	POSITION_BLANK		1785	2100	2415	ns
Gate Driver Section						
Max. source current	I _{SOURCE,max.}			0.8		A
Max. sink current	I _{SINK,max.}			3		A
Turn on Propagation delay	td1			40		ns
Turn off Propagation delay	td2			20		ns

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause perm anent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SOT23-6 Package outline & PCB layout design



Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.