TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOSVI)

SSM3J332R

Power Management Switch Applications

Unit: mm

•	1	.8-	V	dı	ri۱	ıe
•		.0-	v	u	ı١١	/ $\overline{}$

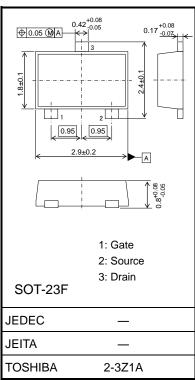
• Low ON-resistance: RDS(ON) = $144 \text{ m}\Omega$ (max) (@VGS = -1.8 V)

RDS(ON) = 72.0 mΩ (max) (@VGS = -2.5 V) RDS(ON) = 50.0 mΩ (max) (@VGS = -4.5 V) RDS(ON) = 42.0 mΩ (max) (@VGS = -10 V)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol		Rating	Unit	
Drain-Source voltage		VDSS		-30	V	
Gate-Source voltage		Vgss		± 12	V	
Drain current	DC	ID ((Note 1)	-6.0	^	
Diain current	Pulse	IDP (Note 1,2) -2		-24.0	Α	
Power dissipation		P _D (Note 3)		1	W	
			t < 10s	2	VV	
Channel temperature		T _{ch}		150	°C	
Storage temperature range		T _{stg}		-55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.



Weight: 11 mg (typ.)

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The channel temperature should not exceed 150°C during use.

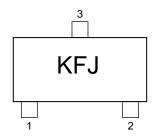
Note 2: PW \leq 1ms, Duty \leq 1%

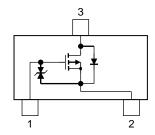
Note 3: Mounted on FR4 board.

 $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}, \text{ Cu Pad: } 645 \text{ mm}^2)$

Marking

Equivalent Circuit (Top View)





Start of commercial production 2010-08

Electrical Characteristics (Ta = 25°C)

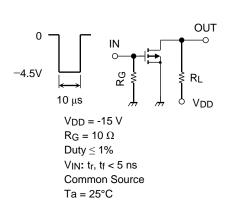
Characteristic		Symbol	Test Conditions		Min	Тур.	Max	Unit
Drain-Source breakdown voltage		V (BR) DSS	ID = -10 mA, VGS = 0 V		-30	_	_	V
		V (BR) DSX	I _D = -10 mA, V _{GS} = 8 V	(Note 5)	-22	_	_	V
Drain cut-off current		IDSS	V _{DS} = -30 V, V _{GS} = 0 V		_	_	-1	μΑ
Gate leakage current		Igss	VGS = ±10 V, VDS = 0 V		_	_	±1	μΑ
Gate threshold voltage		V _{th}	V _{DS} = -3 V, I _D = -1 mA		-0.5	_	-1.2	V
Forward transfer admittance		Y _{fs}	V _{DS} = -3 V, I _D = -2.5 A	(Note 4)	5.7	11.3	_	S
Drain-source ON-resistance			ID = -5.0 A, VGS = -10 V	(Note 4)	_	36.0	42.0	mΩ
		D	ID = -4.0 A, VGS = -4.5 V	(Note 4)	_	42.5	50.0	
		RDS (ON)	I _D = -2.5 A, V _{GS} = -2.5 V	(Note 4)	_	57.5	72.0	
			I _D = -0.5 A, V _G S = -1.8 V	(Note 4)	_	76.5	144	
Input capacitance		Ciss	V 45.V.V 0.V		_	560	_	
Output capacitance		Coss	—— f = 1 MHz		_	80	_	pF
Reverse transfer capacitance		Crss			_	65	_	
Switching time	Turn-on time	ton	V _{DD} = -15 V, I _D = -2.0 A		_	15	_	ns
	Turn-off time	t _{off}	$V_{GS} = 0$ to -4.5 V, $R_{G} = 10 \Omega$		_	75	_	
Total Gate Charge		Qg	V 45.V 1 0.0 A		_	8.2	_	nC
Gate-Source Charge		Q _{gs1}	$V_{DD} = -15 \text{ V}, I_{D} = -6.0 \text{ A},$		_	1.1	_	
Gate-Drain Charge		Q _{gd}	$V_{GS} = -4.5 \text{ V}$		_	2.2	_	
Drain-Source forward voltage		V _{DSF}	I _D = 6.0 A, V _{GS} = 0 V	(Note 4)	_	0.90	1.2	V

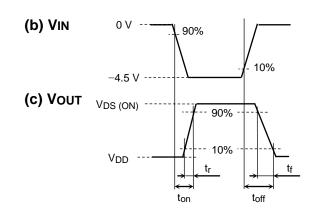
Note4: Pulse test

Note5: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit

(a) Test Circuit





Notice on Usage

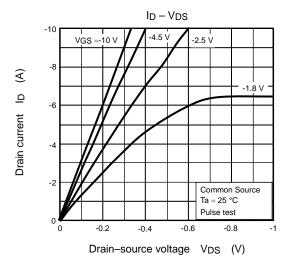
Let V_{th} be the voltage applied between gate and source that causes the drain current (ID) to be low (-1 mA for the SSM3J332R). Then, for normal switching operation, VGS(on) must be higher than V_{th} , and VGS(off) must be lower than V_{th} . This relationship can be expressed as: $VGS(off) < V_{th} < VGS(on)$.

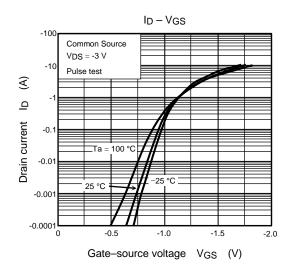
Take this into consideration when using the device.

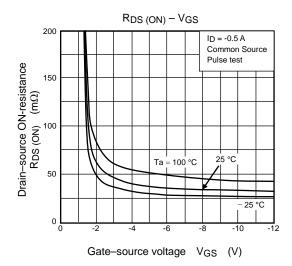
Handling Precaution

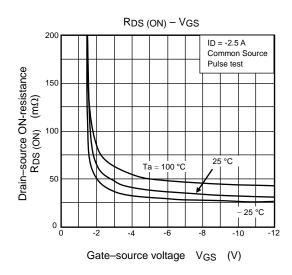
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

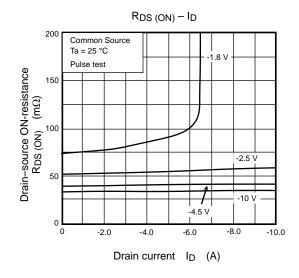
Thermal resistance Rth (ch-a) and power dissipation PD vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

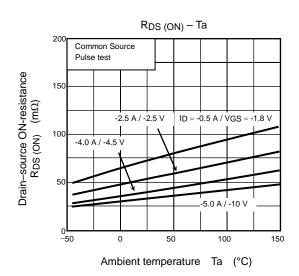




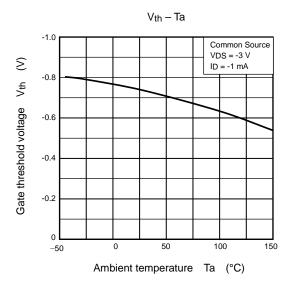


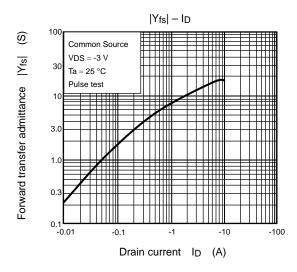


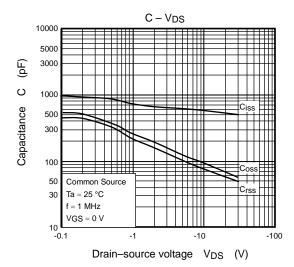


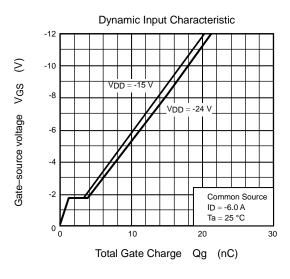


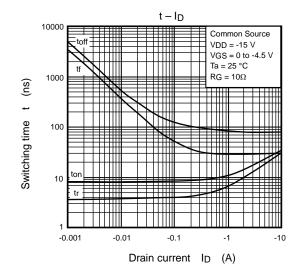
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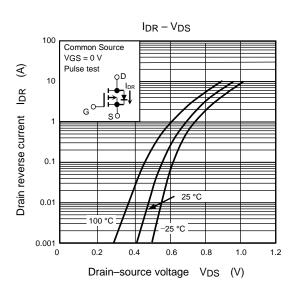




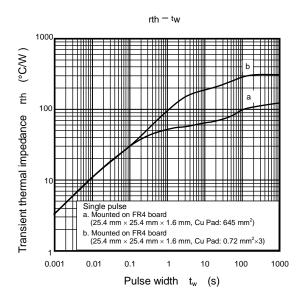


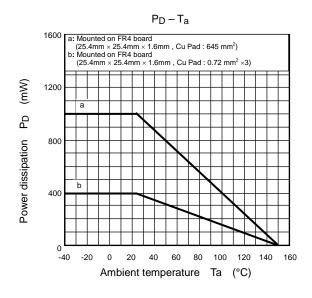


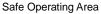


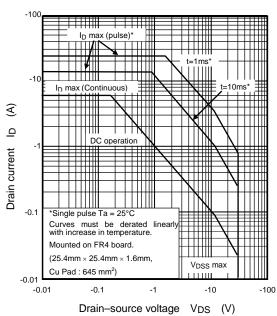


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