

SN65HVD7x 3.3-V Supply RS-485 With IEC ESD Protection

1 Features

- Small-size VSSOP Packages Save Board Space, or SOIC for Drop-in Compatibility
- Bus I/O Protection
 - $> \pm 15$ kV HBM Protection
 - $> \pm 12$ kV IEC 61000-4-2 Contact Discharge
 - $> \pm 4$ kV IEC 61000-4-4 Fast Transient Burst
- Extended Industrial Temperature Range
–40°C to 125°C
- Large Receiver Hysteresis (80 mV) for Noise Rejection
- Low Unit-Loading Allows Over 200 Connected Nodes
- Low Power Consumption
 - Low Standby Supply Current: $< 2 \mu\text{A}$
 - $I_{\text{CC}} < 1 \text{ mA}$ Quiescent During Operation
- 5-V Tolerant Logic Inputs Compatible With 3.3-V or 5-V Controllers
- Signaling Rate Options Optimized for: 250 kbps, 20 Mbps, 50 Mbps
- Glitch Free Power-Up and Power-Down Bus Inputs and Outputs

2 Applications

- Factory Automation
- Telecommunications Infrastructure
- Motion Control

3 Description

These devices have robust 3.3-V drivers and receivers in a small package for demanding industrial applications. The bus pins are robust to ESD events with high levels of protection to Human-Body Model and IEC Contact Discharge specifications.

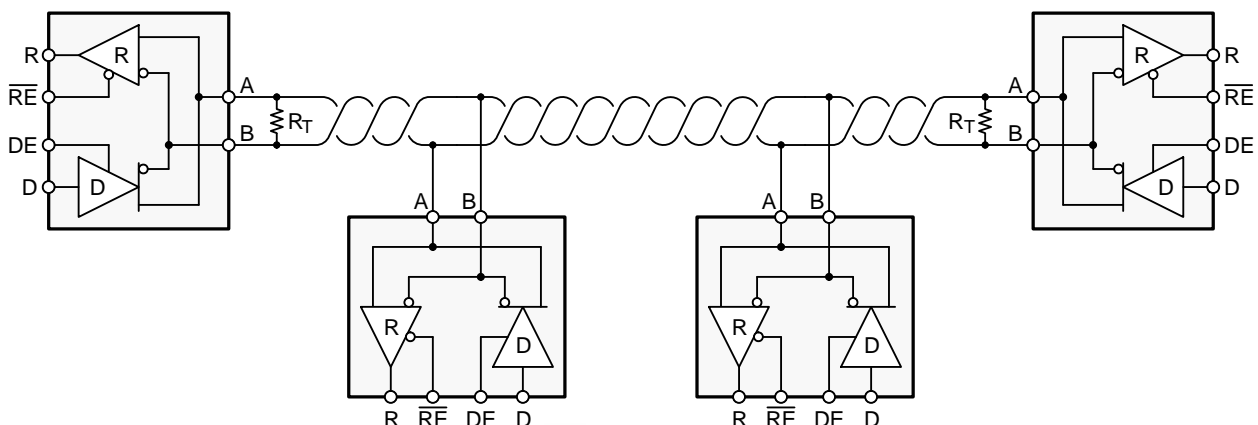
Each of these devices combines a differential driver and a differential receiver which operate from a single 3.3-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. These devices feature a wide common-mode voltage range making the devices suitable for multi-point applications over long cable runs. These devices are characterized from –40°C to 125°C.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD72, SN65HVD75, SN65HVD78	SOIC (8)	4.91 mm x 3.90 mm
	VSSOP (8)	3.00 mm x 3.00 mm
	VSON (8)	

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



Copyright © 2016, Texas Instruments Incorporated



Table of Contents

1 Features	1	9.1 Overview	15
2 Applications	1	9.2 Functional Block Diagram	15
3 Description	1	9.3 Feature Description	15
4 Revision History	2	9.4 Device Functional Modes	15
5 Device Comparison Table	4	10 Application and Implementation	17
6 Pin Configuration and Functions	4	10.1 Application Information	17
7 Specifications	5	10.2 Typical Application	18
7.1 Absolute Maximum Ratings	5	11 Power Supply Recommendations	24
7.2 ESD Ratings	5	12 Layout	25
7.3 Recommended Operating Conditions	5	12.1 Layout Guidelines	25
7.4 Thermal Information	6	12.2 Layout Example	25
7.5 Electrical Characteristics	6	13 Device and Documentation Support	26
7.6 Power Dissipation	7	13.1 Device Support	26
7.7 Switching Characteristics: 250 kbps Device (SN65HVD72) Bit Time $\geq 4 \mu\text{s}$	7	13.2 Documentation Support	26
7.8 Switching Characteristics: 20 Mbps Device (SN65HVD75) Bit Time $\geq 50 \text{ ns}$	8	13.3 Related Links	26
7.9 Switching Characteristics: 50 Mbps Device (SN65HVD78) Bit Time $\geq 20 \text{ ns}$	8	13.4 Community Resources	26
7.10 Typical Characteristics	9	13.5 Trademarks	26
8 Parameter Measurement Information	11	13.6 Electrostatic Discharge Caution	26
9 Detailed Description	15	13.7 Glossary	26
		14 Mechanical, Packaging, and Orderable Information	27

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (September 2016) to Revision F	Page
• Changed pin A From: 7 To: 6, and pin B From: 6 To: 7 in Figure 26	22

Changes from Revision D (July 2015) to Revision E	Page
• Added new Feature: Glitch Free Power-Up and Power-Down Bus Inputs and Outputs	1

Changes from Revision C (September 2013) to Revision D	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

Changes from Revision B (June 2012) to Revision C	Page
• Deleted Feature: > ±12kV IEC61000-4-2 Air-Gap Discharge	1
• Added Footnote 2 to the Absolute Maximum Ratings table	5
• Changed the Switching Characteristics conditions statement From: 250 kbps devices (SN65HVD70, 71, 72) bit time > 4 μs To: 250 kbps device (SN65HVD72) bit time ≥ 4 μs	7
• Changed the Switching Characteristics conditions statement From: 250 kbps devices (SN65HVD73, 74, 75) bit time > 50 ns To: 250 kbps device (SN65HVD75) bit time ≥ 50 ns	8
• Changed the Switching Characteristics conditions statement From: 250 kbps devices (SN65HVD76, 77, 78) bit time > 20 ns To: 250 kbps device (SN65HVD78) bit time ≥ 20 ns	8
• Added note : $R_L = 54 \Omega$ to Figure 6 , Figure 7 , and Figure 8	9
• Added the DGK package to the SN65HVD72, 75, 78 Logic Diagram	15
• Replaced the LOW-POWER STANDBY MODE section	19
• Added text to the Transient Protection section.....	20

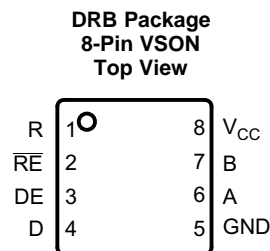
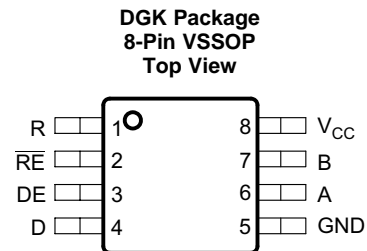
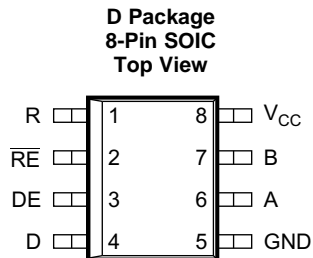
Changes from Revision A (May 2012) to Revision B	Page
• Added the SON-8 package and Nodes column to Device Comparison Table ,.....	4
• Changed the Voltage range at A or B Inputs MIN value From: –8 V To: –13 V	5
• Added footnote for free-air temperature to the Recommended Operating Conditions table.....	5
• Changed the Bus input current (disabled driver) TYP values for HVD78 $V_I = 12 V$ From: 150 To: 240 and $V_I = -7 V$ From: –120 To: –180	7
• Changed, Thermal Information	7
• Changed, Thermal Characteristics	7
• Added TYP values to the Switching Characteristics table.....	8
• Added TYP values to the Switching Characteristics table.....	8
• Changed the SN65HVD72, 75, 78 Logic Diagram	15
• Added section: LOW-POWER STANDBY MODE	19

Changes from Original (March 2012) to Revision A	Page
• Added VALUEs to the Thermal Characteristics table in the DEVICE INFORMATION section.	7
• Changed the Switching Characteristics condition statement From: 15 kbps devices (SN65HVD73, 74, 75) bit time > 65 ns To: 20 Mbps devices (SN65HVD73, 74, 75) bit time > 50 ns	8
• Changed the Switching Characteristics condition statement From: 50 kbps devices (SN65HVD76, 77, 78) bit time > 20 ns To: 50 Mbps devices (SN65HVD76, 77, 78) bit time > 20 ns	8
• Added Figure 4 to <i>Typical Characteristics</i>	9
• Added Figure 5 to <i>Typical Characteristics</i>	9
• Added Figure 6 to <i>Typical Characteristics</i>	9
• Added Figure 7 to <i>Typical Characteristics</i>	9
• Added Figure 8 to <i>Typical Characteristics</i>	9
• Added Figure 9 to <i>Typical Characteristics</i>	9
• Added <i>Application Information</i> section to data sheet.	17

5 Device Comparison Table

PART NUMBER	SIGNALING RATE	NODES	DUPLEX	ENABLES
SN65HVD72	Up to 250 kbps	213	Half	DE, \overline{RE}
SN65HVD75	Up to 20 Mbps			
SN65HVD78	Up to 50 Mbps	96		

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
A	6	Bus I/O	Driver output or receiver input (complementary to B)
B	7	Bus I/O	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Active-high driver enable
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
\overline{RE}	2	Digital input	Active-low receiver enable
V _{CC}	8	Supply	3-V to 3.6-V supply

7 Specifications

7.1 Absolute Maximum Ratings

over recommended operating range (unless otherwise specified) ⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, V_{CC}	-0.5	5.5	V
Voltage at A or B inputs	-13	16.5	
Input voltage at any logic pin	-0.3	5.7	
Voltage input, transient pulse, A and B, through 100 Ω	-100	100	
Receiver output current	-24	24	mA
Junction temperature, T_J		170	°C
Continuous total power dissipation	See Power Dissipation		
Storage temperature, T_{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±8000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1500
		JEDEC Standard 22, Test Method A115 (Machine Model), all pins	±300
		IEC 61000-4-2 ESD (Air-Gap Discharge), bus pins and GND ⁽³⁾	±12000
		IEC 61000-4-2 ESD (Contact Discharge), bus pins and GND	±12000
		IEC 61000-4-4 EFT (Fast transient or burst) bus pins and GND	±4000
		IEC 60749-26 ESD (Human Body Model), bus pins and GND	±15000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) By inference from contact discharge results, see [Application and Implementation](#).

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_I	Input voltage at any bus terminal (separately or common mode) ⁽¹⁾	-7		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)	2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)	0		0.8	V
V_{ID}	Differential input voltage	-12		12	V
I_O	Output current, driver	-60		60	mA
I_O	Output current, receiver	-8		8	mA
R_L	Differential load resistance	54	60		Ω
C_L	Differential load capacitance		50		pF
$1/t_{UI}$	Signaling rate	SN65HVD72		250	kbps
		SN65HVD75		20	Mbps
		SN65HVD78		50	Mbps
T_A ⁽²⁾	Operating free-air temperature (See Thermal Information)	-40		125	°C
T_J	Junction temperature	-40		150	°C

- (1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shutdown (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN65HVD72, SN65HVD75, SN65HVD78			UNIT
		D (SOIC)	DGK (VSSOP)	DRB (VSON)	
		8 PINS			
R _{θJA}	Junction-to-ambient thermal resistance	110.7	168.7	40	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	54.7	62.2	49.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	—	3.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	51.3	89.5	15.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	9.2	7.4	0.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	50.7	87.9	15.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

over recommended operating range (unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OD}	R _L = 60 Ω, 375 Ω on each output to -7 V to 12 V	See Figure 10	1.5	2	V
	R _L = 54 Ω (RS-485)	See Figure 11	1.5	2	
	R _L = 100 Ω (RS-422), T _J ≥ 0°C V _{CC} ≥ 3.2 V		2	2.5	
Δ V _{OD}	Change in magnitude of driver differential output voltage R _L = 54 Ω, C _L = 50 pF	-50	0	50	mV
V _{OC(SS)}	Steady-state common-mode output voltage Center of two 27-Ω load resistors	1	V _{CC} /2	3	V
ΔV _{OC}	Change in differential driver output common-mode voltage Center of two 27-Ω load resistors	-50	0	50	mV
V _{OC(PP)}	Peak-to-peak driver common-mode output voltage Center of two 27-Ω load resistors		200		mV
C _{OD}	Differential output capacitance		15		pF
V _{IT+}	Positive-going receiver differential input voltage threshold	See ⁽¹⁾	-70	-20	mV
V _{IT-}	Negative-going receiver differential input voltage threshold	-200	-150	See ⁽¹⁾	mV
V _{HYS}	Receiver differential input voltage threshold hysteresis (V _{IT+} - V _{IT-})	50	80		mV
V _{OH}	Receiver high-level output voltage I _{OH} = -8 mA	2.4	V _{CC} - 0.3		V
V _{OL}	Receiver low-level output voltage I _{OL} = 8 mA		0.2	0.4	V
I _I	Driver input, driver enable, and receiver enable input current	-2		2	μA
I _{OZ}	Receiver output high-impedance current V _O = 0 V or V _{CC} , \overline{RE} at V _{CC}	-1		1	μA
I _{OS}	Driver short-circuit output current	-160		160	mA

(1) Under any specific conditions, V_{IT+} is assured to be at least V_{HYS} higher than V_{IT-}.

Electrical Characteristics (continued)

over recommended operating range (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
I_I	Bus input current (disabled driver)	$V_{CC} = 3$ to 3.6 V or $V_{CC} = 0$ V DE at 0 V	SN65HVD72	$V_I = 12$ V		75	150	μ A
			SN65HVD75	$V_I = -7$ V	-100	-40		
			SN65HVD78	$V_I = 12$ V		240	333	
				$V_I = -7$ V	-267	-180		
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC} , $\overline{RE} = GND$ No load			750	950	μ A
			Driver enabled, receiver disabled DE = V_{CC} , $\overline{RE} = V_{CC}$ No load			300	500	
			Driver disabled, receiver enabled DE = GND, $\overline{RE} = GND$ No load			600	800	
			Driver and receiver disabled $\overline{DE} = GND$, D = open $\overline{RE} = V_{CC}$, No load			0.1	2	
	Supply current (dynamic)	See Typical Characteristics						
T_{TSD}	Thermal shutdown junction temperature				170		$^{\circ}$ C	

7.6 Power Dissipation

PARAMETER		TEST CONDITIONS		VALUE	UNIT	
PD	Power Dissipation driver and receiver enabled, $V_{CC} = 3.6$ V, $T_J = 150^{\circ}$ C 50% duty cycle square-wave signal at signaling rate: <ul style="list-style-type: none"> • SN65HVD72 at 250 kbps • SN65HVD75 at 20 Mbps • SN65HVD78 at 50 Mbps 	Unterminated	$R_L = 300 \Omega$ $C_L = 50$ pF (driver)	SN65HVD72	120	mW
				SN65HVD75	160	
				SN65HVD78	200	
		RS-422 load	$R_L = 100 \Omega$ $C_L = 50$ pF (driver)	SN65HVD72	155	mW
				SN65HVD75	195	
				SN65HVD78	230	
		RS-485 load	$R_L = 54 \Omega$ $C_L = 50$ pF (driver)	SN65HVD72	190	mW
				SN65HVD75	230	
				SN65HVD78	260	

7.7 Switching Characteristics: 250 kbps Device (SN65HVD72) Bit Time $\geq 4 \mu$ s

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise or fall time	$R_L = 54 \Omega$ $C_L = 50$ pF	See Figure 12	0.3	0.7	1.2	μ s
t_{PHL}, t_{PLH}	Driver propagation delay				0.7	1	μ s
$t_{SK(P)}$	Driver pulse skew, $ t_{PHL} - t_{PLH} $					0.2	μ s
t_{PHZ}, t_{PLZ}	Driver disable time				0.1	0.4	μ s
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See Figure 13 and Figure 14		0.5	1	μ s
		Receiver disabled			3	9	
RECEIVER							
t_r, t_f	Receiver output rise or fall time	$C_L = 15$ pF	See Figure 15		12	30	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				75	100	ns
$t_{SK(P)}$	Receiver pulse skew, $ t_{PHL} - t_{PLH} $				3	15	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				40	100	ns
$t_{PZL(1)}, t_{PZH(1)}, t_{PZL(2)}, t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 16		20	50	ns
		Driver disabled	See Figure 17		3	8	μ s

7.8 Switching Characteristics: 20 Mbps Device (SN65HVD75) Bit Time ≥ 50 ns

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise or fall time	$R_L = 54 \Omega$ $C_L = 50 \text{ pF}$	See Figure 12	2	7	14	ns
t_{PHL}, t_{PLH}	Driver propagation delay			7	11	17	ns
$t_{SK(P)}$	Driver pulse skew, $ t_{PHL} - t_{PLH} $				0	2	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 13 and Figure 14		12	50	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			10	20	ns
		Receiver disabled		3	7	μs	
RECEIVER							
t_r, t_f	Receiver output rise or fall time	$C_L = 15 \text{ pF}$	See Figure 15		5	10	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				60	70	ns
$t_{SK(P)}$	Receiver pulse skew, $ t_{PHL} - t_{PLH} $				0	6	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				15	30	ns
$t_{pZL(1)}, t_{pZH(1)},$ $t_{pZL(2)}, t_{pZH(2)}$	Receiver enable time	Driver enabled	See Figure 16		10	50	ns
		Driver disabled	See Figure 17		3	8	μs

7.9 Switching Characteristics: 50 Mbps Device (SN65HVD78) Bit Time ≥ 20 ns

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise or fall time	$R_L = 54 \Omega$ $C_L = 50 \text{ pF}$	See Figure 12	1	3	6	ns
t_{PHL}, t_{PLH}	Driver propagation delay				9	15	ns
$t_{SK(P)}$	Driver pulse skew, $ t_{PHL} - t_{PLH} $				0	1	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 13 and Figure 14		10	30	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			10	30	ns
		Receiver disabled				8	μs
RECEIVER							
t_r, t_f	Receiver output rise or fall time	$C_L = 15 \text{ pF}$	See Figure 15	1	3	6	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time					35	ns
$t_{SK(P)}$	Receiver pulse skew, $ t_{PHL} - t_{PLH} $					2.5	ns
t_{PLZ}, t_{PHZ}	Receiver disable time					8	30
$t_{pZL(1)}, t_{pZH(1)},$ $t_{pZL(2)}, t_{pZH(2)}$	Receiver enable time	Driver enabled	See Figure 16		10	30	ns
		Driver disabled	See Figure 17		3	8	μs

7.10 Typical Characteristics

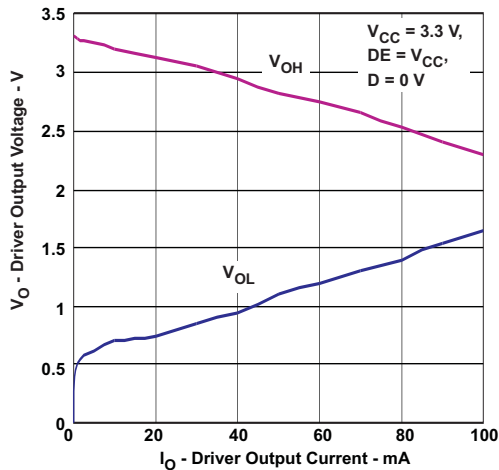


Figure 1. Driver Output Voltage vs Driver Output Current

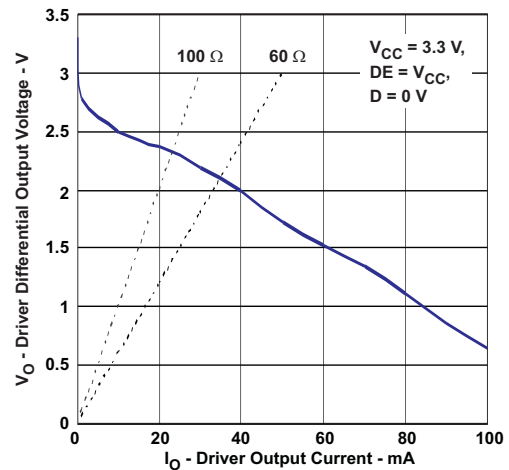


Figure 2. Driver Differential Output Voltage vs Driver Output Current

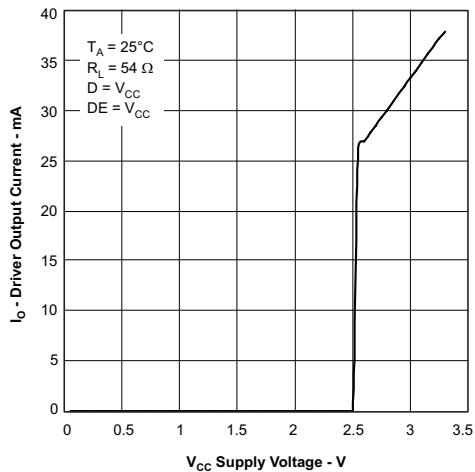


Figure 3. Driver Output Current vs Supply Voltage

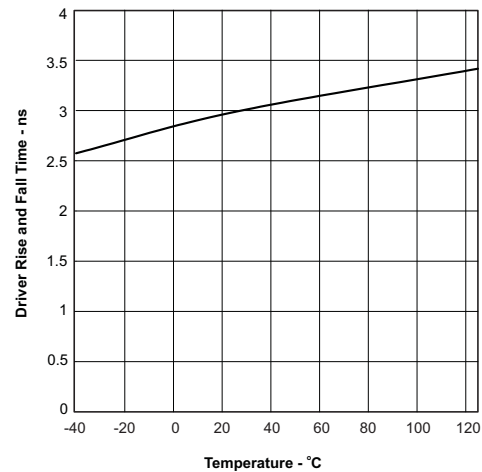


Figure 4. SN65HVD78 Driver Rise or Fall Time vs Temperature

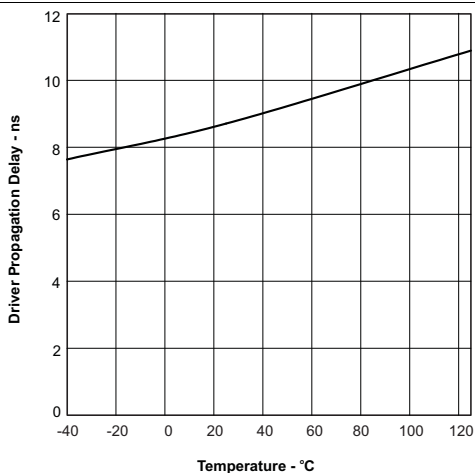


Figure 5. SN65HVD78 Driver Propagation Delay vs Temperature

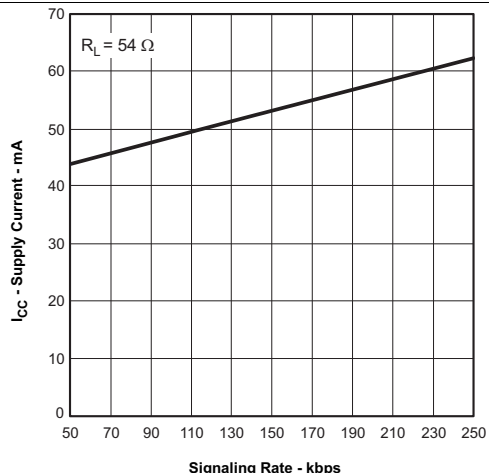


Figure 6. SN65HVD72 Supply Current vs Signal Rate

Typical Characteristics (continued)

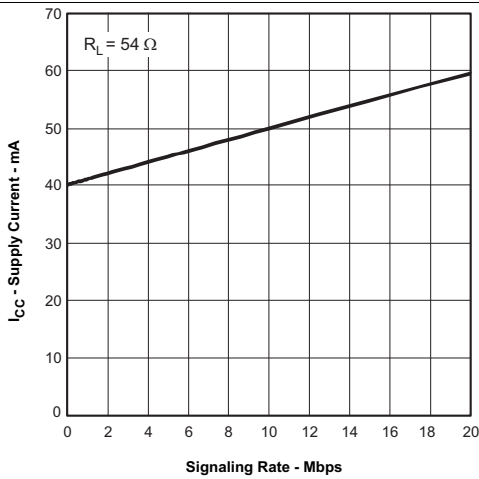


Figure 7. SN65HVD75 Supply Current vs Signal Rate

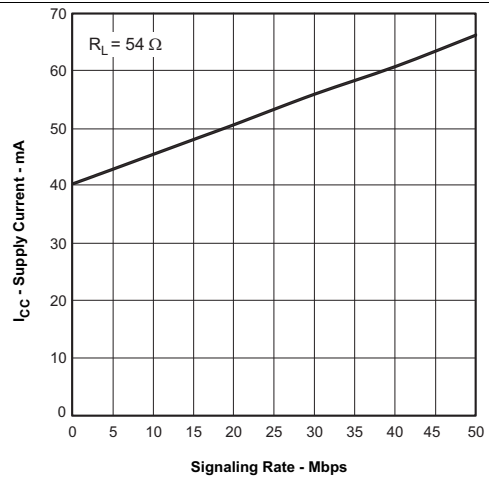


Figure 8. SN65HVD78 Supply Current vs Signal Rate

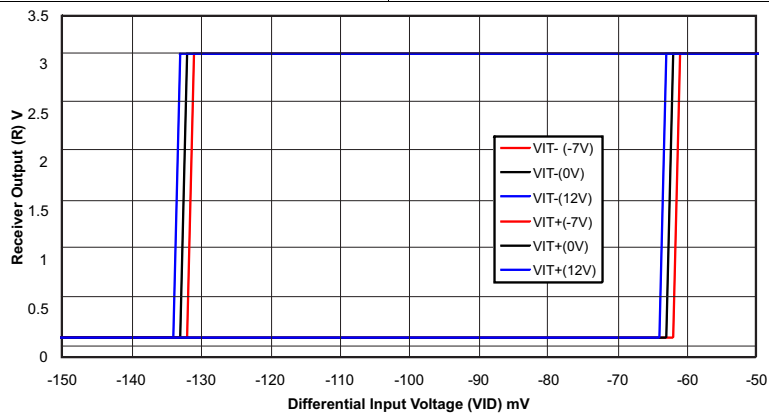


Figure 9. Receiver Output vs Input

8 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise or fall time is less than 6 ns, output impedance is 50 Ω .

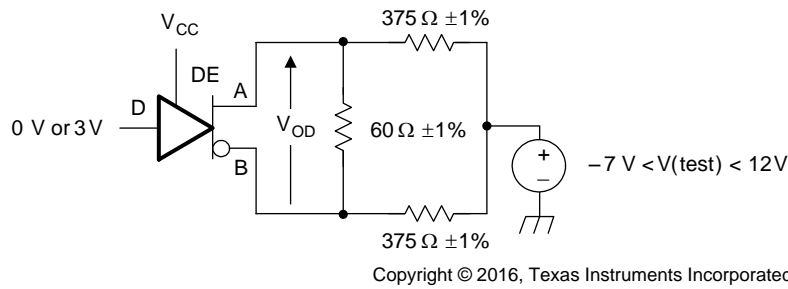


Figure 10. Measurement of Driver Differential Output Voltage With Common-Mode Load

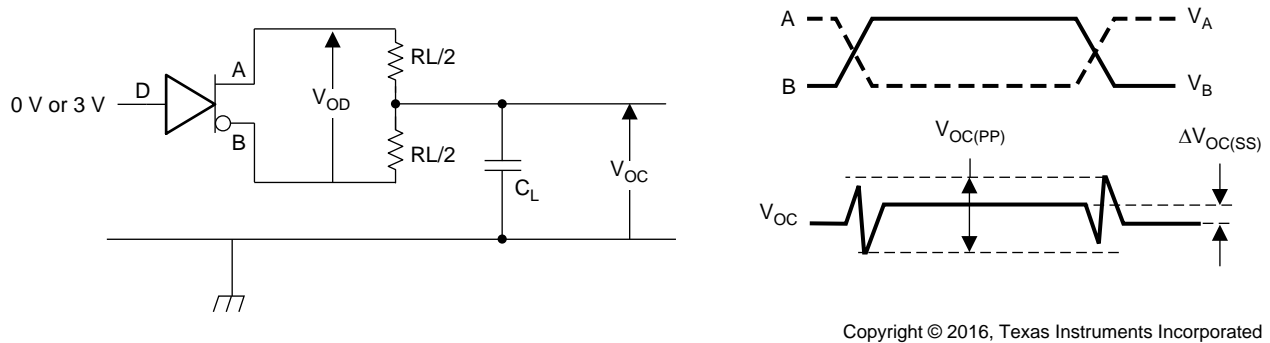


Figure 11. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

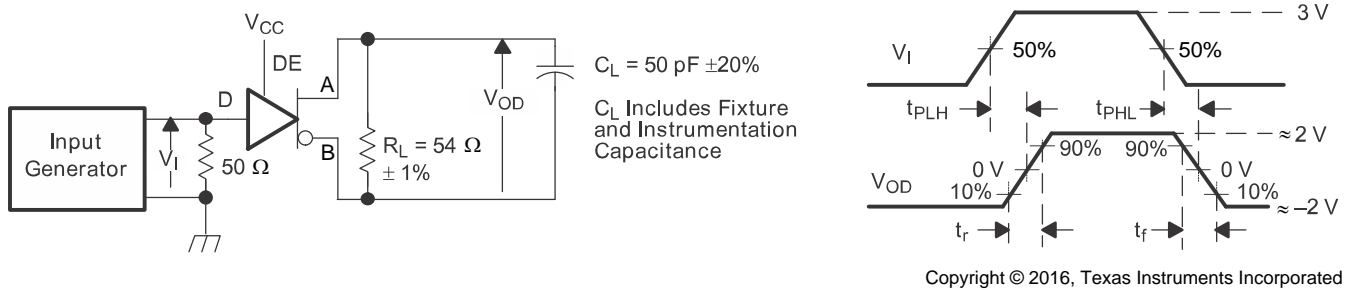
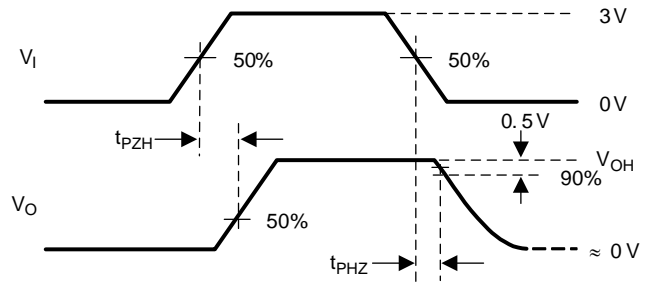
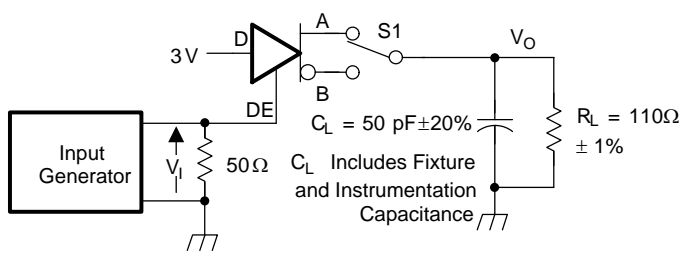


Figure 12. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

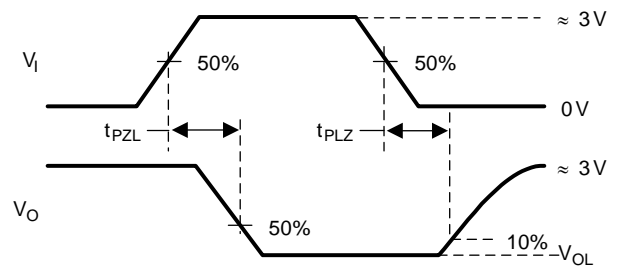
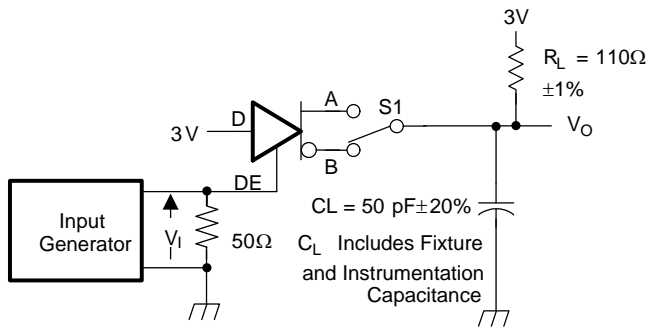
Parameter Measurement Information (continued)



Copyright © 2016, Texas Instruments Incorporated

D at 3 V to test non-inverting output, D at 0 V to test inverting output.

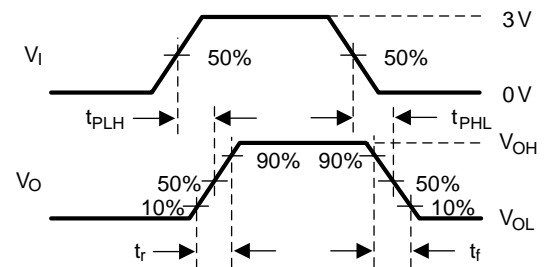
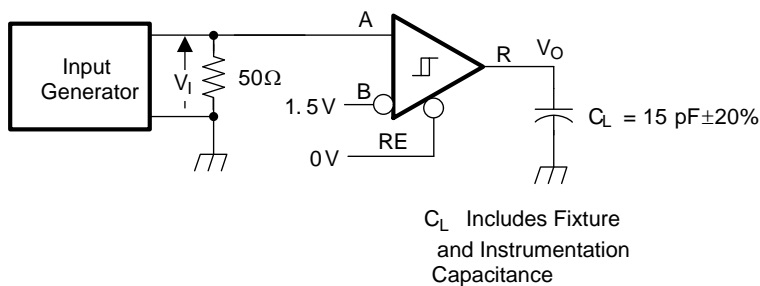
Figure 13. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load



Copyright © 2016, Texas Instruments Incorporated

D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 14. Measurement of Driver Enable and Disable Times With Active Low Output and Pullup Load



Copyright © 2016, Texas Instruments Incorporated

Figure 15. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

Parameter Measurement Information (continued)

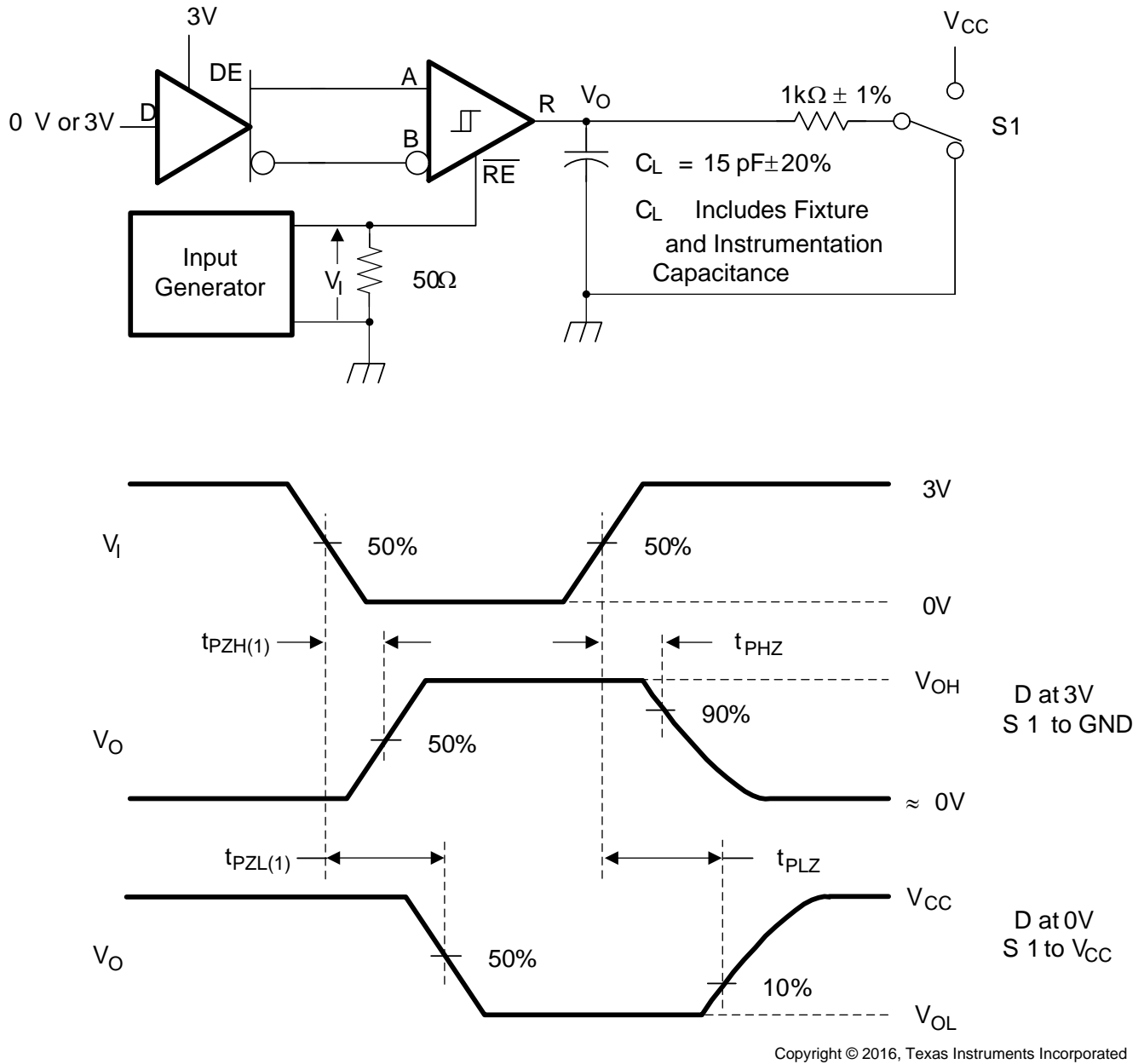


Figure 16. Measurement of Receiver Enable and Disable Times With Driver Enabled

Parameter Measurement Information (continued)

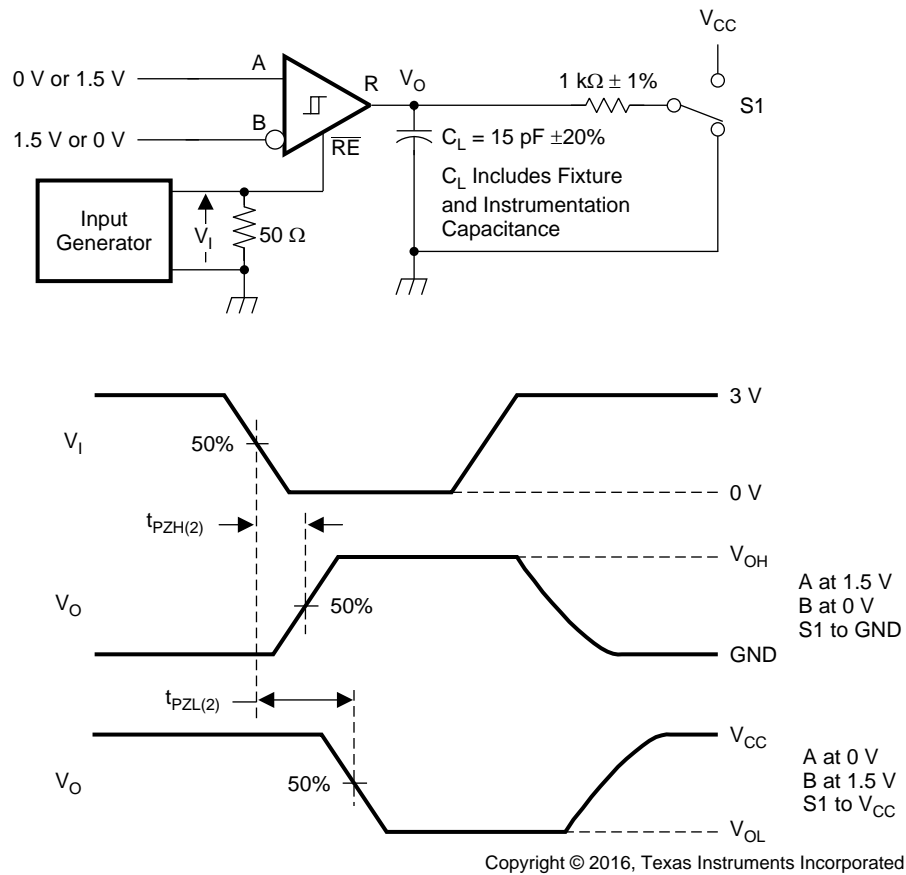


Figure 17. Measurement of Receiver Enable Times With Driver Disabled

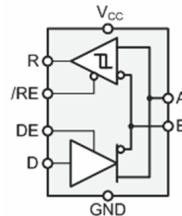
9 Detailed Description

9.1 Overview

The SN65HVD72, SN65HVD75, and SN65HVD78 are low-power, half-duplex RS-485 transceivers available in 3 speed grades suitable for data transmission up to 250 kbps, 20 Mbps, and 50 Mbps.

These devices have active-high driver enables and active-low receiver enables. A standby current of less than 2 μ A can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

9.3 Feature Description

Internal ESD protection circuits protect the transceiver against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ± 12 kV, and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ± 4 kV.

The SN65HVD7x half-duplex family provides internal biasing of the receiver input thresholds in combination with large input threshold hysteresis. At a positive input threshold of $V_{IT+} = -20$ mV and an input hysteresis of $V_{HYS} = 50$ mV, the receiver output remains logic high under a bus-idle or bus-short condition even in the presence of 140-mV_{PP} differential noise without the need for external failsafe biasing resistors.

Device operation is specified over a wide ambient temperature range from -40°C to 125°C .

9.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground; thus, when left open, the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC} ; thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 1. Driver Function Table

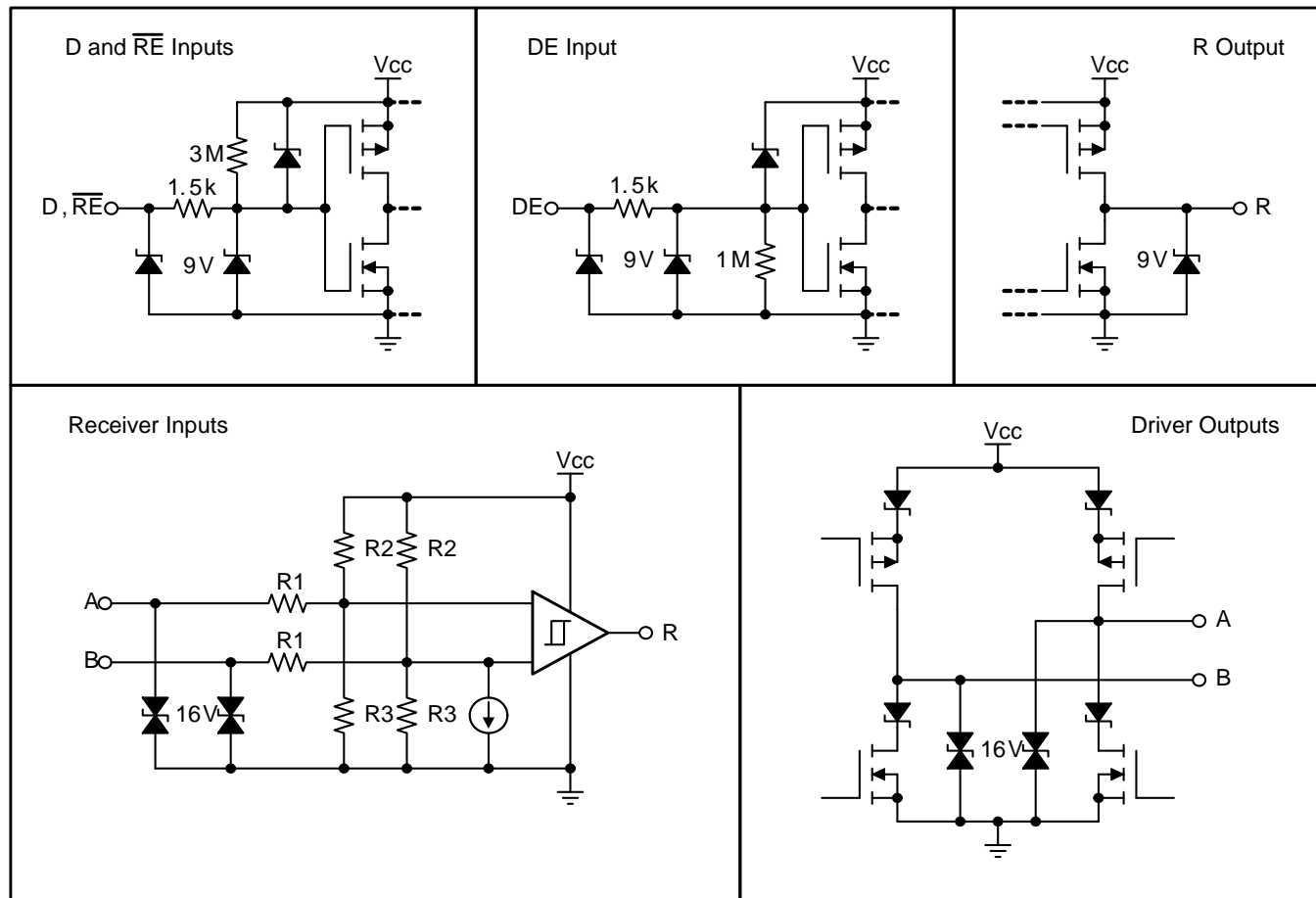
INPUT	ENABLE	OUTPUTS		DESCRIPTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, \overline{RE} , is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+} , the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-} , the receiver output turns low. If V_{ID} is between V_{IT+} and V_{IT-} , the output is indeterminate.

When \overline{RE} is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	DESCRIPTION
$V_{ID} = V_A - V_B$	\overline{RE}	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Failsafe high output
Short-circuit bus	L	H	Failsafe high output
Idle (terminated) bus	L	H	Failsafe high output



Copyright © 2016, Texas Instruments Incorporated

Figure 18. Equivalent Input and Output Circuit Diagrams

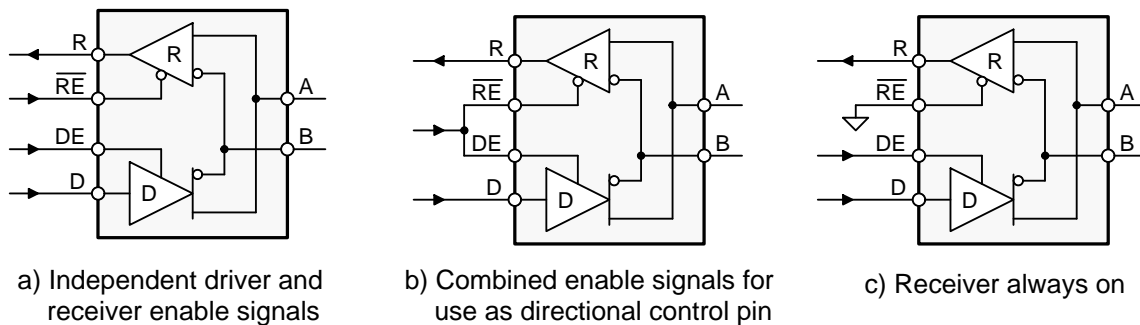
10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN65HVD72, SN65HVD75, and SN65HVD78 are half-duplex RS-485 transceivers commonly used for asynchronous data transmission. The driver and receiver enable pins allow for the configuration of different operating modes.



Copyright © 2016, Texas Instruments Incorporated

Figure 19. Transceiver Configurations

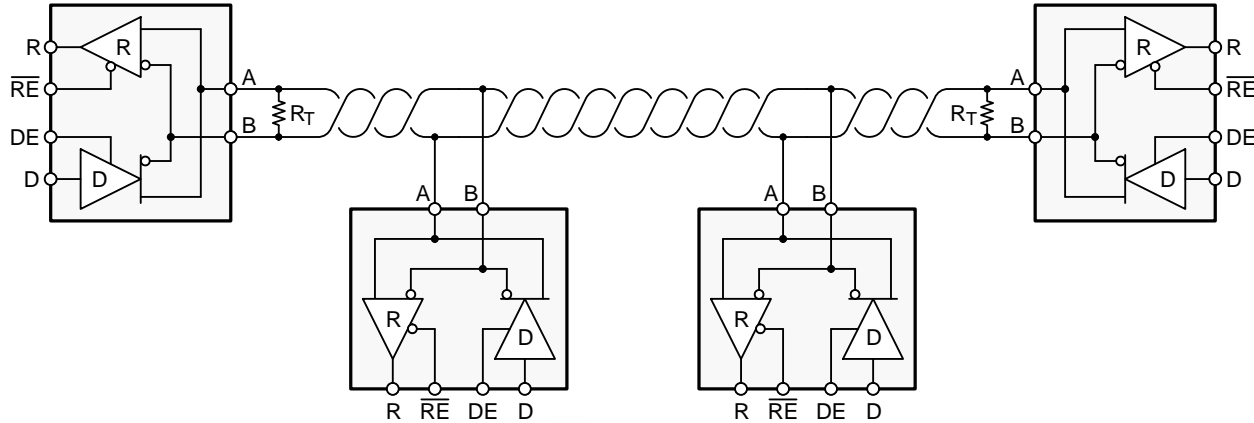
Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high, and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

10.2 Typical Application

An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T , whose value matches the characteristic impedance, Z_0 , of the cable. This method, known as parallel termination, allows for relatively high data rates over long cable lengths.



Copyright © 2016, Texas Instruments Incorporated

Figure 20. Typical RS-485 Network With SN65HVD7x Transceivers

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with $Z_0 = 100 \Omega$, and RS-485 cable with $Z_0 = 120 \Omega$. Typical cable sizes are AWG 22 and AWG 24.

The maximum bus length is typically given as 4000 ft or 1200 m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6 dB. Actual maximum usable cable length depends on the signaling rate, cable characteristics, and environmental conditions.

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

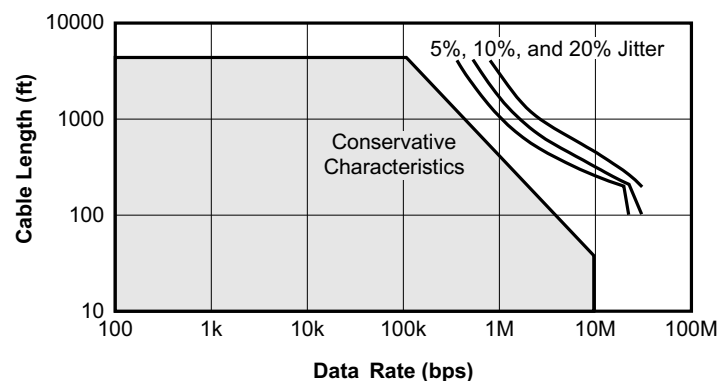


Figure 21. Cable Length vs Data Rate Characteristic

Typical Application (continued)

10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in [Equation 1](#).

$$L_{\text{stub}} \leq 0.1 \times t_r \times v \times c$$

where:

- t_r is the 10/90 rise time of the driver
 - c is the speed of light (3×10^8 m/s)
 - v is the signal velocity of the cable or trace as a factor of c
- (1)

Per [Equation 1](#), [Table 3](#) shows the maximum cable-stub lengths for the minimum driver output rise times of the SN65HVD7x half-duplex family of transceivers for a signal velocity of 78%.

Table 3. Maximum Stub Length

DEVICE	MINIMUM DRIVER OUTPUT RISE TIME (ns)	MAXIMUM STUB LENGTH	
		(m)	(ft)
SN65HVD72	300	7	23
SN65HVD75	2	0.05	0.16
SN65HVD78	1	0.025	0.08

10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a receiver input current of 1 mA at 12 V, or a load impedance of approximately 12 k Ω . Because the SN65HVD72 and SN65HVD75 have a receiver input current of 150 μ A at 12 V, they are 3/20 UL transceivers, and no more than 213 transceivers should be connected to the bus. Similarly, the SN65HVD78 has a receiver input current of 333 μ A at 12 V and is a 1/3 UL transceiver, meaning no more than 96 transceivers should be connected to the bus.

10.2.1.4 Receiver Failsafe

The differential receiver is failsafe to invalid bus states caused by:

- Open bus conditions such as a disconnected connector
- Shorted bus conditions such as cable damage shorting the twisted-pair together, or
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the input-indeterminate range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than -200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} , V_{IT-} , and V_{HYS} (the separation between V_{IT+} and V_{IT-}). As shown in [Electrical Characteristics](#), differential signals more negative than -200 mV will always cause a low receiver output, and differential signals more positive than 200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the maximum V_{IT+} threshold of -20 mV, and the receiver output will be high. Only when the differential input is more than V_{HYS} below V_{IT+} will the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value, V_{HYS} , as well as the value of V_{IT+} .

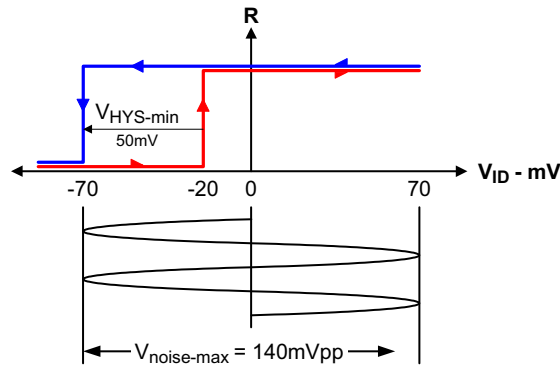
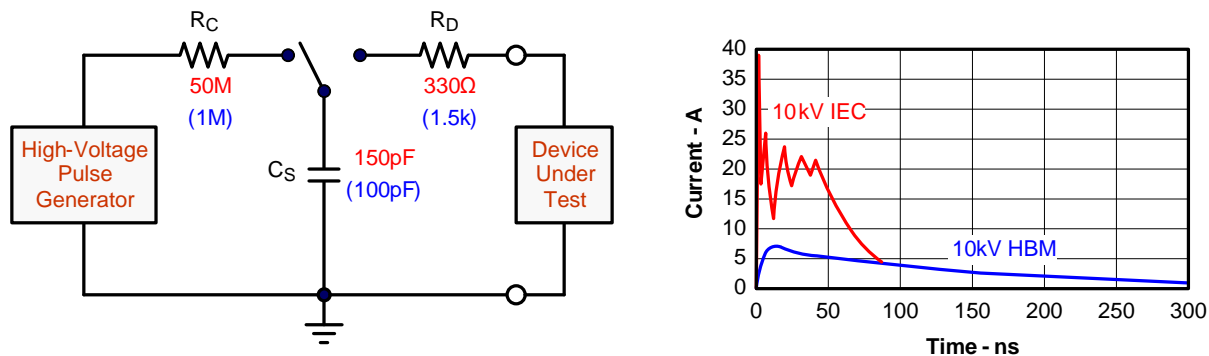


Figure 22. SN65HVD7x Noise Immunity

10.2.1.5 Transient Protection

The bus pins of the SN65HVD7x transceiver family possess on-chip ESD protection against ± 15 -kV human body model (HBM) and ± 12 -kV IEC 61000-4-2 contact discharge. The IEC-ESD test is far more severe than the HBM-ESD test. The 50% higher charge capacitance, C_S , and 78% lower discharge resistance, R_D , of the IEC-model produce significantly higher discharge currents than the HBM-model.

As stated in the IEC 61000-4-2 standard, contact discharge is the preferred test method; although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results.



Copyright © 2016, Texas Instruments Incorporated

Figure 23. HBM and IEC-ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur due to human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 24 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left-hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right-hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

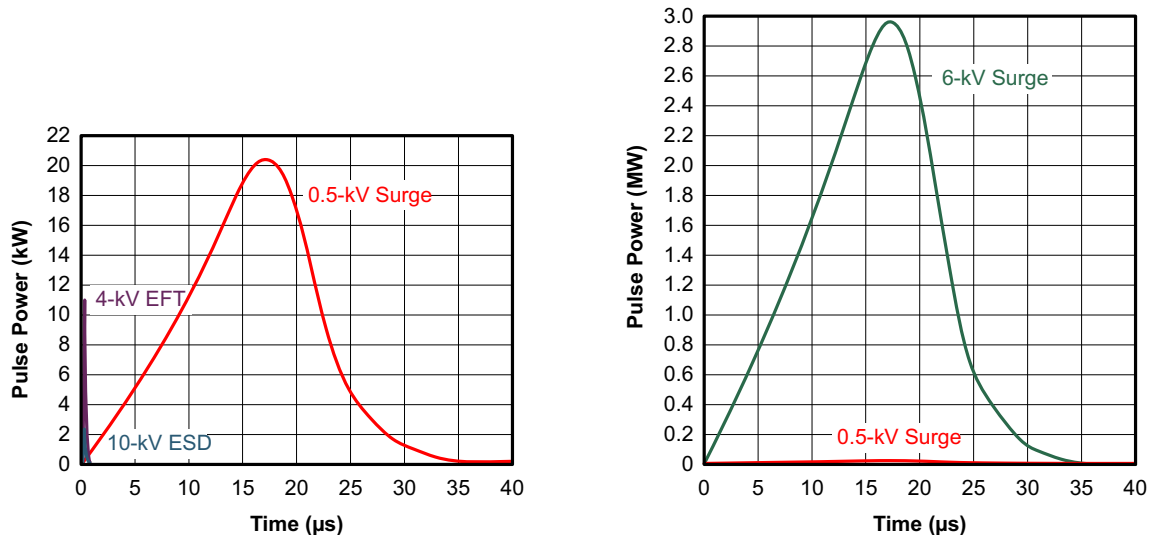


Figure 24. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy which heats and destroys the protection cells, thus destroying the transceiver. Figure 25 shows the large differences in transient energies for single ESD, EFT, and surge transients, as well as for an EFT pulse train, commonly applied during compliance testing.

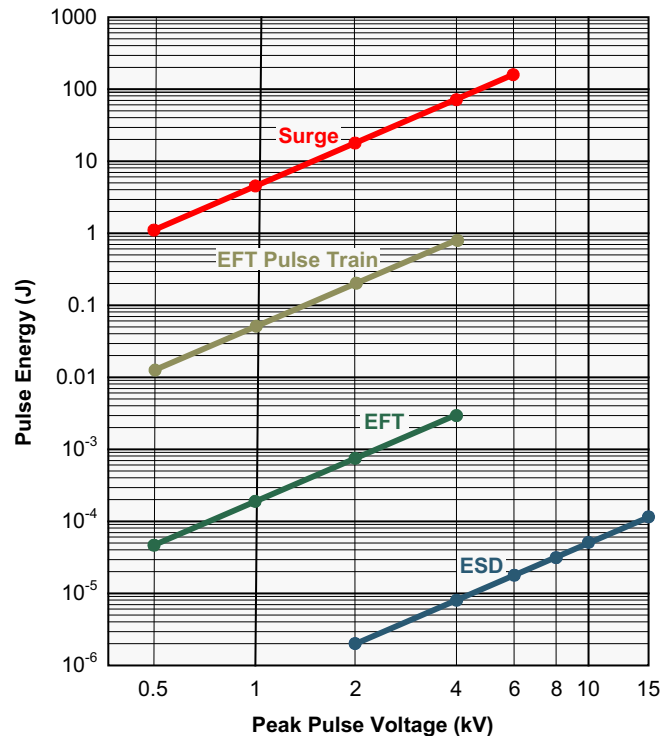


Figure 25. Comparison of Transient Energies

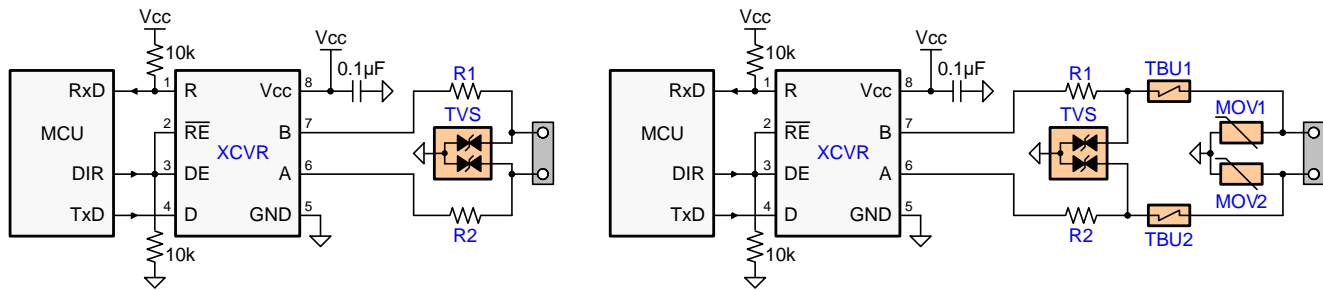
10.2.2 Detailed Design Procedure

10.2.2.1 External Transient Protection

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary. [Figure 26](#) suggests two circuits that provide protection against light and heavy surge transients, in addition to ESD and EFT transients. [Table 4](#) presents the associated bill of materials.

Table 4. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	3.3-V, 250-kbps RS-485 Transceiver	SN65HVD72D	TI
R1, R2	10-Ω, Pulse-Proof Thick-Film Resistor	CRCW060310RJNEAHP	Vishay
TVS	Bidirectional 400-W Transient Suppressor	CDSOT23-SM712	Bourns
TBU1, TBU2	Bidirectional Surge Suppressor	TBU-CA-065-200-WH	Bourns
MOV1, MOV2	200-mA Transient Blocking Unit, 200-V, Metal-Oxide Varistor	MOV-10D201K	Bourns



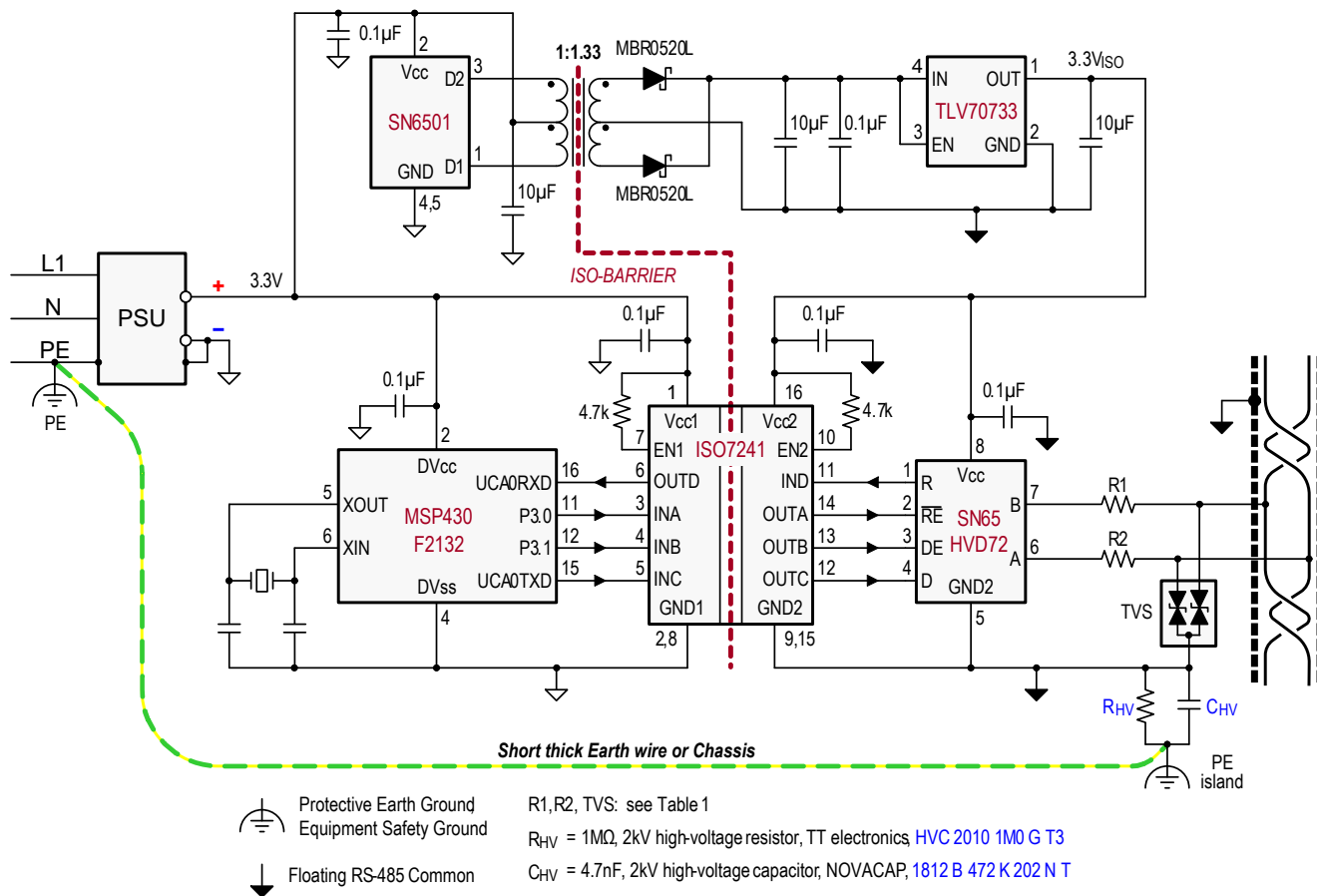
Copyright © 2016, Texas Instruments Incorporated

Figure 26. Transient Protections Against ESD, EFT, and Surge Transients

The left-hand circuit provides surge protection of ≥ 500 -V surge transients, while the right-hand circuit can withstand surge transients of up to 5 kV.

10.2.2.2 Isolated Bus Node Design

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a microcontroller that connects to the bus transceiver via a multi-channel, digital isolator (Figure 27).



Copyright © 2016, Texas Instruments Incorporated

Figure 27. Isolated Bus Node with Transient Protection

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TLV70733.

Signal isolation uses the quadruple digital isolator ISO7241. Notice that both enable inputs, EN₁ and EN₂, are pulled up via 4.7 kΩ resistors to limit their input currents during transient events.

While the transient protection is similar to the one in Figure 26 (left circuit), an additional high-voltage capacitor is used to divert transient energy from the floating RS-485 common further towards Protective Earth (PE) ground. This is necessary as noise transients on the bus are usually referred to Earth potential.

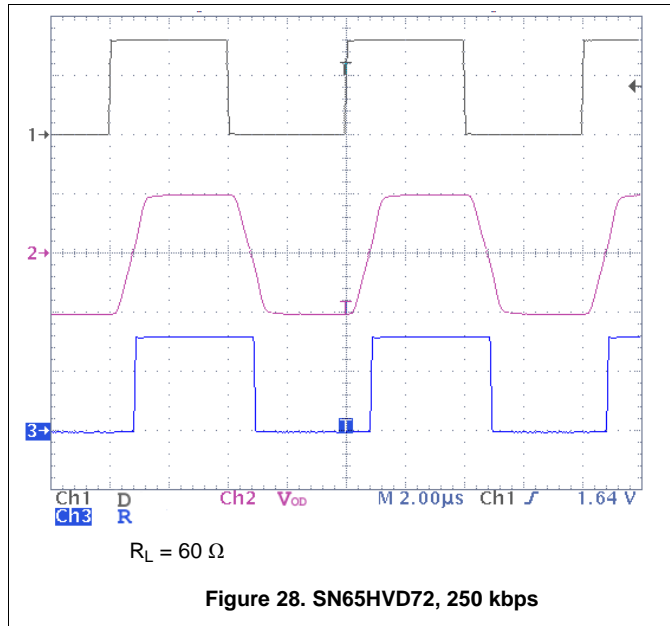
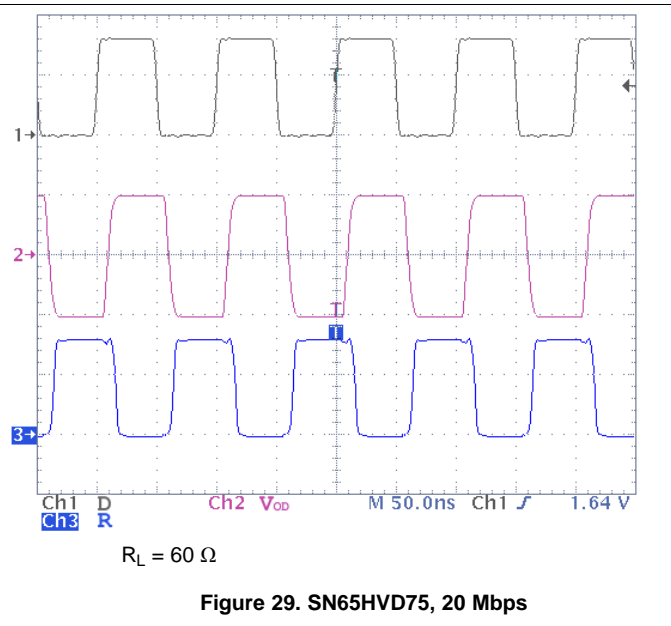
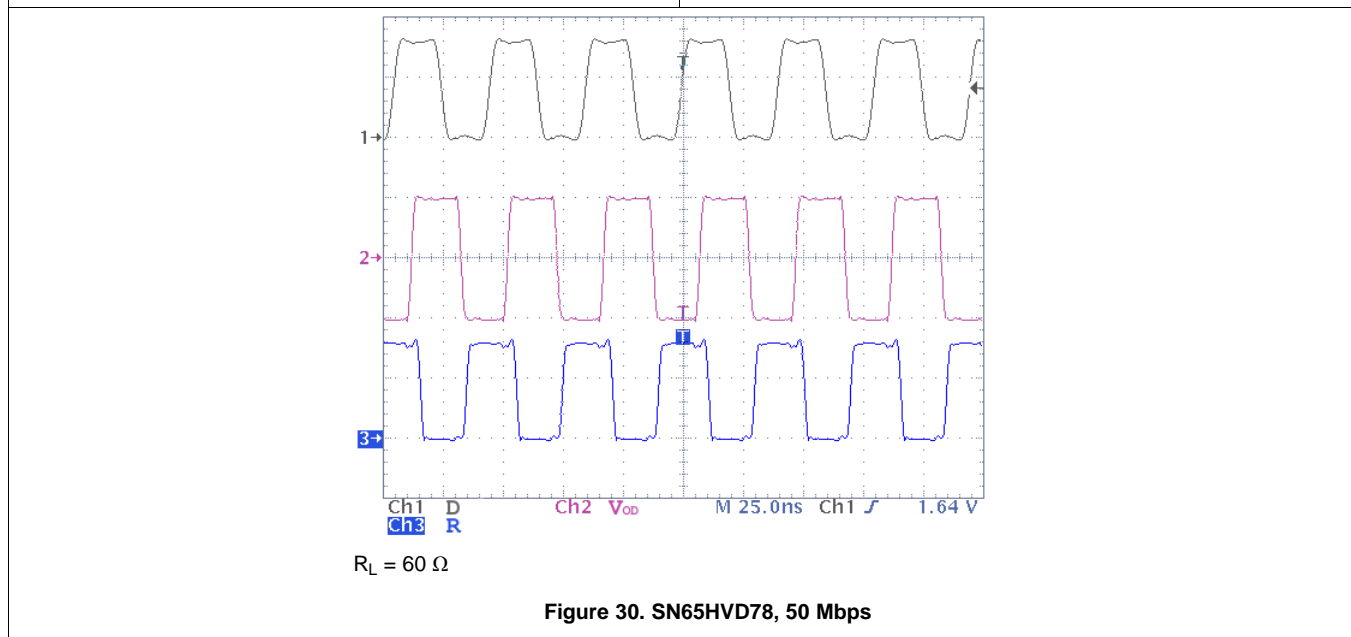
R_{HV} refers to a high voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Occasionally varistors are used instead of resistors to rapidly discharge C_{HV}, if it is expected that fast transients might charge C_{HV} to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components, C_{HV} and R_{HV}, are connecting to the chassis at the other end.

10.2.3 Application Curves


Figure 28. SN65HVD72, 250 kbps

Figure 29. SN65HVD75, 20 Mbps

Figure 30. SN65HVD78, 50 Mbps

11 Power Supply Recommendations

To assure reliable operation at all data rates and supply voltages, each supply should be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS76333 is a linear voltage regulator suitable for the 3.3 V supply.

See the [SN6501](#) data sheet for isolated power supply designs.

12 Layout

12.1 Layout Guidelines

On-chip IEC ESD protection is sufficient for laboratory and portable equipment but often insufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

For a successful PCB design, start with the design of the protection circuit in mind.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use V_{CC} and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC} pins of transceiver, UART, and controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1-k Ω to 10-k Ω pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof series resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to 200 mA.

12.2 Layout Example

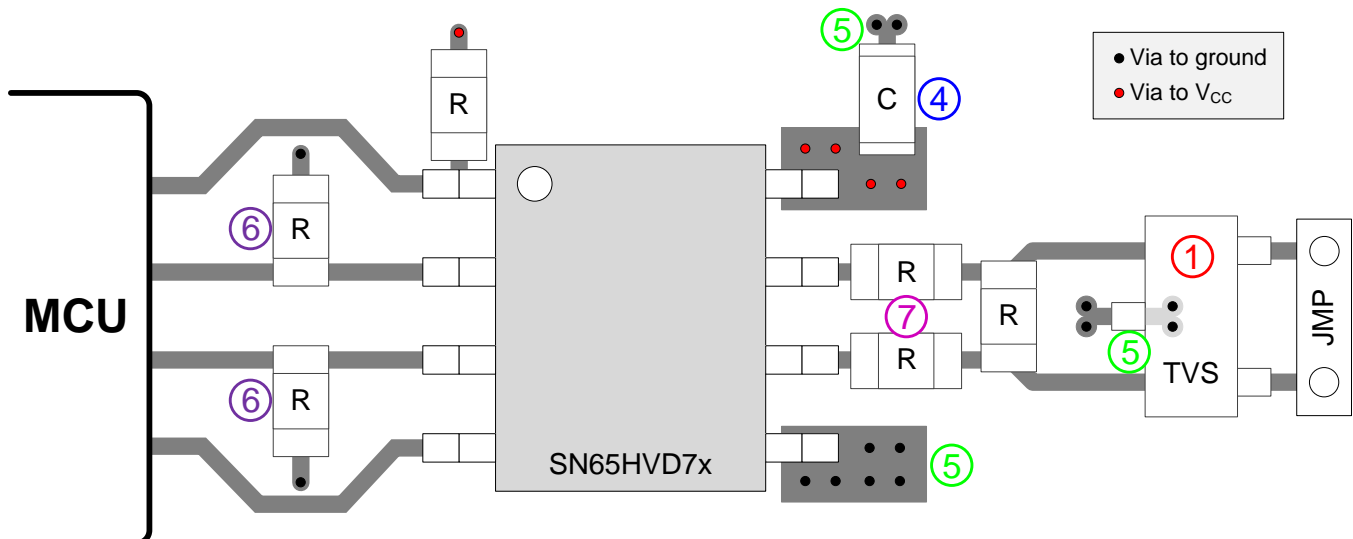


Figure 31. SN65HVD7x Half-Duplex Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

SN6501 Transformer Driver for Isolated Power Supplies, [SLLSEA0](#)

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65HVD72	Click here	Click here	Click here	Click here	Click here
SN65HVD75	Click here	Click here	Click here	Click here	Click here
SN65HVD78	Click here	Click here	Click here	Click here	Click here

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD72D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD72	Samples
SN65HVD72DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HVD72	Samples
SN65HVD72DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HVD72	Samples
SN65HVD72DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD72	Samples
SN65HVD72DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD72	Samples
SN65HVD72DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD72	Samples
SN65HVD75D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD75	Samples
SN65HVD75DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HVD75	Samples
SN65HVD75DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HVD75	Samples
SN65HVD75DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD75	Samples
SN65HVD75DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD75	Samples
SN65HVD75DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD75	Samples
SN65HVD78D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD78	Samples
SN65HVD78DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HVD78	Samples
SN65HVD78DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HVD78	Samples
SN65HVD78DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD78	Samples
SN65HVD78DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD78	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD78DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD78	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD72DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD72DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD72DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65HVD72DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65HVD75DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD75DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD75DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65HVD75DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65HVD78DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD78DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD78DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65HVD78DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD72DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
SN65HVD72DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD72DRBR	SON	DRB	8	3000	367.0	367.0	35.0
SN65HVD72DRBT	SON	DRB	8	250	210.0	185.0	35.0
SN65HVD75DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
SN65HVD75DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD75DRBR	SON	DRB	8	3000	367.0	367.0	35.0
SN65HVD75DRBT	SON	DRB	8	250	210.0	185.0	35.0
SN65HVD78DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
SN65HVD78DR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD78DRBR	SON	DRB	8	3000	367.0	367.0	35.0
SN65HVD78DRBT	SON	DRB	8	250	210.0	185.0	35.0

DRB 8

GENERIC PACKAGE VIEW

VSON - 1 mm max height

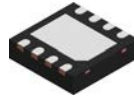
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

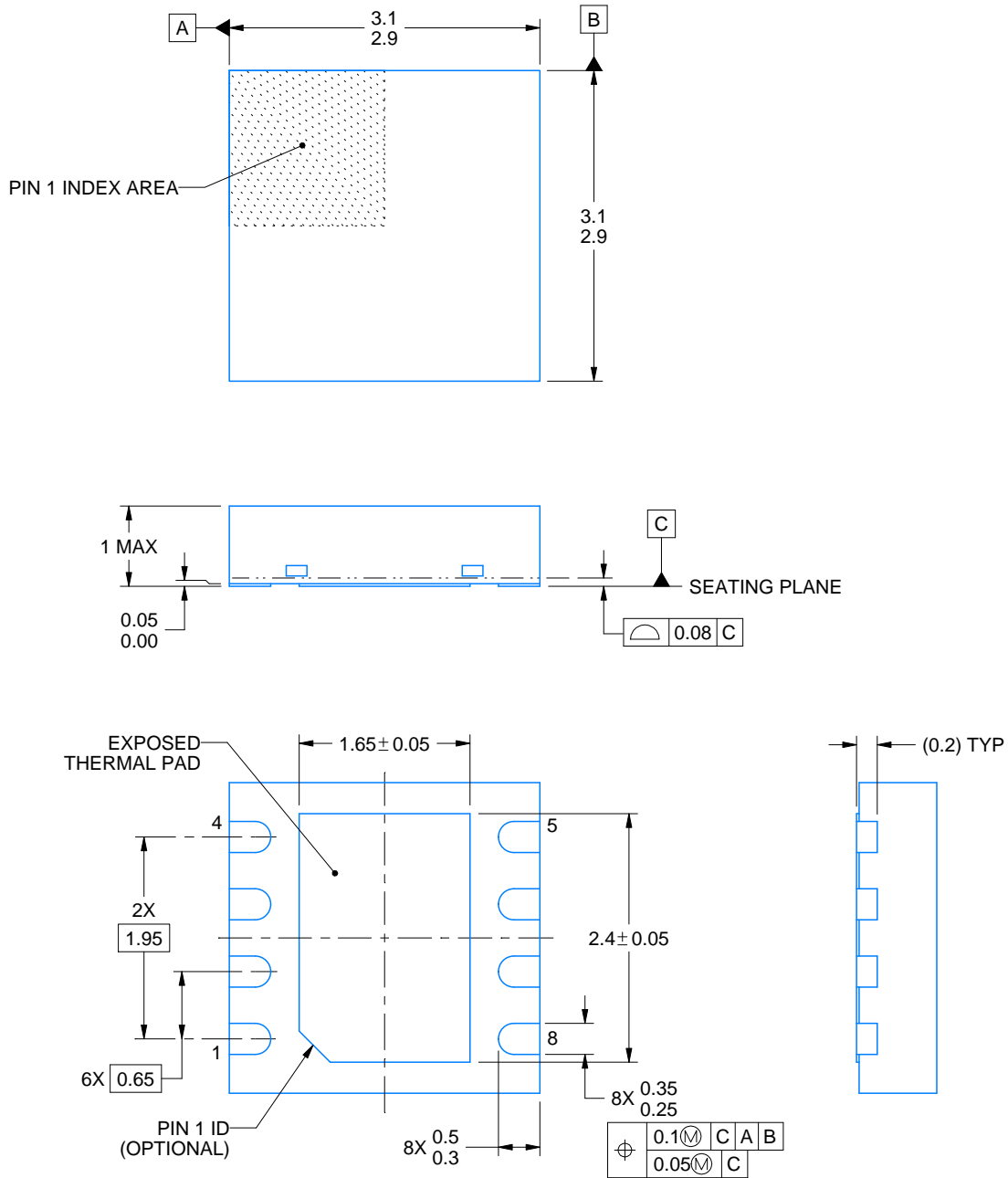
DRB0008B



PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218876/A 12/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

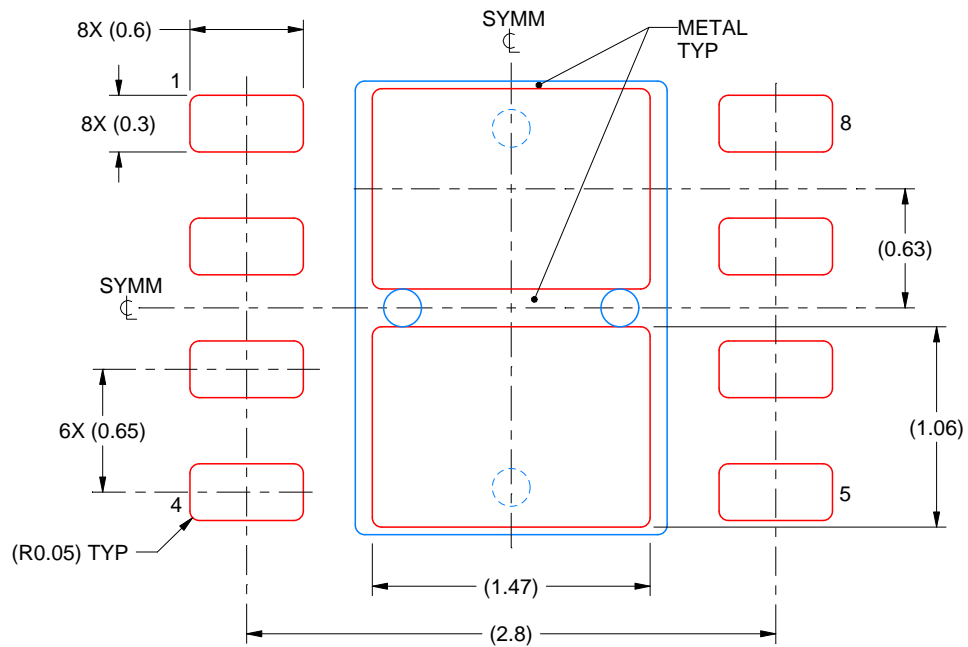
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040047-3/M 06/11

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

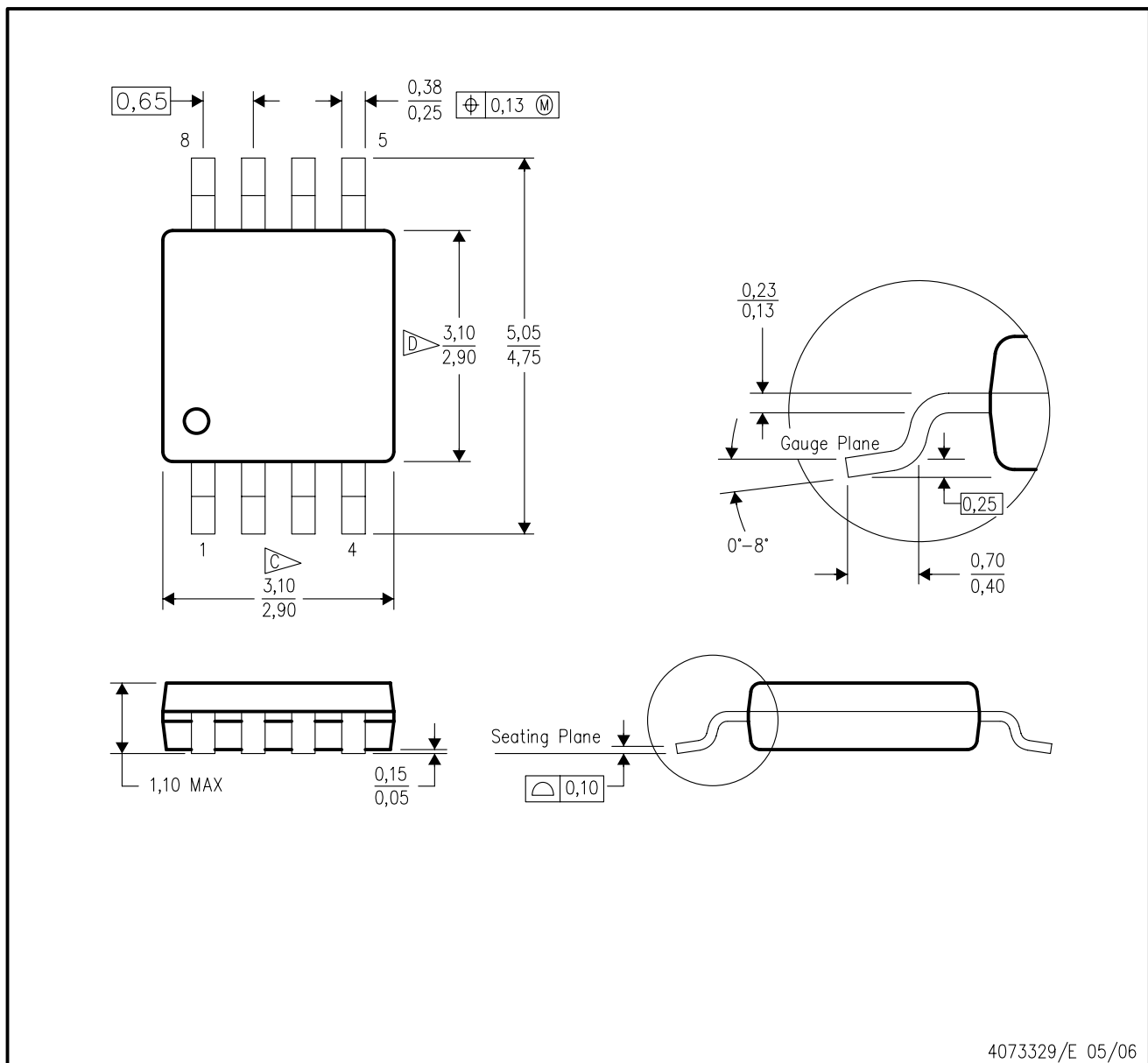


4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.