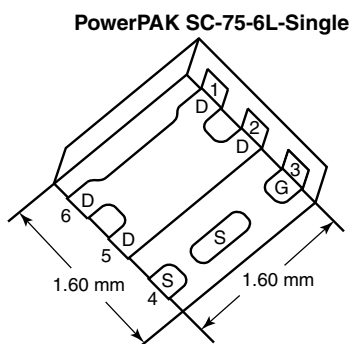




N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A) ^a	Q _g (Typ.)
100	0.185 at V _{GS} = 10 V	6.3	1.8 nC
	0.310 at V _{GS} = 4.5 V	4.9	



Ordering Information:
SiB456DK-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATRUES

- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-75 Package
 - Small Footprint Area
 - Low On-Resistance
- 100 % R_g and UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

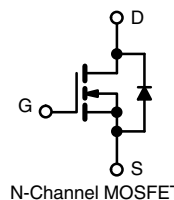
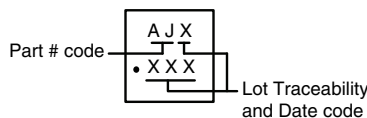


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- DC/DC Converters
- Full-Bridge Converters
- For Power Bricks and POL Power

Marking Code



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	6.3
		T _C = 70 °C	5
		T _A = 25 °C	2.7 ^{b, c}
		T _A = 70 °C	2.2 ^{b, c}
Pulsed Drain Current (t = 300 μs)	I _{DM}	7	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	6.3
		T _A = 25 °C	2 ^{b, c}
Single Pulse Avalanche Current	I _{AS}	2.4	
Single Pulse Avalanche Energy	E _{AS}	0.29	mJ
Maximum Power Dissipation	P _D	T _C = 25 °C	13
		T _C = 70 °C	8.4
		T _A = 25 °C	2.4 ^{b, c}
		T _A = 70 °C	1.6 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	41	51	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	7.5	9.5	

Notes

- T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 105 °C/W.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		54		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 4.1		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.6		3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	6			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 1.9 A		0.153	0.185	Ω
		V _{GS} = 4.5 V, I _D = 1.5 A		0.220	0.310	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 1.9 A		3.7		S
Dynamic^b						
Input Capacitance	C _{iSS}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		130		pF
Output Capacitance	C _{oss}			54		
Reverse Transfer Capacitance	C _{rss}			10		
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 2.7 A		3.3	5	nC
		V _{DS} = 50 V, V _{GS} = 4.5 V, I _D = 2.7 A		1.8	2.7	
Gate-Source Charge	Q _{gs}			0.7		
Gate-Drain Charge	Q _{gd}			1		
Gate Resistance	R _g	f = 1 MHz	1.3	6.5	13	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 23 Ω I _D ≅ 2.2 A, V _{GEN} = 4.5 V, R _g = 1 Ω		15	30	ns
Rise Time	t _r			45	90	
Turn-Off Delay Time	t _{d(off)}			11	20	
Fall Time	t _f			13	25	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 23 Ω I _D ≅ 2.2 A, V _{GEN} = 10 V, R _g = 1 Ω		5	10	
Rise Time	t _r			11	20	
Turn-Off Delay Time	t _{d(off)}			10	20	
Fall Time	t _f			10	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			6.3	A
Pulse Diode Forward Current	I _{SM}				7	
Body Diode Voltage	V _{SD}	I _S = 2.2 A, V _{GS} = 0 V		0.9	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 2.2 A, di/dt = 100 A/μs, T _J = 25 °C		25	50	ns
Body Diode Reverse Recovery Charge	Q _{rr}			20	40	nC
Reverse Recovery Fall Time	t _a			18		ns
Reverse Recovery Rise Time	t _b			7		

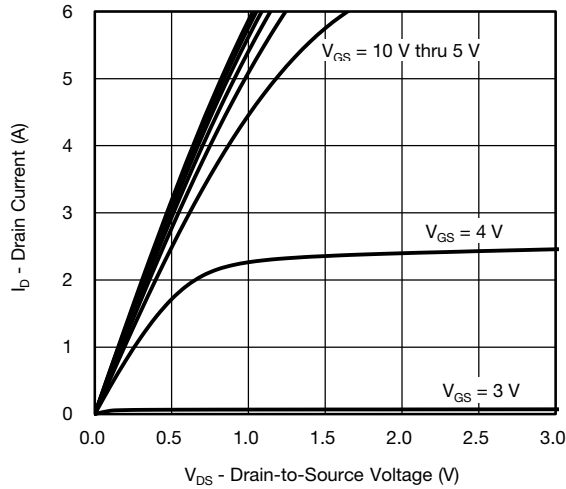
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

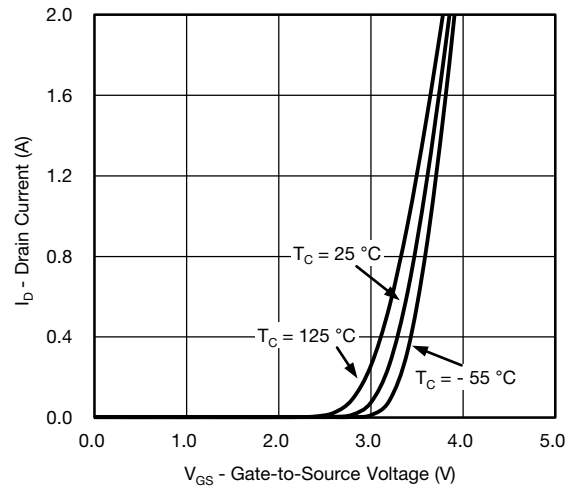
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



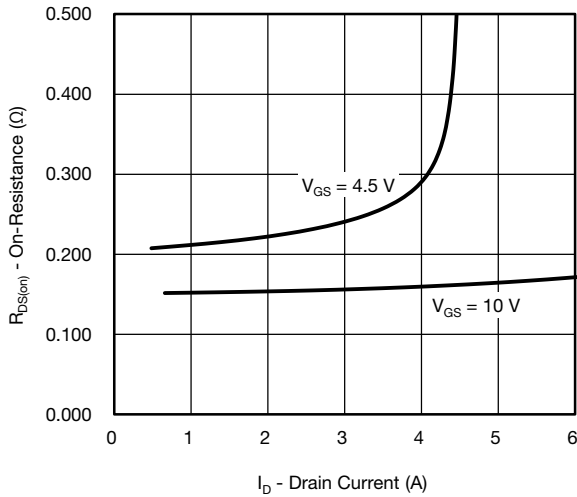
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



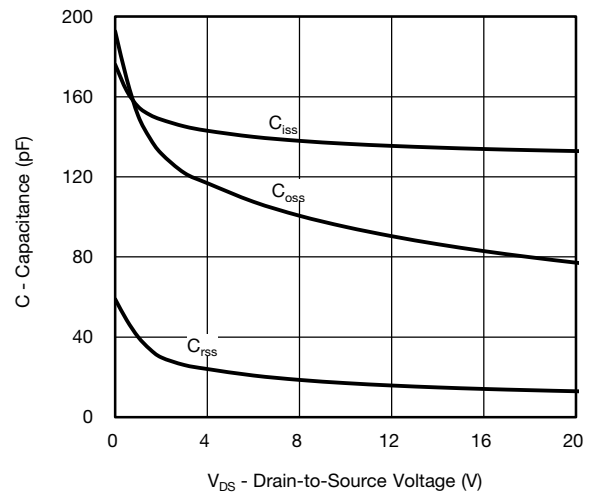
Output Characteristics



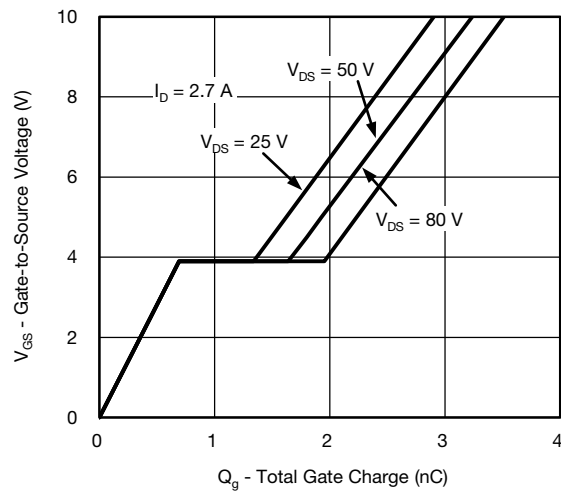
Transfer Characteristics



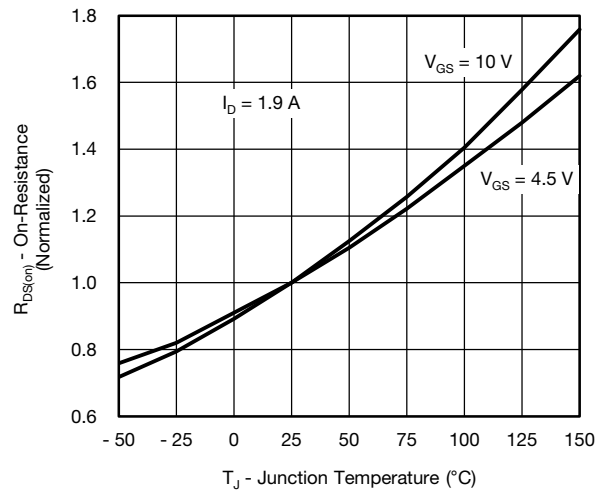
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



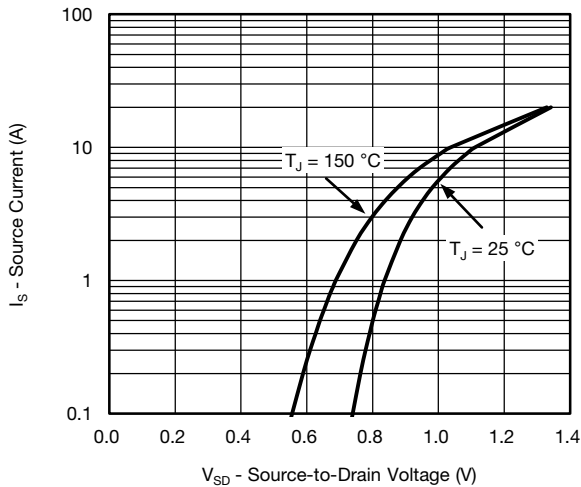
Gate Charge



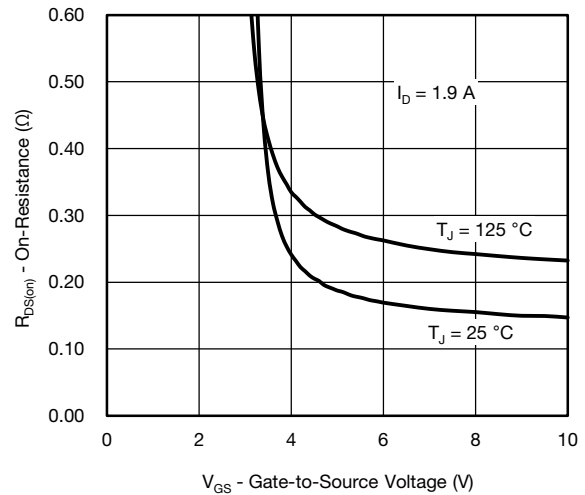
On-Resistance vs. Junction Temperature



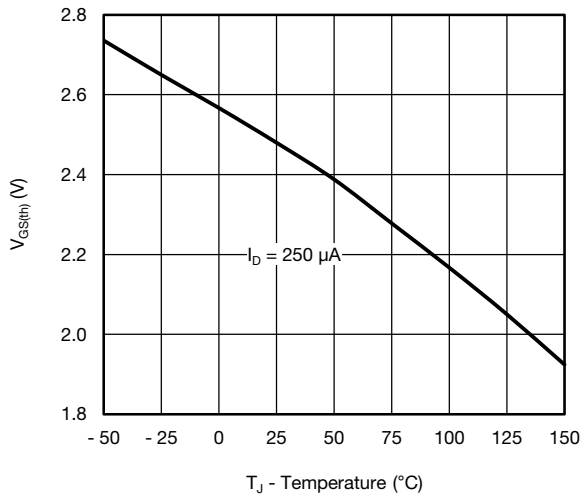
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



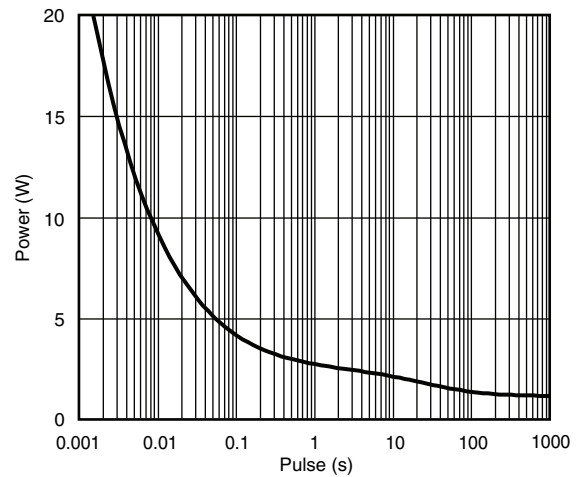
Source-Drain Diode Forward Voltage



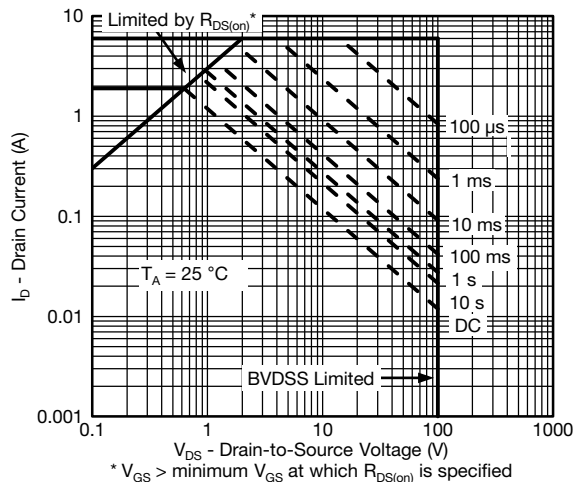
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



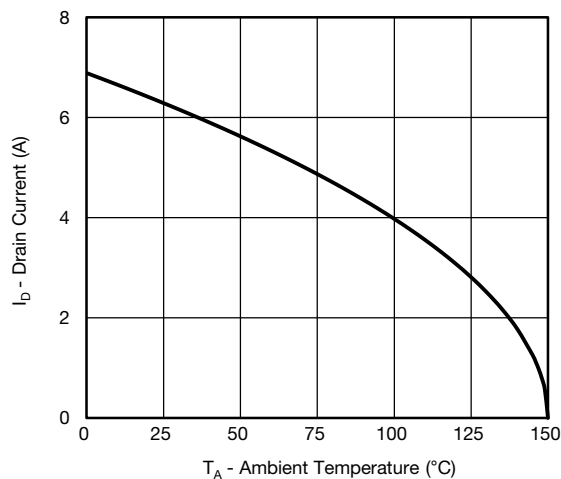
Single Pulse Power, Junction-to-Ambient



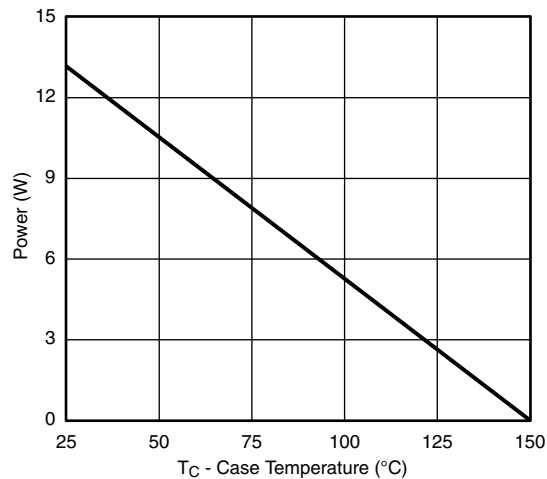
Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*

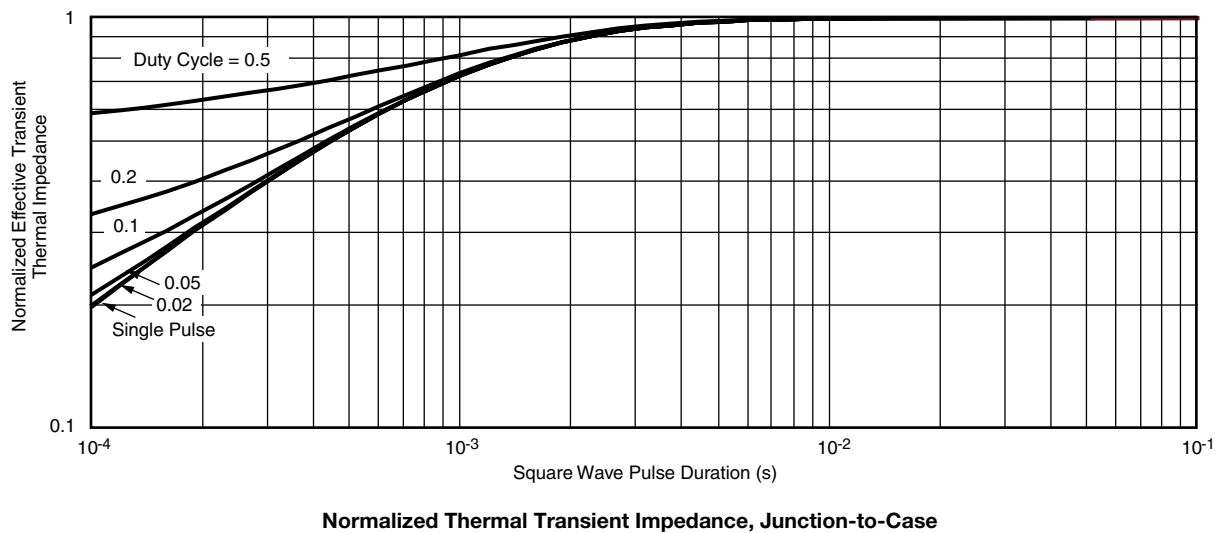
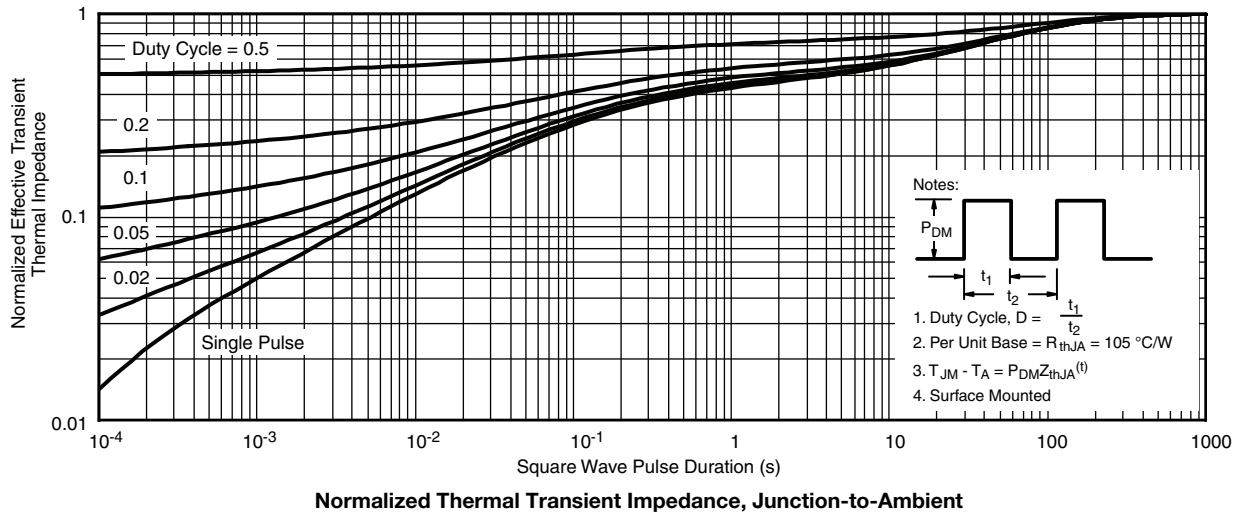


Power Derating

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62715.



PowerPAK® SC75-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



Notes:

1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021
D2	0.10	0.20	0.30	0.004	0.008	0.012						
E	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028
E2	0.20	0.25	0.30	0.008	0.010	0.012						
E3	0.32	0.37	0.42	0.013	0.015	0.017						
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
K	0.180 TYP			0.007 TYP			0.245 TYP			0.010 TYP		
K1	0.275 TYP			0.011 TYP			0.320 TYP			0.013 TYP		
K2	0.200 TYP			0.008 TYP			0.200 BSC			0.008 TYP		
K3	0.255 TYP			0.010 TYP								
K4	0.300 TYP			0.012 TYP								
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014
T							0.03	0.08	0.13	0.001	0.003	0.005

ECN: C-07431 – Rev. C, 06-Aug-07
DWG: 5935

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC75-6L Single



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