

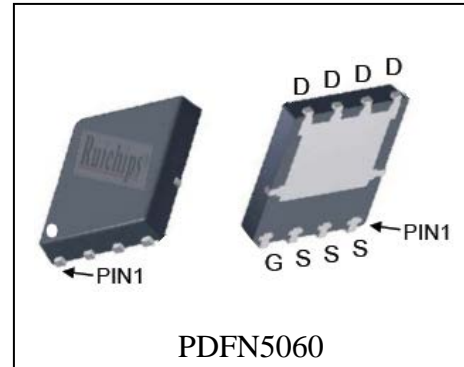
Features

- 30V/98A,
 $R_{DS(ON)} = 1.7m\Omega(Typ.) @ V_{GS} = 10V$
 $R_{DS(ON)} = 3.2m\Omega(Typ.) @ V_{GS} = 4.5V$
- Super High Dense Cell Design
- Reliable and Rugged
- 100% avalanche tested
- Lead Free and Green Devices Available (RoHS Compliant)

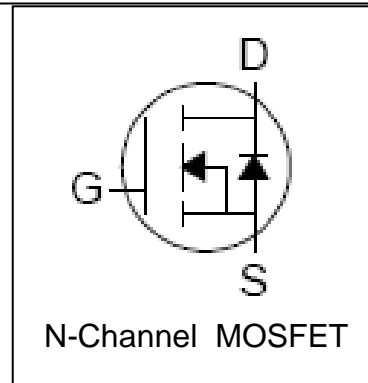
Applications

- DC/DC Conversion
- Switching Application

Pin Description



PDFN5060



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit	
Common Ratings ($T_C = 25^\circ C$ Unless Otherwise Noted)				
V_{DSS}	Drain-Source Voltage	30	V	
V_{GSS}	Gate-Source Voltage	± 20		
T_J	Maximum Junction Temperature	150	$^\circ C$	
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$	
I_S	Diode Continuous Forward Current	$T_C = 25^\circ C$	50	A
Mounted on Large Heat Sink				
I_{DP}	300 μs Pulse Drain Current Tested	$T_C = 25^\circ C$	380 ^②	A
I_D	Continuous Drain Current ($V_{GS} = 10V$)	$T_C = 25^\circ C$	98 ^①	A
		$T_C = 100^\circ C$	68 ^①	
		$T_A = 25^\circ C$	29 ^③	
		$T_A = 70^\circ C$	23 ^③	
P_D	Maximum Power Dissipation	$T_C = 25^\circ C$	66	W
		$T_C = 100^\circ C$	26	
		$T_A = 25^\circ C$	4.2 ^③	
		$T_A = 70^\circ C$	2.7 ^③	

Mounted on Large Heat Sink			
$R_{\theta JC}$	Thermal Resistance-Junction to Case	1.9	$^{\circ}C/W$
$R_{\theta JA}^{(3)}$	Thermal Resistance-Junction to Ambient	30	$^{\circ}C/W$
Drain-Source Avalanche Ratings			
$E_{AS}^{(4)}$	Avalanche Energy, Single Pulsed	256	mJ

Electrical Characteristics ($T_C=25^{\circ}C$ Unless Otherwise Noted)

Symbol	Parameter	Test Condition	RU3090M			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30V, V_{GS}=0V$ $T_J=85^{\circ}C$			1 30	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1	-	3	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
$R_{DS(ON)}^{(5)}$	Drain-Source On-state Resistance	$V_{GS}=10V, I_{DS}=20A$		1.7	2.5	$m\Omega$
		$V_{GS}=4.5V, I_{DS}=20A$		3.2	5	$m\Omega$
Diode Characteristics						
$V_{SD}^{(5)}$	Diode Forward Voltage	$I_{SD}=20A, V_{GS}=0V$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD}=20A, dI_{SD}/dt=100A/\mu s$		46		ns
Q_{rr}	Reverse Recovery Charge			32		nC
Dynamic Characteristics ⁽⁶⁾						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1MHz$		2		Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=15V,$ Frequency=1.0MHz		3840		pF
C_{oss}	Output Capacitance			850		
C_{riss}	Reverse Transfer Capacitance			185		
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=15V, R_L=0.75\Omega,$ $I_{DS}=20A, V_{GEN}=10V,$ $R_G=3\Omega$		12		ns
t_r	Turn-on Rise Time			17		
$t_{d(OFF)}$	Turn-off Delay Time			35		
t_f	Turn-off Fall Time			9		
Gate Charge Characteristics ⁽⁶⁾						
Q_g	Total Gate Charge	$V_{DS}=24V, V_{GS}=10V,$ $I_{DS}=20A$		58		nC
Q_{gs}	Gate-Source Charge			11		
Q_{gd}	Gate-Drain Charge			20		

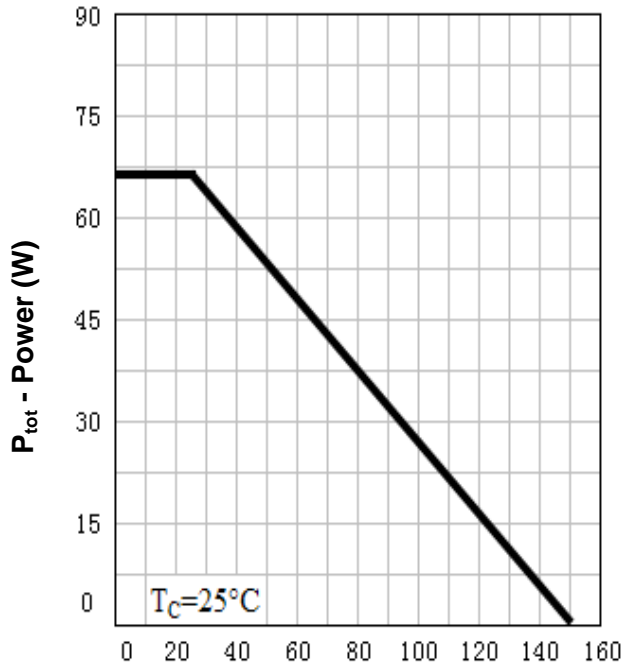
- Notes:
- ① Max current is limited to 50A by the package.
 - ② Pulse width limited by safe operating area.
 - ③ When mounted on 1 inch square copper board, $t \leq 10\text{sec}$.
 - ④ Limited by $T_{J\text{max}}$, $I_{AS} = 32\text{A}$, $V_{DD} = 24\text{V}$, $R_G = 50\Omega$, Starting $T_J = 25^\circ\text{C}$.
 - ⑤ Pulse test ; Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
 - ⑥ Guaranteed by design, not subject to production testing.

Ordering and Marking Information

Device	Marking	Package	Packaging	Quantity	Reel Size	Tape width
RU3090M	RU3090M	PDFN5060	Tape&Reel	3000	13''	12mm

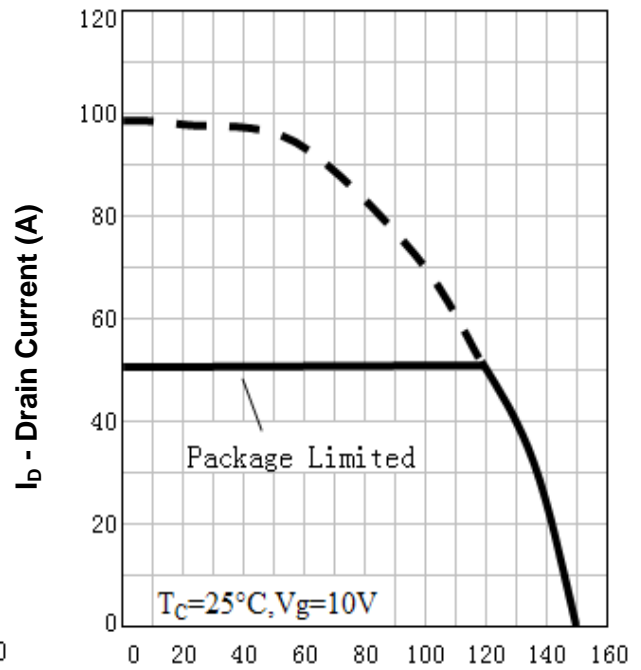
Typical Characteristics

Power Dissipation



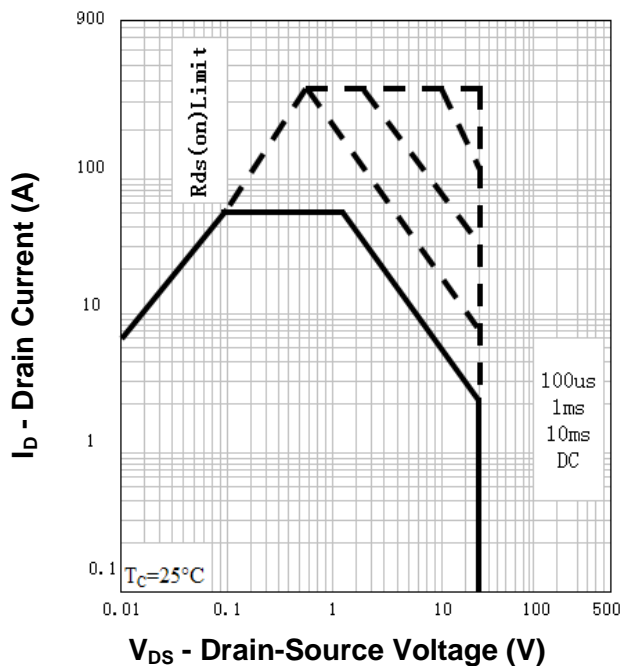
T_j - Junction Temperature (°C)

Drain Current

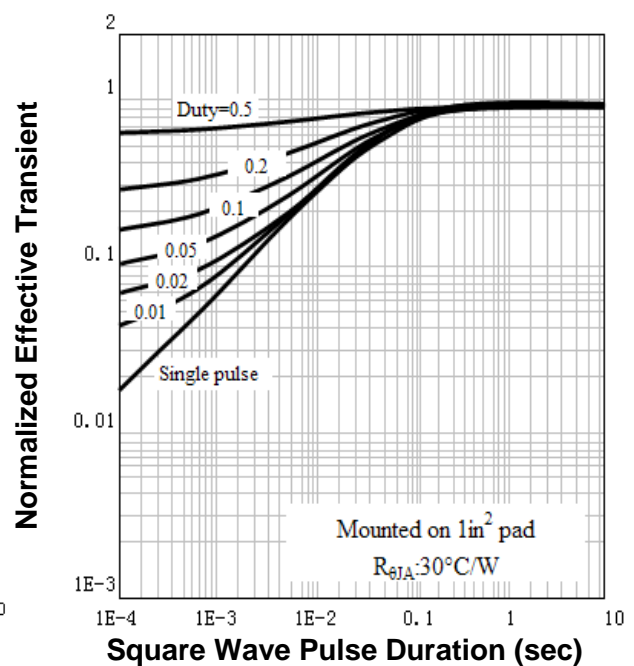


T_j - Junction Temperature (°C)

Safe Operation Area

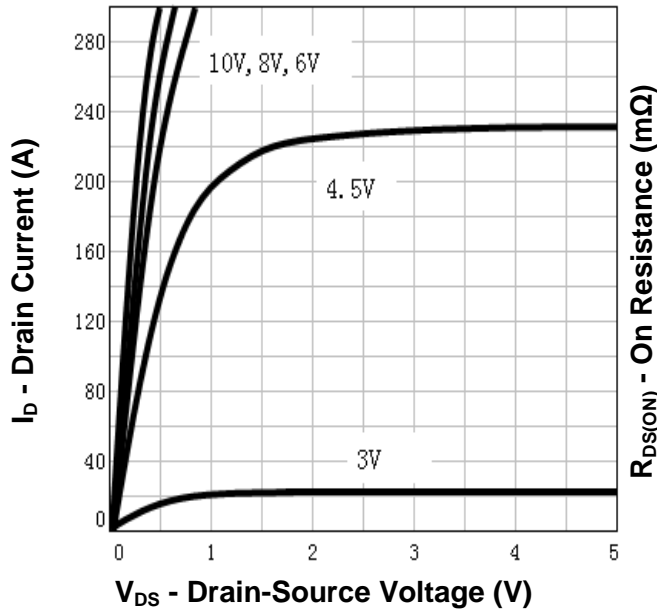


Thermal Transient Impedance

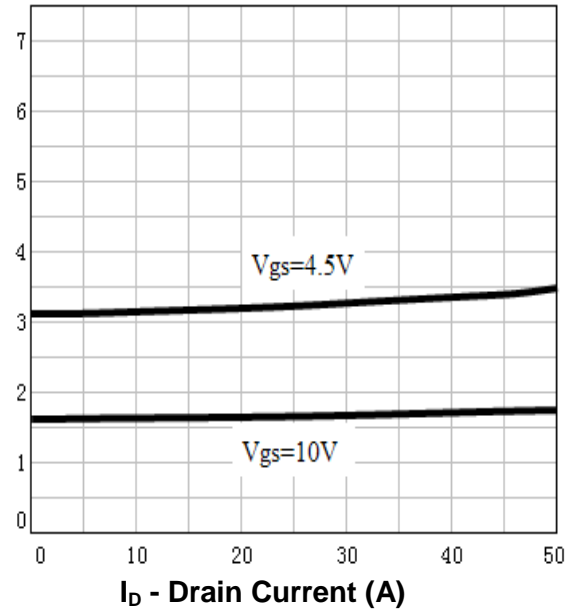


Typical Characteristics

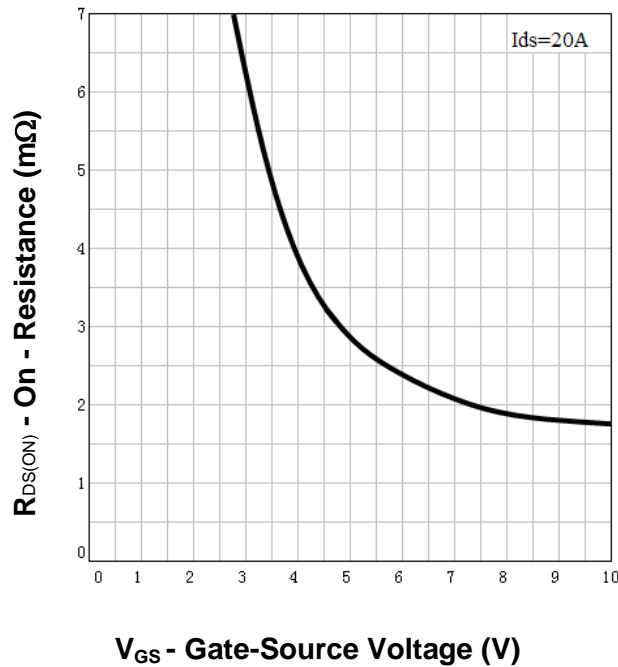
Output Characteristics



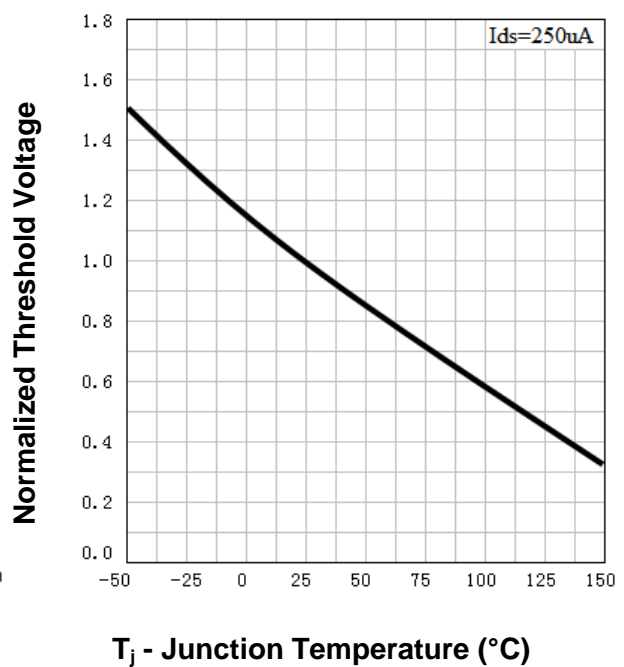
Drain-Source On Resistance



Drain-Source On Resistance

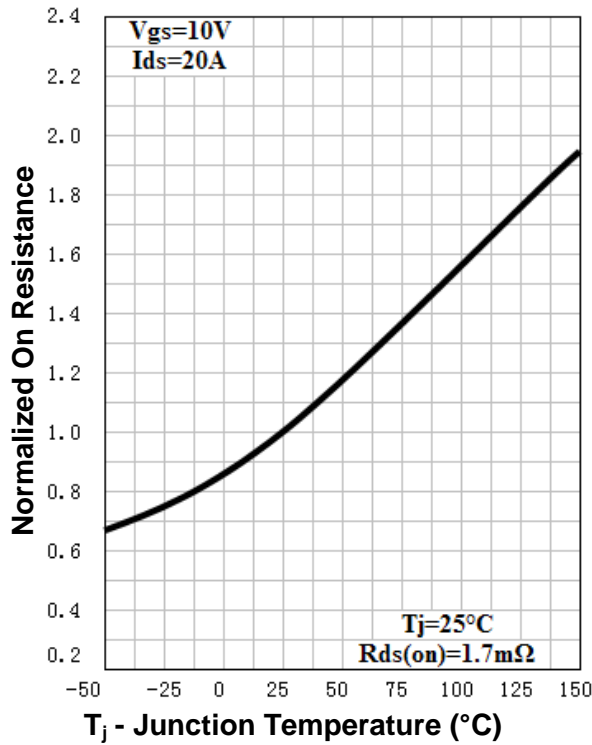


Gate Threshold Voltage

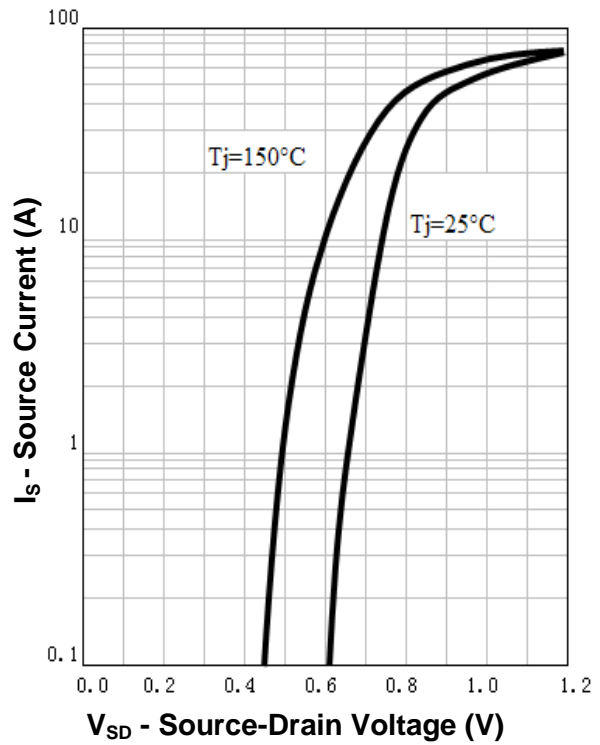


Typical Characteristics

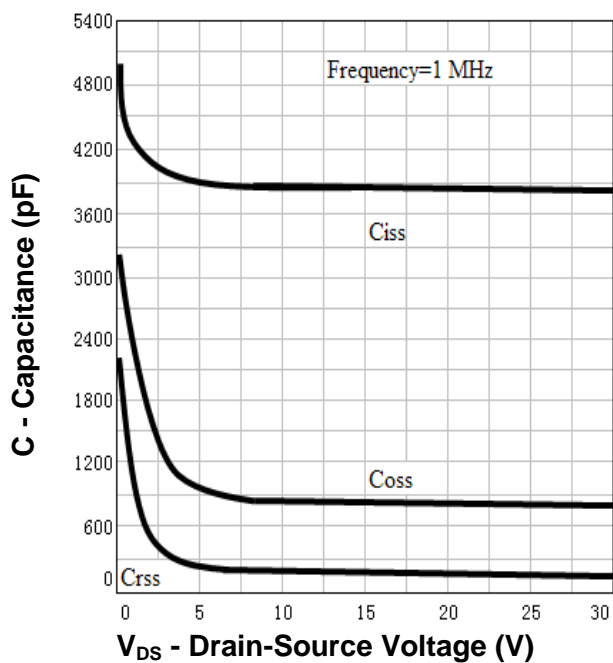
Drain-Source On Resistance



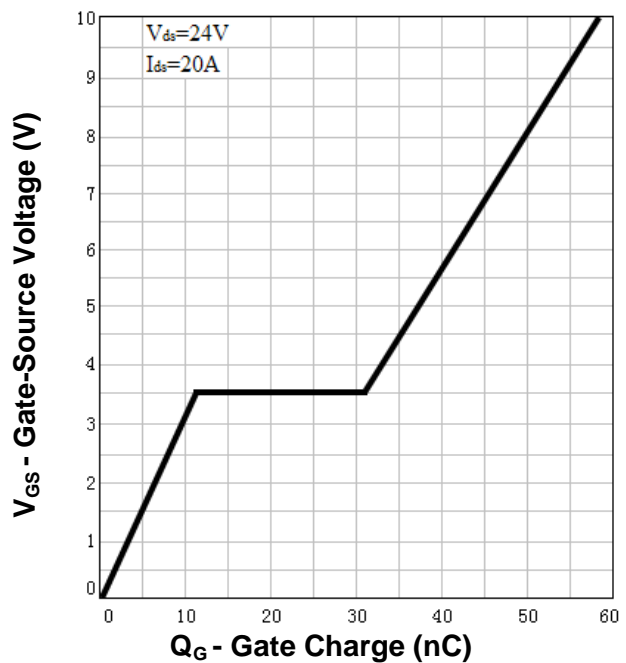
Source-Drain Diode Forward



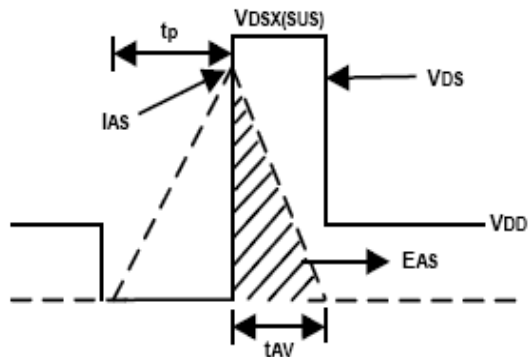
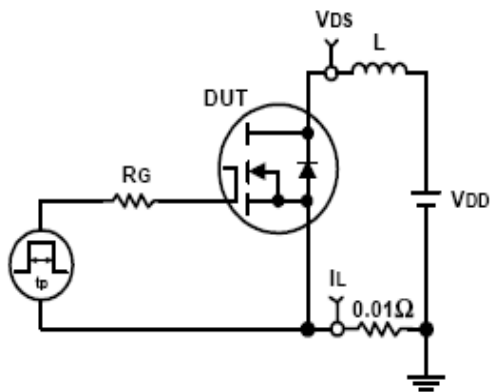
Capacitance



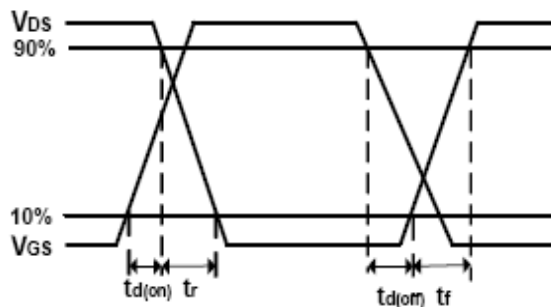
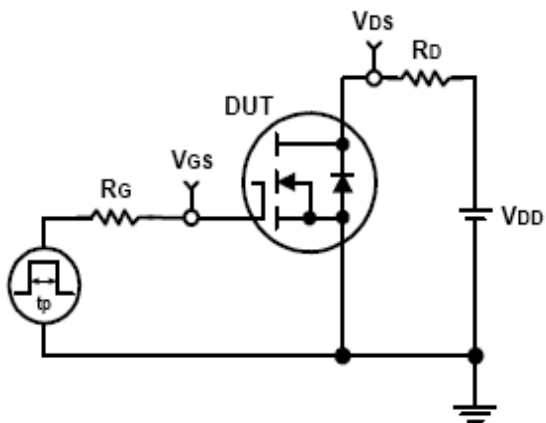
Gate Charge



Avalanche Test Circuit and Waveforms

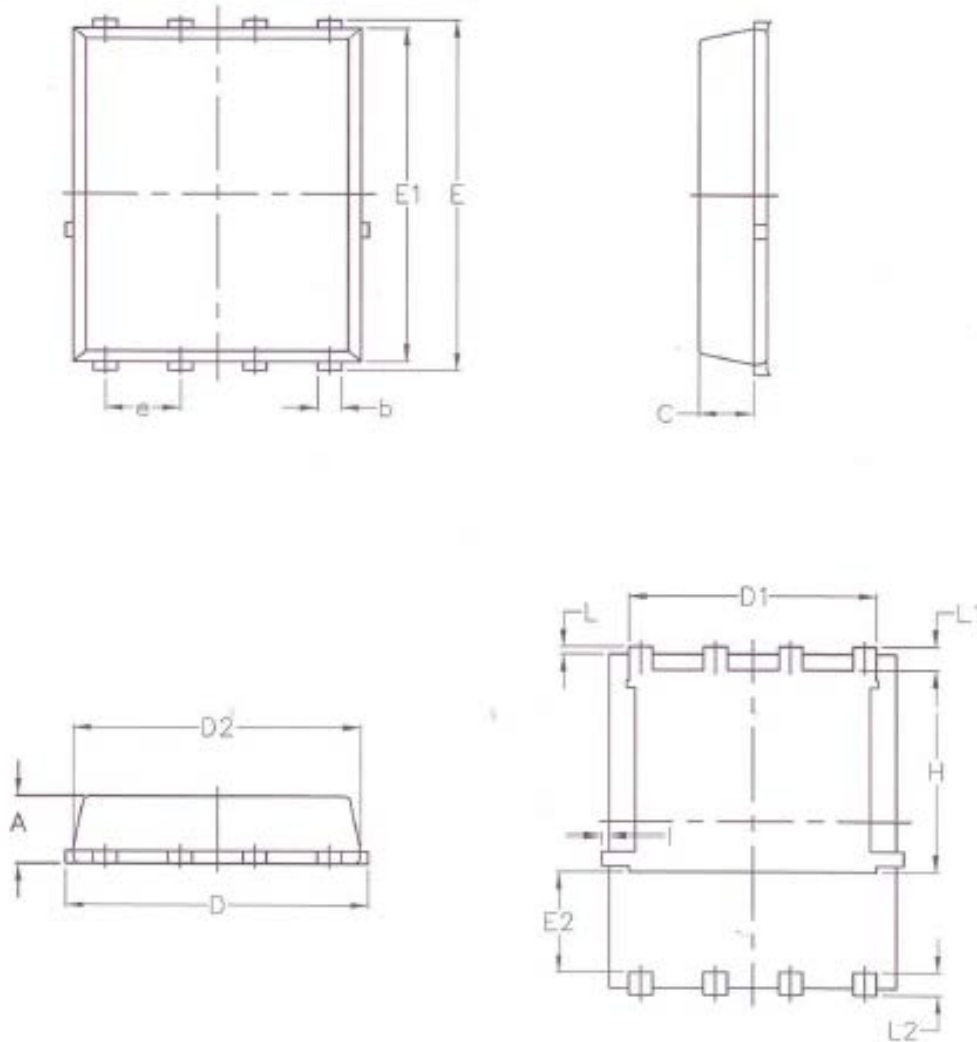


Switching Time Test Circuit and Waveforms



Package Information

PDFN5060



SYMBOL	MM		INCH		SYMBOL	MM		INCH	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	1.030	1.170	0.040	0.046	E2	1.600	-	0.063	-
b	0.340	0.480	0.013	0.019	e	1.270 BSC		0.050 BSC	
C	0.824	0.970	0.032	0.038	L	0.050	0.250	0.002	0.010
D	4.800	5.400	0.189	0.213	L1	0.380	0.500	0.015	0.020
D1	4.110	4.310	0.162	0.170	L2	0.380	0.500	0.015	0.020
D2	4.800	5.000	0.189	0.197	H	3.500	3.700	0.138	0.146
E	5.950	6.150	0.234	0.242	I	-	0.180	-	0.007
E1	5.650	5.850	0.222	0.230					

**ALL DIMENSIONS REFER TO JEDEC STANDARD
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS**

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