RDA5820NS

SINGLE-CHIP BROADCAST FM TRANSCEIVER

Rev.1.1–Mar.2011

1 General Description

The RDA5820NS is the newest generation single-chip broadcast FM receive/transmit tuner with fully integrated synthesizer, IF selectivity and MPX decoder. The chip uses the CMOS process, support multi-interface and require the least external component. The package size is 3X3mm and is completely adjustment-free. All these make it very suitable for portable devices.

The RDA5820NS has a powerful low-IF digital audio processor, this make it have optimum sound quality with varying reception conditions.

The RDA5820NS use RDA patented dual synthesizers, all digital transmit structure, this make it have perfectly transmition performance and agility.

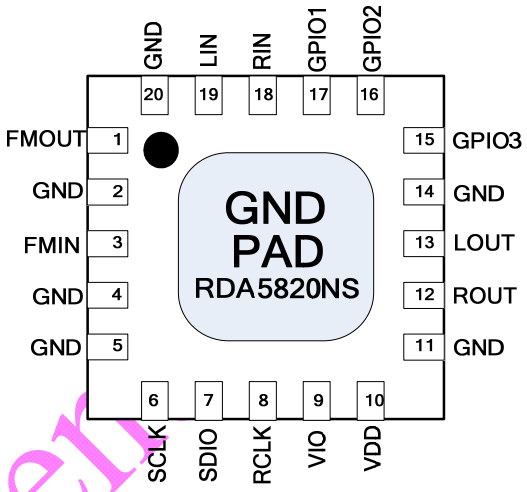


Figure 1-1. RDA5820NS Top View

The RDA5820NS support 50M~115M frequency band FM and RDS/RBDS receive and transmit, support power supply range is 1.8-5.5V, all these make it can be used in simple wireless control appliance such as mobile phone or toys.

The RDA5820NS package is pin-to-pin compatible with FM receive tuner RDA5802NS.

1.1 Features

- CMOS single-chip fully-integrated FM transceiver
- Low power consumption
  - Total current consumption is about 22mA at 3.0 V power supply (receive mode)
  - Total current consumption is about 26 mA at 3.0 V power supply (maximum power transmit mode)
- Support worldwide and campus frequency band
  - 50 -115 MHz
- Support flexible channel spacing mode
  - 100KHz, 200KHz, 50KHz and 25KHz
- Digital low-IF tuner
  - Image-reject down-converter
  - High performance A/D converter
  - IF selectivity performed internally
- Fully integrated digital frequency synthesizer
  - Fully integrated on-chip RF and IF VCO
  - Fully integrated on-chip loop filter
- All digital transmitter
- Autonomous search tuning
- Support RDS/RBDS receive and transmit
- Support SNR FM searching
- Support 32.768KHz crystal oscillator
- Digital auto gain control (AGC)
- Digital adaptive noise cancellation
  - Mono/stereo switch

  - Soft mute
  - High cut
- Programmable de-emphasis (50/75 μs)
- Receive signal strength indicator (RSSI) and SNR
- Bass boost
- Volume control
- Support I2S digital transmitter
- Support audio power amplifier (32Ω resistance loading)
- I^2S digital input / output interface
- Line-level analog output voltage
- 32.768 KHz, 12M,24M,13M,26M,19.2M,38.4MHz reference clock
- Only support IIC serial control bus interface
- Directly support 32Ω resistance loading
- Integrated LDO regulator
  - 1.8 to 5.5 V operation voltage
- 3X3mm 20 pin QFN package
- Pin-to-pin compatible with RDA5802NS

1.2 Applications

- Cellular handsets
- MP3, MP4 players
- Portable radios
- PDAs, Notebook PCs
- Wireless Toys

2 Table of Contents

3 Functional Description

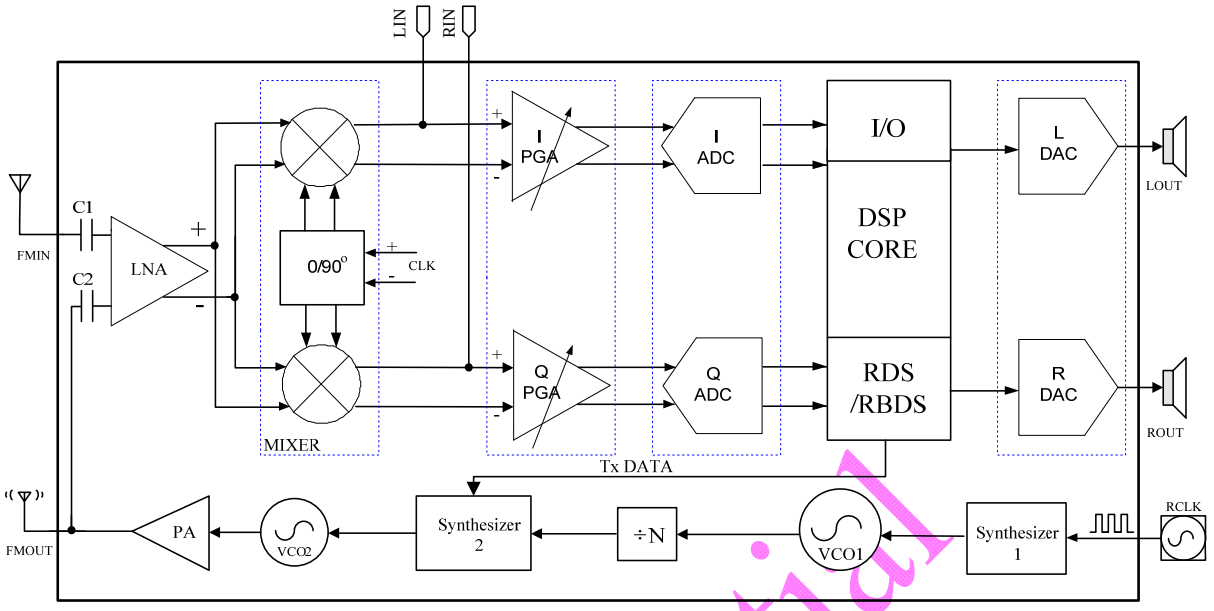


Figure 3-1. RDA5820NS FM Transceiver Block Diagram

3.1 FM Transceiver Structure

The RDA5820NS is a single-chip FM transceiver (Rx/Tx). Based on RDA patented dual synthesizers RF structure, it has perfectly FM receive and transmit performances, also least external components.

Except FM receive and transmit, the RDA5820NS also have RDS/RBDS, I2S input/output, audio amplify functions. All these make it very suitable for portable devices.

3.2 FM Receive

The receiver uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduces complexity, and integrates a low noise amplifier (LNA) supporting the FM broadcast band (50 to 115MHz), a quadrature image-reject mixer, a programmable gain control (PGA), a high resolution analog-to-digital converters (ADCs), an audio DSP and a high-fidelity digital-to-analog converters (DACs).

The LNA has differential input ports, which have same characters and anyone of them can used as FM signal input port. The two LNA ports can be arbitrary selected by set according registers bits (LNA_PORT_SEL[1:0]). It default input common mode voltage is GND.

The quadrature mixer down converts the LNA output differential RF signal to low-IF, it also has image-reject function.

The PGA amplifies the mixer output IF signal and then digitized with ADCs.

The DSP core finishes the channel selection, FM demodulation, stereo MPX decoder and output audio signal. The MPX decoder can autonomous switch from stereo to mono to limit the output noise.

The DACs convert digital audio signal to analog and change the volume at same time. The DACs has low-pass feature and -3dB frequency is about 30 KHz.

The PA (Power Amplifier) is power down. Its output impedance is high resistance.

3.3 FM Transmit

The transmit uses a digital modulate structure. Audio signals (LIN and RIN) are amplified by PGAs firstly, then converted to digital codes by ADCs. The DSP core finishes audio coding and FM modulate, pre-emphasis. The syntersizer2 transmits the digital FM data to VCO2. The PA (Power Amplifier) amplify the FM signal.

The PGA gain and PA gain are adjustable by set according registers bits (PGA_GAIN[2:0] [1]and PA_GAIN[5:0][2]).

Table 3-1 PGA_GAIN and Input Signal Strength

PGA_GAIN[2:0]	V-LIN(V_{PP})	PGA_GAIN[2:0]	V-LIN(V_{PP})
000	1.20V	100	0.075V
001	0.60V	101	0.037V
010	0.30V	110	0.018V
011	0.15V	111	0.009V

Table 3-2 PA_GAIN and Fm Transmit Power

PA_GAIN[5:0]	P_{OUT}	PA_GAIN[5:0]	P_{OUT}
111111	3dBm	011001	-3dBm
100111	0dBm	000000	-32dBm

3.4 Audio Amplify

Audio signals (LIN and RIN) can also directly send to audio amplifier in DACs and driving the headphone through LOUT and ROUT ports.

3.5 I2S Transmit

The RDA5820NS supports directly digital FM transmit. The digital signals can input through chip's ports GPIO1/2/3, then transmits directly through synthersizer2 and PA, also transimts to DAC and send out through LOUT and ROUT ports. I2S mode support slave mode.

3.6 PA

The PA (Power Amplifier) work frequency band is 50~115MHz, and output power is linearly adjustable. The PA use linear structure for better frequency distortion performance.

3.7 Synthesizer1

The frequency synthesizer 1 (including synthesizer1 and VCO1) generates the local oscillator signal which divide to quadrature, then be used to downconvert the RF input to a constant low intermediate frequency (IF). The synthesizer reference clock is 32.768 KHz.

The synthesizer1 frequency is defined by bits CHAN[9:0] with the range from 50MHz to 115MHz.

The synthesizer1 also generates reference to synthesizer2 under FM TX (transmit) mode.

3.8 Synthesizer2

The frequency synthesizer 2 (including synthesizer2 and VCO2) generates clock signals for ADC under FM RX (receive) mode.

The frequency synthesizer2 is also the FM transmit core. The digital signals (audio and RDS/RBDS) are directly added on it.

3.9 Power Supply

The RDA5820NS integrated one LDO which supplies power to the chip. The external supply voltage range is 1.8-5.5 V.

3.10 RESET and Control Interface select

The RDA5820NS is RESET itself When VIO is Power up. And also support soft reset by trigger 02H BIT1 from 0 to 1.

3.11 Control Interface

The RDA5820NS only supports I^2C control interface.

The I^2C interface is compliant to I^2C Bus Specification 2.1. It includes two pins: SCLK and

[1] Register 0x68H_BIT[12:10] PGA_GAIN_BIT[2:0]
[2] Register 0x41H_BIT[5:0] PA_GAIN_BIT[2:0]

SDIO. A I^{2}C interface transfer begins with START condition, a command byte and data bytes, each byte has a followed ACK (or NACK) bit, and ends with STOP condition. The command byte includes a 7-bit chip address (0010001b) and a R/W bit. The ACK (or NACK) is always sent out by receiver. When in write transfer, data bytes is written out from MCU, and when in read transfer, data bytes is read out from RDA5820NS.

3.12 I^{2}S Audio Data Interface

The RDA5820NS supports I^{2}S (Inter_IC Sound Bus) audio interface. The interface is fully compliant with I^{2}S bus specification. When setting I2SEN bit high, RDA5820NS will output SCK, WS, SD signals from GPIO3, GPIO1, GPIO2 as I^{2}S master and transmitter, the sample rate is 42Kbps.

3.13 GPIO Outputs

The RDA5820NS has three GPIOs. The function of GPIOs could programmed with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0] and I2SEN.

If I2SEN is set to low, GPIO pins could be programmed to output low or high or high-Z, or be programmed to output interrupt and stereo indicator with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0]. GPIO2 could be programmed to output a low interrupt (interrupt will be generated only with interrupt enable bit STCIEN is set to high) when seek/tune process completes. GPIO3 could be programmed to output stereo indicator bit ST. Constant low, high or high-Z functionality is available regardless of the state of VDD supplies or the ENABLE bit.

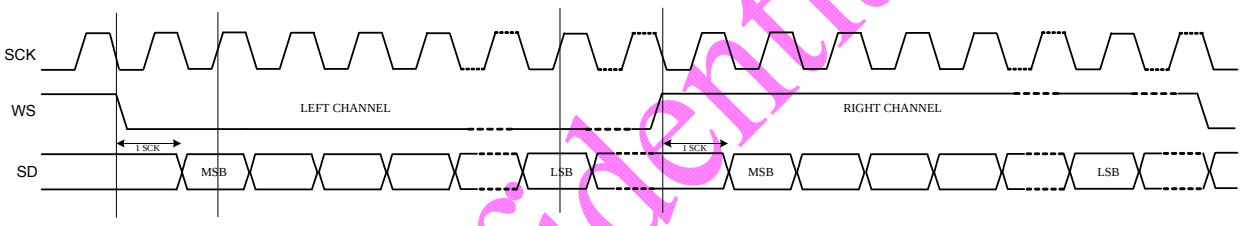


Figure 3-2. I2S Digital Audio Format

4 Electrical Characteristics

Table 4-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VDD	Supply Voltage	1.8	3.3	5.5	V
VIO	Interface Supply Voltage	1.5	-	3.6	V
T_{amb}	Ambient Temperature	-20	27	+70	℃
V_{IL}	CMOS Low Level Input Voltage	0		0.3*VIO	V
V_{IH}	CMOS High Level Input Voltage	0.7*VIO		VIO	V
V_{TH}	CMOS Threshold Voltage		0.5*VIO		V

Table 4-2 DC Electrical Specification (Absolute Maximum Ratings):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VIO	Interface Supply Voltage	-0.5		+4	V
T_{amb}	Ambient Temperature	-40		+90	°C
I_{IN}	Input Current (1)	-10		+10	mA
V_{IN}	Input Voltage(1)	-0.3		VIO+0.3	V
V_{lna}	LNA FM Input Level			0	dBm

Notes:

1. For Pin: SCLK, SDIO

Table 4-3 Power Consumption Specification

(VDD = 3 V, VIO=3 V, T_A =25℃, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITION	TYP	UNIT
FM Receive				
I_{VDD}	Supply Power Current	ENABLE=1	22	mA
I_{VIO}	Interface Supply Current	SCLK and RCLK inactive	200	μA
I_{APD}	Analog Powerdown Current	ENABLE=0	5	μA
I_{DPD}	Digital Powerdown Current	ENABLE=0	10	μA
FM Transmit				
I_{VDD}	Supply Power Current	PA_GAIN[5:0]=[111111];V_{RF}=3dBm	26	mA
I_{VDD}	Supply Power Current	PA_GAIN[5:0]=[100111];V_{RF}=0dBm	25	mA
I_{VDD}	Supply Power Current	PA_GAIN[5:0]=[011001];V_{RF}=3dBm	24.5	mA
I_{VDD}	Supply Power Current	PA_GAIN[5:0]=[000000];V_{RF}=-32dBm	23	mA

5 Receiver Characteristics

Table 5-1 Receiver Characteristics

(VDD = 3 V, VIO=3 V, T_A = 25 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
General Specifications							
F_{in}	FM Input Frequency Range	Adjust BAND Register		50		115	MHz
V_{rf}	Sensitivity[1,2,3]	S/N=26dB	50MHz	-	1.5		μV EMF
			65MHz	-	1.2		
			88MHz	-	1.2		
			98MHz	-	1.2		
			108MHz	-	1.3		
IF_{rej}	IF Rejection			40			dB
I_{image_rej}	Image Rejection			40			dB
$IP3_{in}$	Input IP3[4]	AGCD=1		80		-	dBμV
α_{am}	AM Suppression[1,2]	m=0.3		60	-	-	Db
S_{200}	Adjacent Channel Selectivity	±200KHz		50	70	-	Db
S_{400}	400KHz Selectivity	±400KHz		60	85		
V_{AFL}; V_{AFR}	Audio L/R Output Voltage (Pins LOUT and ROUT)	Volume [3 :0] =1111			420		mV
S/N	Maximum Signal to Noise Ratio[1,2,3,5]		Mono[2]	55	57	-	dB
			Stereo[6]	53	55		
α_{SCS}	Stereo Channel Separation			35	-	-	dB
R_L	Audio Output Loading Resistance	Single-ended		32	-	-	Ω
THD	Audio Total Harmonic Distortion[1,3,6]	Volume[3:0]=1111	R_{load}=1KΩ		0.03	0.05	%
			R_{load}=32Ω				
α_{AOI}	Audio Output L/R Imbalance[1,6]			-	-	0.05	dB
R_{mute}	Mute Attenuation Ratio[1]	Volume[3:0]=0000		60	-	-	dB
BW_{audio}	Audio Response[1]	1KHz=0dB ± 3dB point	Low Freq[9]		100		Hz
			High Freq		14		
Pins FMIN,FMOUT, LOUT, ROUT,LIN,RIN							
V_{com_fmin}	Pins FMIN Input Common Mode Voltage				0		V
V_{com_fmout}	Pin FMOUT Common Mode Voltage				0		V
V_{com_in}	Pins LIN/RIN Input Common Mode Voltage				1.1		V
V_{com}	Audio Output Common Mode Voltage[8]			0.95	1.	1.05	V

Notes:

1. F_{in}=65 to 115MHz; F_{mod}=1KHz; de-emphasis=75μs; MONO=1; L=R unless noted otherwise;
2. ∆f=22.5KHz;
3. B_{AF} = 300Hz to 15KHz, RBW <=10Hz;
4. $|f_2-f_1|$>1MHz, $f_0=2xf_1-f_2$, AGC disable, F_{in}=76 to 108MHz;
5. $P_{RF}=60dB_UV$;
6. ∆f=75KHz.
7. Measured at V_{EMF} = 1 m V, f_{RF} = 76 to 108MHz
8. At LOUT and ROUT pins
9. Adjustable

6 Transmitter Characteristics

Table 6-1 Transmitter Characteristics

(VDD = 3 V, VIO=3 V, T_A = 25 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
F_{rf}	Transmit Frequency		50		115	MHz
$_{\triangle}F$	Transmit Frequency Accuracy and Stability[2,3]			2.6		KHz
V_{RF}	Maximum Transmit Voltage	PA_GAIN=[111111]		3		dBm
V_{RF}	Minimum Transmit Voltage	PA_GAIN=[000000]		-32		dBm
	Transmit Voltage Step			3		dBm
	Transmit Voltage Stability			1		dB
	Transmit Channel Edge Power	>±100KHz Pre-emphasis off			-85	dBc
	Transmit Adjacent Channel Power	>±200KHz Pre-emphasis off			-85	dBc
	Transmit Alternate Channel Power	>±400KHz Pre-emphasis off			-85	dBc
	Transmit Emissions	In band(76 to 108MHz)			-50	dBc
	Pre-emphasis Time Constant	TX_PREMPHASIS=75 us	70	75	80	us
		TX_PREMPHASIS=50 us	45	50	55	us
	Audio SNR Mono	$_{\triangle}$f=22.5KHz, Mono Limiter off	50	55		dB
	Audio SNR Stereo	$_{\triangle}$f=22.5KHz, $_{\triangle}$fpolit=6.75KHz, Stereo Limiter off	51	55		dB
	Audio THD Mono	$_{\triangle}$f=75KHz, Mono Limiter off		0.08	0.6	%
	Audio THD Stereo	$_{\triangle}$f=68.25KHz, $_{\triangle}$fpolit=6.75KHz, Stereo Limiter off		0.08	0.6	%
	Audio Stereo Separation			40		dB
SCR	Sub Carrier Rejection Ratio			27		dB
	Power up Setting Time				30	ms
	Input Signal Level				1	V_{PK}
	Frequency Flatness	Mono, ±1.5dB, $_{\triangle}$f=75KHz, 0, 50, 75us pre-emphasis, limiter off	30		15K	Hz

	High-Pass Frequency Response	Mono, -3dB, △f=75KHz, 0, 50, 75us pre-emphasis, limiter off	5		30	Hz
	Low-Pass Frequency Response	Mono, -3dB, △f=75KHz, 0, 50, 75us pre-emphasis, limiter off	15k		16k	Hz
	Audio Imbalance	Mono	-1		1	dB
	Pilot Modulation Rate Accuracy	△f=68.25KHz, $\triangle f_{pilot}$=6.75KHz, Stereo	-10		10	%
	Audio Modulation Rate Accuracy	△f=68.25KHz, $\triangle f_{pilot}$=6.75KHz, Stereo	-10		10	%
	Input Resistance		10	15	20	KΩ
	Input Capacitance		0.5	0.7	1	pF

Notes:

1. F_{in}=65 to 115MHz; F_{mod}=1KHz; de-emphasis=75μs; MONO=1; L=R unless noted otherwise;
2. Guaranteed by Characterization only ;
3. No measurable $\triangle f_{RF}/\triangle V_{DD}$ at $\triangle V_{DD}$ of 500mV pk-pk at 100HZ to 10KHz;

Serial Interface

6.1 I²C Interface Timing

Table 6-1 I²C Interface Timing Characteristics

(VDD = 3 V, VIO=3 V, T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCLK Frequency	f_{scl}		0	-	400	KHz
SCLK High Time	t_{high}		0.6	-	-	μs
SCLK Low Time	t_{low}		1.3	-	-	μs
Setup Time for START Condition	$t_{su:sta}$		0.6	-	-	μs
Hold Time for START Condition	$t_{hd:sta}$		0.6	-	-	μs
Setup Time for STOP Condition	$t_{su:sto}$		0.6	-	-	μs
SDIO Input to SCLK↑ Setup	$t_{su:dat}$		100	-	-	ns
SDIO Input to SCLK↓ Hold	$t_{hd:dat}$		0	-	900	ns
STOP to START Time	t_{buf}		1.3	-	-	μs
SDIO Output Fall Time	$t_{f:out}$		$20+0.1C_b$	-	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{r:in}$ / $t_{f:in}$		$20+0.1C_b$	-	300	ns
Input Spike Suppression	t_{sp}		-	-	50	ns
SCLK, SDIO Capacitive Loading	C_b		-	-	50	pF
Digital Input Pin Capacitance					5	pF

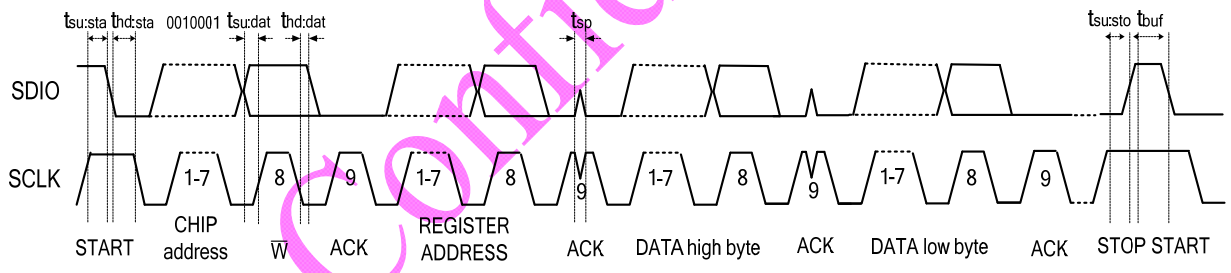


Figure 6-1. I²C Interface Write Timing Diagram

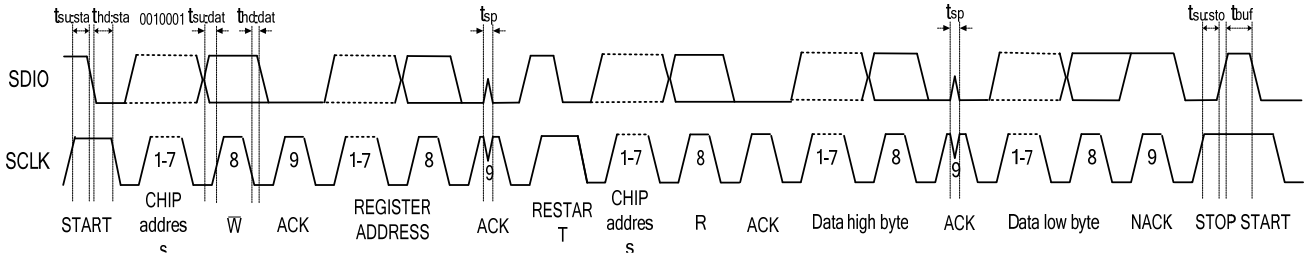


Figure 6-2. I²C Interface Read Timing Diagram

7 Register Definition

REG	BITS	NAME	FUNCTION	DEFAULT
00H	15:0	CHIPID[15:0]	Chip ID.	0x5820
02H	15	DHIZ	Audio Output High-Z Disable. *0 = High impedance; 1 = Normal operation*	0
	14	DMUTE	Mute Disable. *0 = Mute; 1 = Normal operation*	0
	13	MONO	Mono Select. *0 = Stereo; 1 = Force mono*	0
	12	BASS	Bass Boost. *0 = Disabled; 1 = Bass boost enabled*	0
	11	RCLK NON-CALIBRATE MODE	0=RCLK clock is always supply 1=RCLK clock is not always supply when FM work (when 1, RDA5820NS can't directly support -20℃~70℃ temperature. Only suppory ±20℃ temperature swing from tune point)	0
	10	RCLK DIRECT INPUT MODE	1=RCLK clock use the directly input mode	0
	9	SEEKUP	Seek Up. *0 = Seek down; 1 = Seek up*	0
	8	SEEK	Seek. *0 = Disable stop seek; 1 = Enable* *Seek begins in the direction specified by* SEEKUP *and ends when a channel is found, or the entire band has been searched.* *The* SEEK *bit is set low and the* STC *bit is set high when the seek operation completes.*	0
	7	SKMODE	Seek Mode 0 = wrap at the upper or lower band limit and continue seeking 1 = stop seeking at the upper or lower band limit	0
	6:4	CLK_MODE[2:0]	000=32.768kHz 001=12Mhz 101=24Mhz 010=13Mhz 110=26Mhz 011=19.2Mhz 111=38.4Mhz	000
	3	RDS_EN	RDS/RBDS enable If 1, RDS/RBDS enable	0
	2	RSVD	Reserved	0
	1	SOFT_RESET	Soft reset. If 0, not reset; If 1, reset.	0

REG	BITS	NAME	FUNCTION	DEFAULT
	0	ENABLE	Power Up Enable. *0 = Disabled; 1 = Enabled*	0
03H	15:6	CHAN[9:0]	Channel Select. BAND = *0* *Frequency* = *Channel Spacing (kHz) x* CHAN+ *87.0 MHz* BAND = *1or 2* *Frequency* = *Channel Spacing (kHz) x* CHAN + *76.0 MHz* BAND = *3* *Frequency* = *Channel Spacing (kHz) x* CHAN + *65.0 MHz* CHAN *is updated after a seek operation.*	0x00
	5	DIRECT MODE	Directly Control Mode, Only used when test.	0
	4	TUNE	Tune 0 = Disable 1 = Enable The tune operation begins when the TUNE bit is set high. The STC bit is set high when the tune operation completes. The tune bit is reset to low automatically when the tune operation completes..	0
	3:2	BAND[1:0]	Band Select. 00 = 87–108 MHz (US/Europe) 01 = 76–91 MHz (Japan) 10 = 76–108 MHz (world wide) 11[3] = 65 –76 MHz （East Europe） or 50-65MHz	00
	1:0	SPACE[1:0]	Channel Spacing. 00 = 100 kHz 01 = 200 kHz 10 = 50kHz 11 = 25KHz	00
04H	15	RDSIEN	RDS ready Interrupt Enable. 0 = Disable Interrupt 1 = Enable Interrupt Setting STCIEN = 1 will generate a low pulse on GPIO2 when the interrupt occurs.	0
	14	STCIEN	Seek/Tune Complete Interrupt Enable. 0 = Disable Interrupt 1 = Enable Interrupt Setting STCIEN = 1 will generate a low pulse on GPIO2 when the interrupt occurs.	0
	13	RBDS	1 = RBDS mode enable 0 = RDS mode only	0
	12	RDS_FIFO_EN	1 = RDS fifo mode enable.	0

[3] If 0x07h_bit[9] (band)=1, 65-76MHz; =0, 50-76MHz

REG	BITS	NAME	FUNCTION	DEFAULT
	11	DE	De-emphasis. *0 = 75 μs; 1 = 50 μs*	0
	10	RDS_FIFO_CLR	1 = clear RDS fifo	1
	9	SOFTMUTE_EN	If 1, softmute enable	1
	8	AFCD	AFC disable. If 0, afc work; If 1, afc disabled.	0
	7	RSVD	Reserved	0
	6	I2S_ENABLED	I2S bus enable If 0, disabled; If 1, enabled.	0
	5:4	GPIO3[1:0]	General Purpose I/O 3. *00 = High impedance* *01 = Mono/Stereo indicator (ST)* *10 = Low* *11 = High*	00
	3:2	GPIO2[1:0]	General Purpose I/O 2. *00 = High impedance* *01 = Interrupt (INT)* *10 = Low* *11 = High*	00
	1:0	GPIO1[1:0]	General Purpose I/O 1. *00 = High impedance* *01 = Reserved* *10 = Low* *11 = High*	00
05H	15	INT _MODE	If 0, generate 5ms interrupt; If 1, interrupt last until read reg0CH action occurs.	1
	14:13	SEEK_MODE[1:0]	01= adjacent seek process && noise condition 10= adjacent seek process || noise condition	00
	12	RSVD	Reserved	0
	11:8	SEEKTH[3:0][4] (inverse of noise_h_th<3:0>)	Seek SNR threshold value: Noise_th(dB) = 79 – seek_th	1000
	7:6	LNA_PORT_SEL[1:0]	LNA input port selection bit: 00: no input 01: LNAN 10: LNAP 11: dual port input	10
	5:4	RSVD	Reserved	00
	3:0	VOLUME[3:0]	DAC Gain Control Bits (Volume). 0000=min; 1111=max Volume scale is logarithmic When 0000, output mute and output impedance is very large	1111

[4] The default noise threshold is 71dB.

REG	BITS	NAME	FUNCTION	DEFAULT
06H	15:13	RSVD	reserved	000
	12	I2S_MODE[5]	If 0, master mode; If 1, slave mode.	0
	11	SW_LR[3]	Ws relation to l/r channel. If 0, ws=0 ->r, ws=1 ->l; If 1, ws=0 ->l, ws=1 ->r.	10
	10	SCLK_I_EDGE[3]	When I2S enable If 0, use normal sclk internally; If 1, inverte sclk internally.	0
	9	DATA_SIGNED[3]	If 0, I2S output unsigned 16-bit audio data. If 1, I2S output signed 16-bit audio data.	0
	8	WS_I_EDGE[3]	If 0, use normal ws internally; If 1, inverte ws internally.	0
	7:4	I2S_SW_CNT[4:0][3] (Only valid in master mode)	4'b1000: WS_STEP_48; 4'b0111: WS_STEP=44.1kbps; 4'b0110: WS_STEP=32kbps; 4'b0101: WS_STEP=24kbps; 4'b0100: WS_STEP=22.05kbps; 4'b0011: WS_STEP=16kbps; 4'b0010: WS_STEP=12kbps; 4'b0001: WS_STEP=11.025kbps; 4'b0000: WS_STEP=8kbps;	0000
	3	SW_O_EDGE[3]	If 1, invert ws output when as master.	0
	2	SCLK_O_EDGE[3]	If 1, invert sclk output when as master.	0
	1	L_DELY[3]	If 1, L channel data delay 1T.	0
	0	R_DELY[3]	If 1, R channel data delay 1T.	0
07H	15	RSVD	Must be 0	0
	14:10	TH_SOFRBLEND[5:0]	Softblend threshold setting for noise. If (127-noise_db2)>4*th, turn soft blend off.	10011
	9	65M_50M MODE	Valid when band[1:0] = 2'b11 (0x03H_bit<3:2>) 1 = 65~76 MHz; 0 = 50~76 MHz.	1
	8	RSVD	Reserved	0
	7:2	SEEK_TH_OLD[6]	Seek threshold for old seek mode, Valid when Seek_Mode=01	000000
	1	SOFTBLEND_EN	If 1, Softblend enable	1
	0	FREQ_MODE	If 1, then freq setting changed. Freq = 76000(or 87000) kHz + freq_direct (08H) kHz.	0
0AH	15	RDSR	RDS ready 0 = No RDS/RBDS group ready(default) 1 = New RDS/RBDS group ready	0
	14	STC	Seek/Tune Complete. 0 = Not complete 1 = Complete	0

3 This function is open when I2S_Enabled=1.

[6] 0x05H_bit[14:13], SEEK_MODE register. Default value is 00; When = 01, will add the 5802E seek mode.

REG	BITS	NAME	FUNCTION	DEFAULT
			The seek/tune complete flag is set when the seek or tune operation completes.	
	13	**SF**	**Seek Fail.** ***0 = Seek successful; 1 = Seek failure*** ***The seek fail flag is set when the seek operation fails to find a channel with an RSSI level greater than SEEKTH[5:0].***	0
	12	**RDSS**	**RDS Synchronization** **0 = RDS decoder not synchronized(default)** **1 = RDS decoder synchronized** **Available only in RDS Verbose mode**	**0**
	11	**BLK_E**	**When RDS enable:** **1 = Block E has been found** **0 = no Block E has been found**	**0**
	10	**ST**	**Stereo Indicator.** ***0 = Mono; 1 = Stereo*** ***Stereo indication is available on GPIO3 by setting GPIO3[1:0] =01.***	1
	9:0	**READCHAN[9:0]**	**Read Channel.** **BAND = 0** **Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 87.0 MHz** **BAND = 1 or 2** **Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 76.0 MHz** **BAND = 3** **Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 65.0 MHz** **READCHAN[9:0] is updated after a tune or seek operation.**	**8'h00**
0BH	**15:9**	**RSSI[6:0]**	**RSSI.** **000000 = min** **111111 = max** **RSSI scale is logarithmic.**	**0**
	8	**FM TRUE**	**1 = the current channel is a station** **0 = the current channel is not a station**	**0**
	7	**FM_READY**	**1=ready** **0=not ready**	**0**
	6:5	**RSVD**	**Reserved**	**00**
	4	**ABCD_E**	**1= the block id of register 0cH,0dH,0eH,0fH is E** **0= the block id of register 0cH, 0dH, 0eH,0fH is A, B, C, D**	**0**
	3:2	**BLERA[1:0]**	**Block Errors Level of RDS_DATA_0, and is always read as Errors Level of RDS BLOCK A (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)** **00= 0 errors requiring correction** **01= 1~2 errors requiring correction** **10= 3~5 errors requiring correction** **11= 6+ errors or error in checkword, correction not**	**00**

REG	BITS	NAME	FUNCTION	DEFAULT
			possible. Available only in RDS Verbose mode	
	1:0	BLERB[1:0]	Block Errors Level of RDS_DATA_1, and is always read as Errors Level of RDS BLOCK B (in RDS mode) or E (in RBDS mode when ABCD_E flag is 1). 00= 0 errors requiring correction 01= 1~2 errors requiring correction 10= 3~5 errors requiring correction 11= 6+ errors or error in checkword, correction not possible. Available only in RDS Verbose mode	00
0CH	15:0	RDSA[15:0]	BLOCK A (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)	16'h5820
0DH	15:0	RDSB[15:0]	BLOCK B (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)	16'h5820
0EH	15:0	RDSC[15:0]	BLOCK C (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)	16'h5805
0FH	15:0	RDSD[15:0]	BLOCK D (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)	16'h5805
40H	15:4	RSVD	Reserved	16'h000
	3:0	WORK MODE	0000 = FM Receive 0001 = FM Transmit 1000 = Audio Amplify 1100 = Codec 1110 = ADC	0000
41H	15:12	RSVD	Reserved	0000
	11:9	TXPA_VCOM[2:0]	TXPA Common Voltage	000
	8:6	TXPA_IBIT[2:0]	TXPA Bias Current	111
	5:0	TXPA_GAIN[5:0]	TXPA Gain Bit	000000
67H	15:8	FMTX_PILOT_DEV[7:0]	FM Transmit Pilot Tone Modulate Parameter	16'h0E
	7:0	FMTX_RDS_ DEV[7:0]	FM Transmit RDS Signal Modulate Parameter	16'h10
68H	<15:13>	RSVD	Reserved	00
	<12:10>	FMTX_PGA_GAIN	FM Transmit PGA Gain Bit	001
	<9:8>	FMTX_ADC_GAIN	FM Transmit ADC Gain Bit	000
	<7:0>	FMTX_AUDIO_DEV<7:0>	FM Transmit Audio Signal Modulate Parameter	16'hF0

8 Pins Description

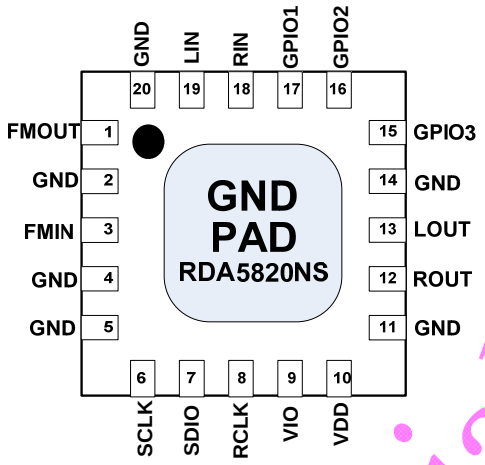
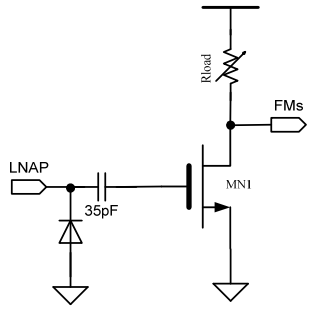
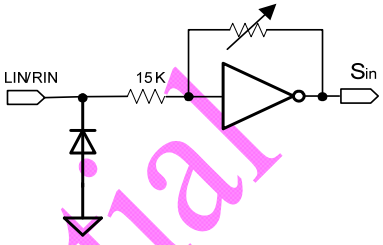
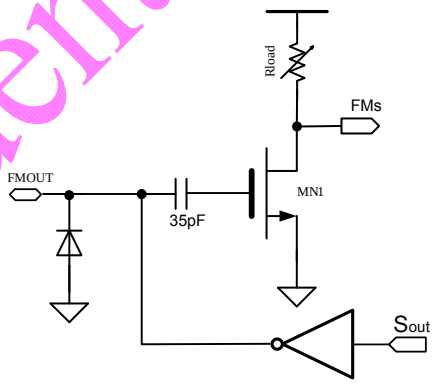
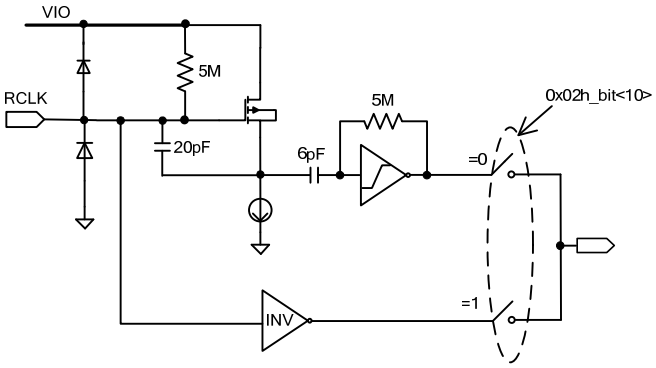


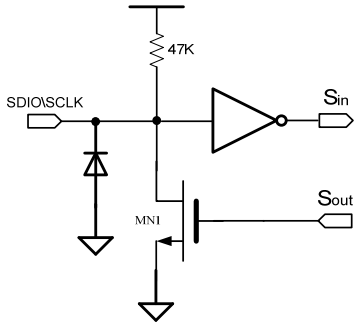
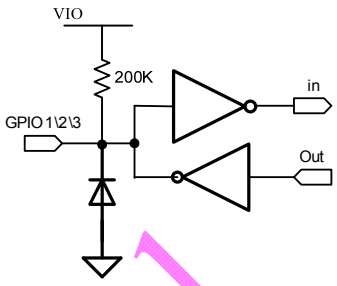
Figure 8-1. RDA5820NS Top View

Table 8-1 RDA5820NS Pins Description

SYMBOL	PIN	DESCRIPTION
GND	2,4,5,11,14,20,21	Ground. Connect to ground plane on PCB
FMIN	3	FM LNAP input port.
FMOUT	1	.FM output port and LNAN input port
SCLK	6	Clock input for serial control bus
SDIO	7	Data input/output for serial control bus
RCLK	8	32.768KHz crystal oscillator and reference clock input
VIO	9	Power supply for I/O
VDD	10	Power supply for analog and digital section
ROUT,LOUT	12,13	Right/Left audio output port
RIN,LIN	18,19	Right/Left audio input port
GPIO1/2/3	17,16,15	General purpose input/output

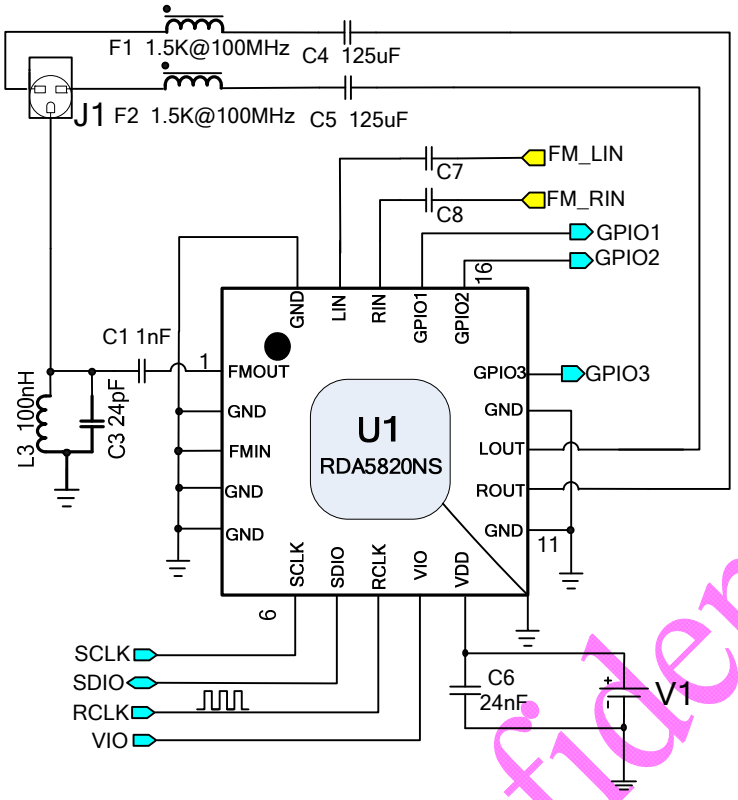
Table 8-2 Internal Pin Configuration

SYMBOL	PIN	DESCRIPTION
FMIN	4	
RIN/LIN	17/18	
FMOUT	1	
RCLK	8	

SCLK/SDIO	9/10	
GPIO1/GPIO2/GPIO3	17/16/15	

9 Application Diagram

9.1 RDA5820NS Common Application Diagram:



Notes:

1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5820NS Chip;
3. VDD: Power Supply (1.8~5.5V);
4. C7/C8: Audio Input Couple Capacitance;
5. FM Choke (L3 and C3) for Audio Common;
6. C1: Fm Antenna Couple Capacitor
7. Place C6 Close to VDD pin.
8. Ferrite F1/F2 should close to J1.

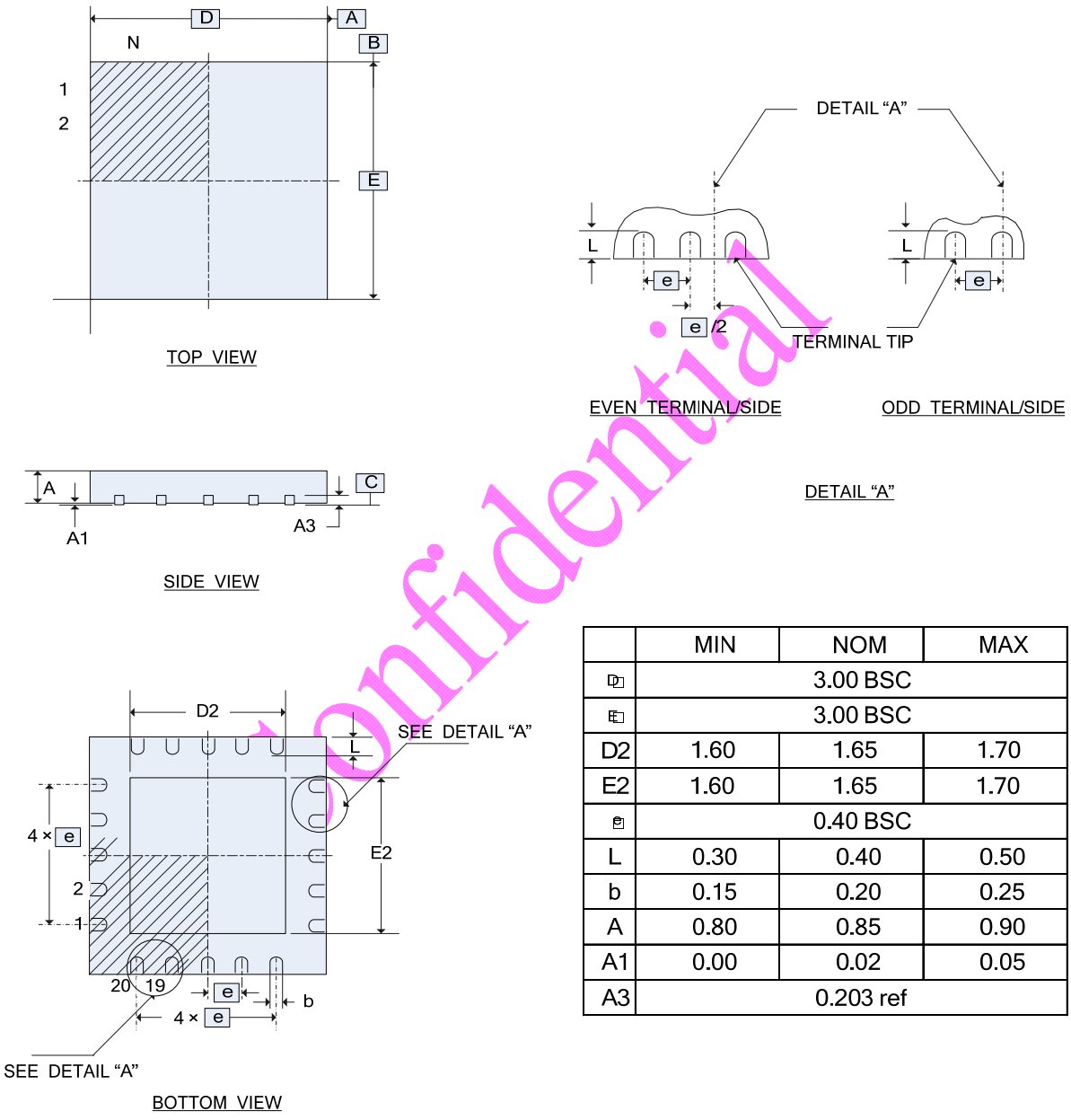
Figure 9-1. RDA5820NS FM Transceiver Application Diagram (TCXO Application)

9.1.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5820NS	Broadcast FM Transceiver	RDA
J1		Common 32Ω Resistance Headphone	
F1/F2	1.5K@100MHz	FM Band Ferrite	Murata
C1	1nF	FM Antenna Couple Capacitor	Murata
C7/C8	0.22uF	Audio Couple Capacitors	Murata
L3/C3	100nH/24pF	LC Chock for LNA Input	Murata
C4,C5	125μF	Audio AC Couple Capacitors	Murata
C6	24nF	Power Supply Bypass Capacitor	Murata

10 Package Physical Dimension

Figure 10-1 illustrates the package details for the RDA5820NS. The package is lead-free and RoHS-compliant.



	MIN	NOM	MAX
D		3.00 BSC	
E		3.00 BSC	
D2	1.60	1.65	1.70
E2	1.60	1.65	1.70
e		0.40 BSC	
L	0.30	0.40	0.50
b	0.15	0.20	0.25
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 ref	

Figure 10-2. 20-Pin 3x3 Quad Flat No-Lead (QFN)

11 PCB Land Pattern

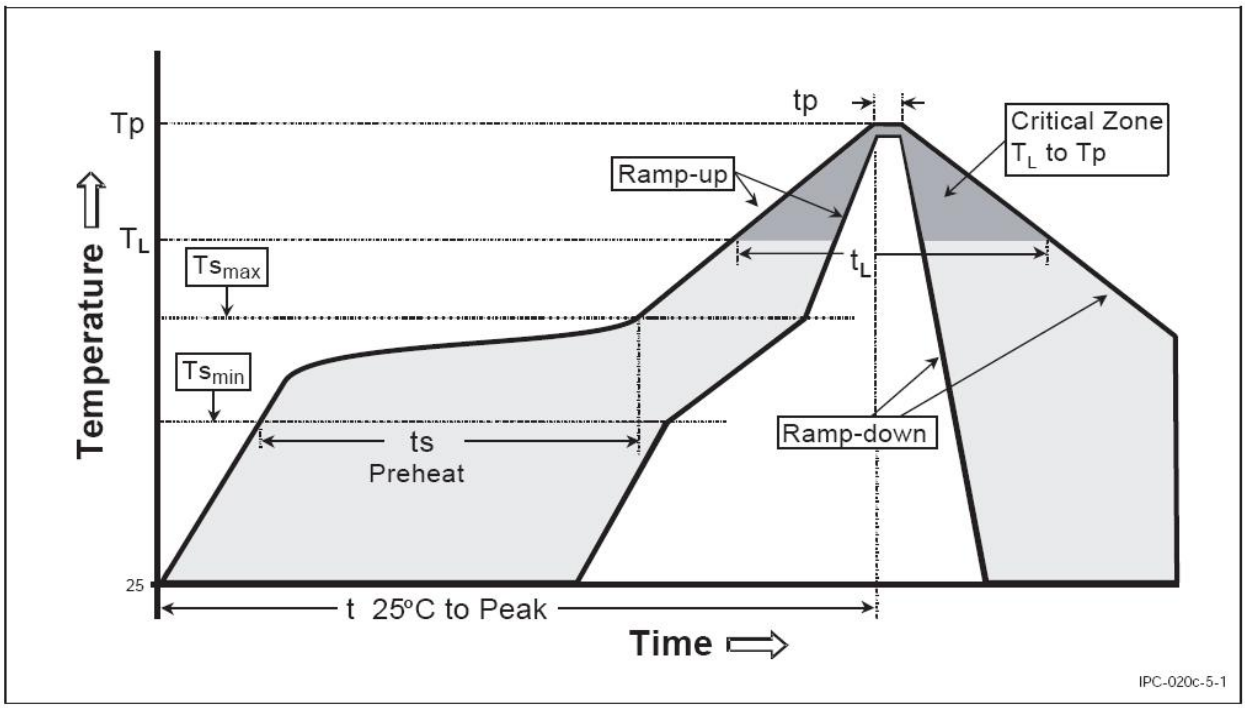


Figure 18.Classification Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T_{Smax} to T_p)	3 °C/second max.	3 °C/second max.
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (t_{smin} to t_{smax})	 100 °C 100 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	 183 °C 60-150seconds	 217°C 60-150 seconds
Peak /Classification Temperature(T_p)	See Table-II	See Table-III
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Table-I Classification Reflow Profiles

Package Thickness	Volume mm^3 <350	Volume mm^3 ⩾350
＜2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
⩾2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table – II SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 ＜350	Volume mm^3 350-2000	Volume mm^3 ＞2000
＜1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
⩾2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Table – III Pb-free Process – Package Classification Reflow Temperatures

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 ° C, - X ° C (based on machine variation capability)whatever

is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a “lead-free” assembly process **shall** be evaluated using the “lead free” classification temperatures and profiles defined in Table-I II III whether or not lead free.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

12 Change List

REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	2011-03-14	Chun Zhao, Yanan Liu	Original Draft.
V1.1	2011-03-24	Chun Zhao, Kai Wang	

13 Notes：

14 Contact Information

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