DESCRIPTION

PT6964 is an LED Controller driven on a 1/5 to 1/8 duty factor. 10 segment output lines, 4 grid output lines, 3 segment/ grid output lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to PT6964 via a three-line serial interface. Housed in a 28 pins SOP Package, PT6964 pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

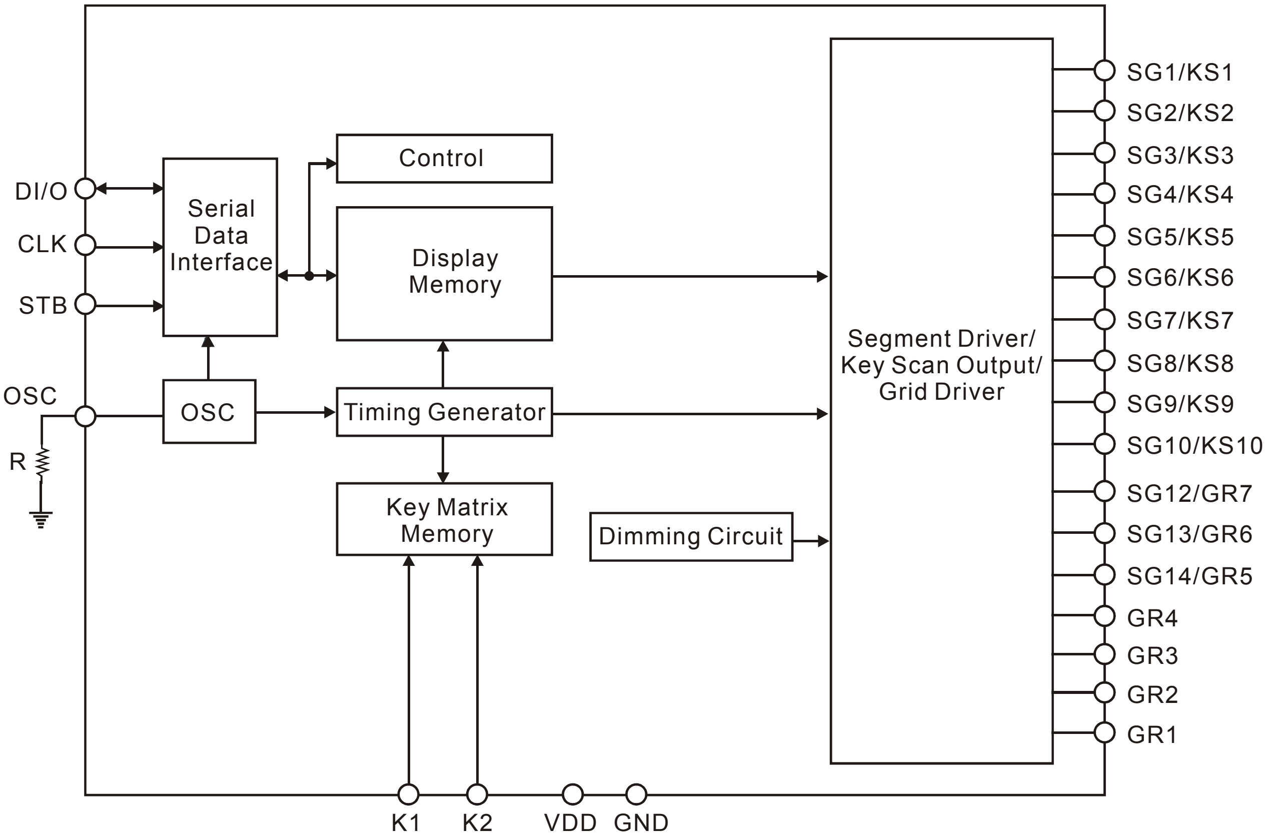
FEATURES

- CMOS technology
- Low power consumption
- Multiple display modes (10 segment, 7 grid to 13 segment, 4 grid)
- Key scanning (10 x 2 Matrix)
- 8-step dimming circuitry
- Serial interface for clock, data input, data output, strobe pins
- Available in 28 pins, SOP

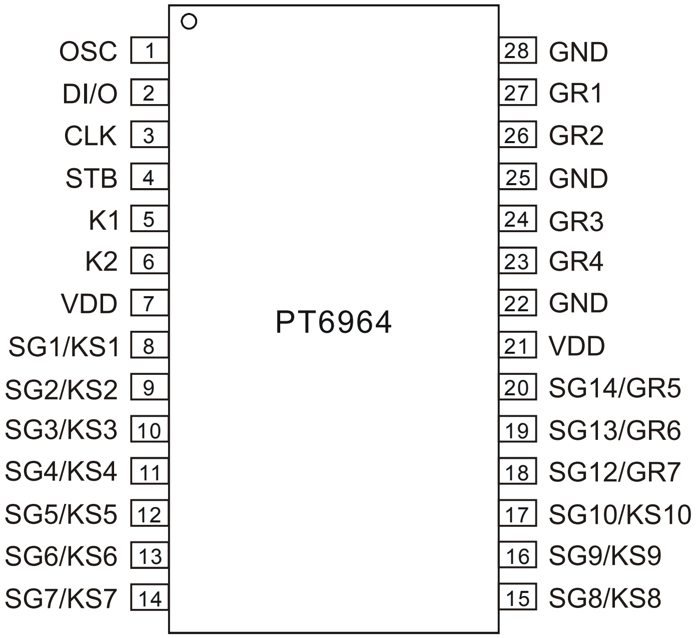
APPLICATIONS

- Micro-computer peripheral device
- VCR set
- Combo set

BLOCK DIAGRAM


DI/O
CLK
STB
OSC
R
Serial Data Interface
Control
Display Memory
OSC
Timing Generator
Key Matrix Memory
Dimming Circuit
Segment Driver/ Key Scan Output/ Grid Driver
SG1/KS1
SG2/KS2
SG3/KS3
SG4/KS4
SG5/KS5
SG6/KS6
SG7/KS7
SG8/KS8
SG9/KS9
SG10/KS10
SG12/GR7
SG13/GR6
SG14/GR5
GR4
GR3
GR2
GR1
K1
K2
VDD
GND

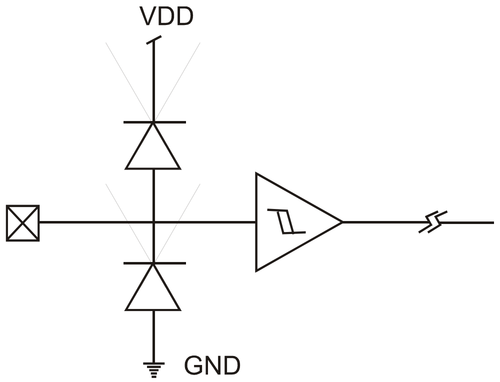
PIN DESCRIPTION


OSC 1
DI/O 2
CLK 3
STB 4
K1 5
K2 6
VDD 7
SG1/KS1 8
SG2/KS2 9
SG3/KS3 10
SG4/KS4 11
SG5/KS5 12
SG6/KS6 13
SG7/KS7 14
PT6964
28 GND
27 GR1
26 GR2
25 GND
24 GR3
23 GR4
22 GND
21 VDD
20 SG14/GR5
19 SG13/GR6
18 SG12/GR7
17 SG10/KS10
16 SG9/KS9
15 SG8/KS8

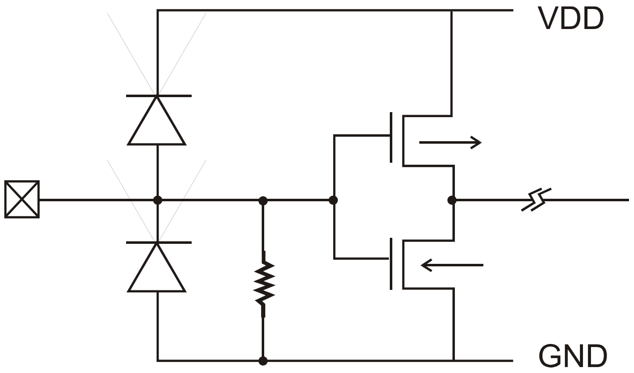
INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below.

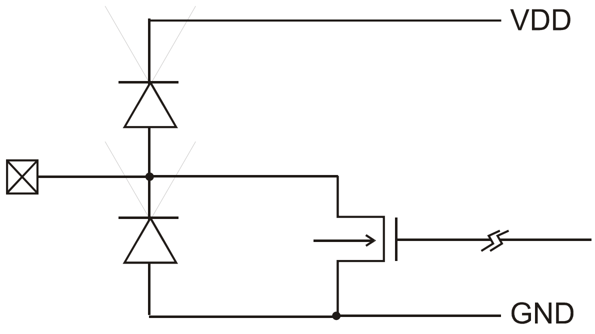
- **Input Pins: CLK, STB**



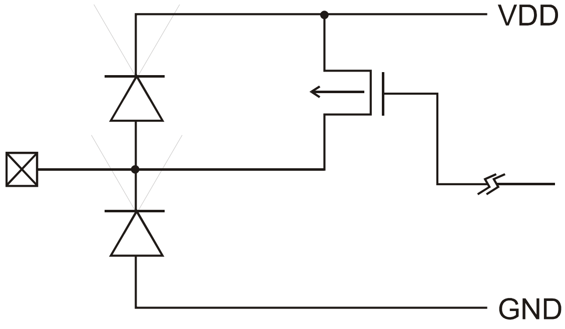
- **Input Pins: K1 to K2**



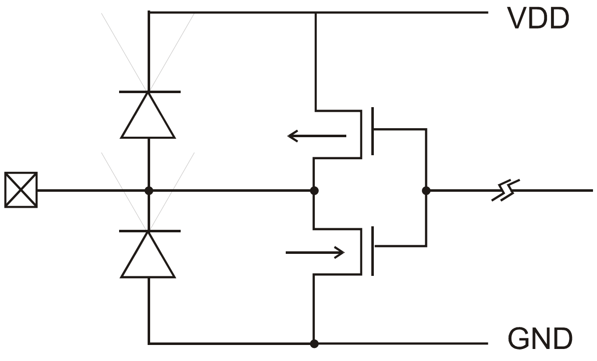
- **Output Pins: GR1 to GR4**



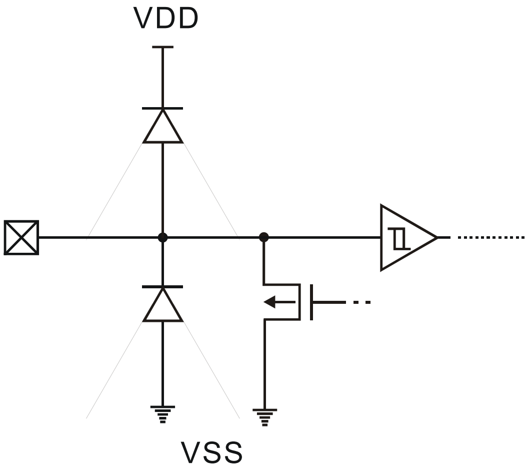
- **Output Pins: SG1/KS1 to SG10/KS10**



- **Output Pins: SG14/GR5, SG13/GR6 and SG12/GR7**



- **Input Pin & Output Pin: DI/O**



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency	1
DI/O	I/O	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit) Data Output Pin (N-Channel, Open-Drain)	2
CLK	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	3
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is HIGH", CLK is ignored.	4
K1 ~ K2	I	Key Data Input Pins The data sent to these pins are latched at the end of the display cycle. (Internal Pull-Low Resistor)	5, 6
GND	-	Ground Pin	22, 25, 28
SG1/KS1 ~ SG10/KS10	O	Segment Output Pins (p-channel, open drain) Also acts as the Key Source	8 ~ 17
SG12/GR7 ~ SG14/GR5	O	Segment / Grid Output Pins	18 ~ 20
VDD	-	Power Supply	7, 21
GR4 ~ GR1	O	Grid Output Pins	26, 27, 23, 24

FUNCTION DESCRIPTION

COMMANDS

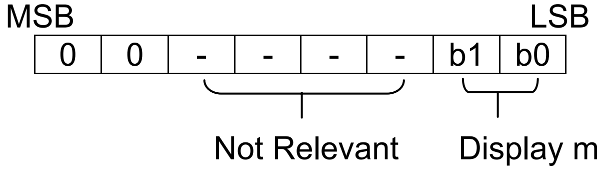
A command is the first byte (b0 to b7) inputted to PT6964 via the DI/O Pin after STB Pin has changed from HIGH to LOW State. If for some reason the STB Pin is set to HIGH while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMANDS 1: DISPLAY MODE SETTING COMMANDS

PT6964 provides 2 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6964 via the DI/O Pin when STB is LOW. However, for these commands, the bit 3 to bit 6 (b2 to b5) are ignored, bit 7 & bit 8 (b6 to b7) are given a value of 0.

The Display Mode Setting Commands determine the number of segments and grids to be used (10 to 13 segments, 7 to 4 grids). A display command ON must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned ON, the 7-grid, 10-segment modes is selected.



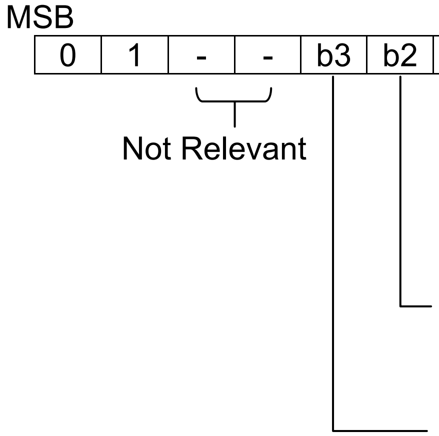
0	0	-	-	-	-	b1	b0

Display mode settings:
00: 4 digits, 13 segments
01: 5 digits, 12 segments
10: 6 digits, 11 segments
11: 7 digits, 10 segments

COMMANDS 2: DATA SETTING COMMANDS

The Data Setting Commands executes the Data Write or Data Read Modes for PT6964. The data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of 1 while bit 8 (b7) is given the value of 0. Please refer to the diagram below.

When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of 0.



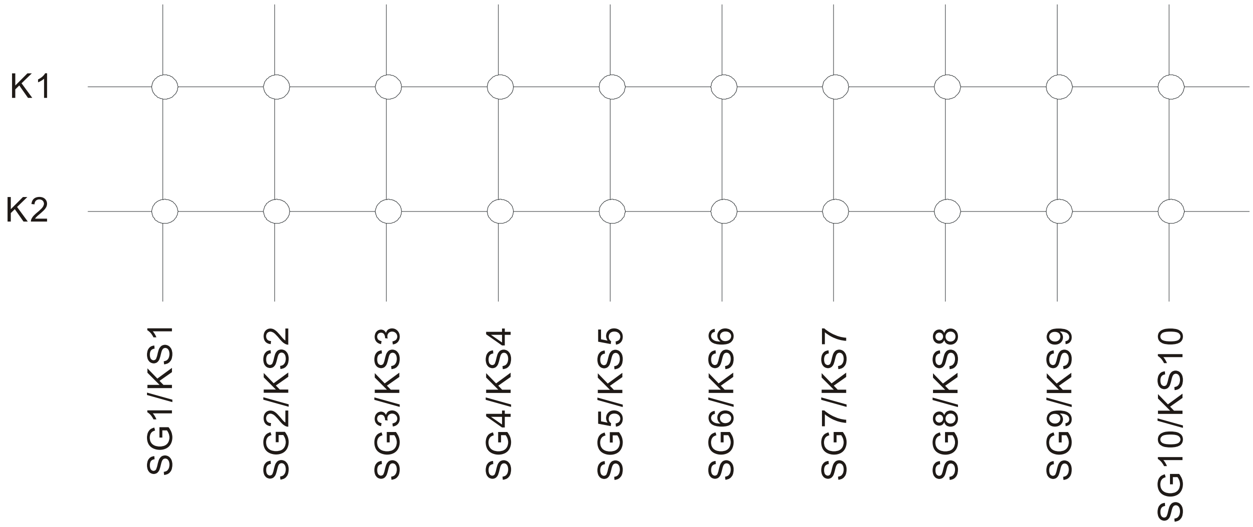
Data write & read mode settings:
00: Write data to display mode
10: Read key data

Address increment mode settings (Display mode):
0: Increment address after data has been written
1: Fixed address

Mode settings:
0: Normal operation mode
1: Test mode

PT6964 KEY MATRIX & KEY INPUT DATA STORAGE RAM

PT6964 Key Matrix consists of 10 x 2 array as shown below:


K1
K2
SG1/KS1
SG2/KS2
SG3/KS3
SG4/KS4
SG5/KS5
SG6/KS6
SG7/KS7
SG8/KS8
SG9/KS9
SG10/KS10

Each data entered by each key is stored as follows and read by a READ Command, starting from the last significant bit. When the most significant bit of the data (b0) has been read, the least significant bit of the next data (b7) is read.

K1…………………K2	K1…………………K2	
SG1/KS1	SG2/KS2	x
SG3/KS3	SG4/KS4	x
SG5/KS5	SG6/KS6	x
SG7/KS7	SG8/KS8	x
SG9/KS9	SG10/KS10	x
b0………………….b1	b3………………….b4	b6………………….b7

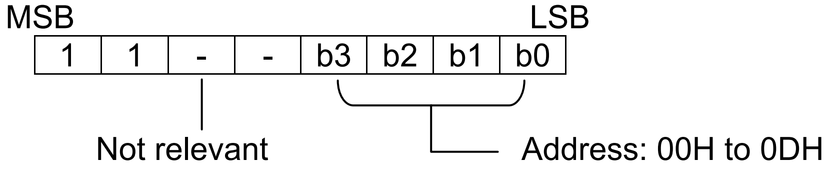
↓ Reading Sequence

Note: b6 and b7 do not care.

COMMANDS 3: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of 00H to 0DH. If the address is set to 0EH or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at 00H.

Please refer to the diagram below.



MSB							LSB
1	1	-	-	b3	b2	b1	b0

DISPLAY MODE AND RAM ADDRESS

Data transmitted from an external device to PT6964 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM addresses of PT6964 are given below in 8 bits unit.

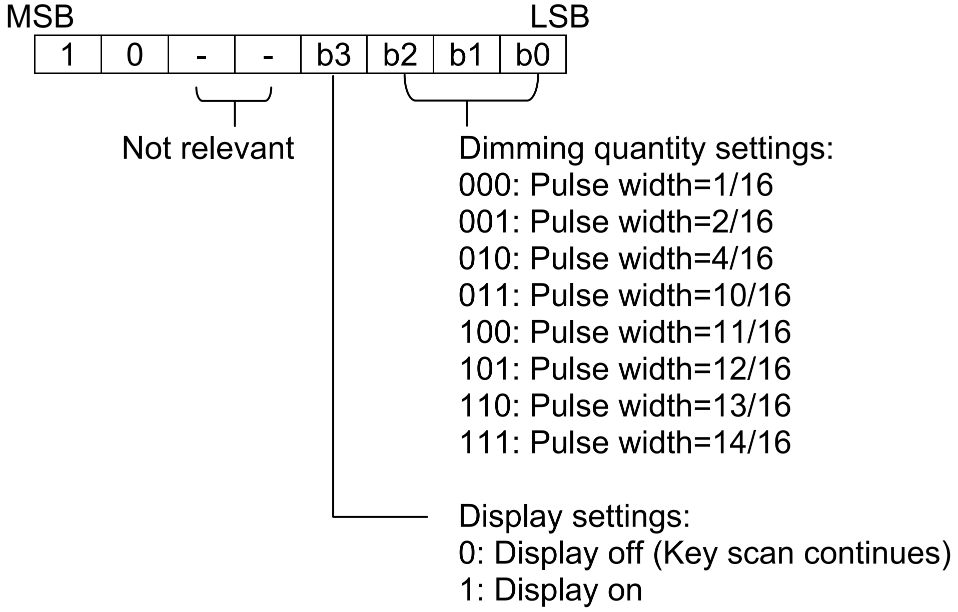
SG1 SG4	SG5 SG8	SG9 SG10	X	SG12	SG13 SG14	
00HL	00HU	01HL	-		01HU	DIG1
02HL	02HU	03HL	-		03HU	DIG2
04HL	04HU	05HL	-		05HU	DIG3
06HL	06HU	07HL	-		07HU	DIG4
08HL	08HU	09HL	-		09HU	DIG5
0AHL	0AHU	0BHL	-		0BHU	DIG6
0CHL	0CHU	0DHL	-		0DHU	DIG7

b0 b3	b4 b7
xxHL	xxHU
Lower 4 bits	Higher 4 bits

Note: X = Not relevant

COMMAND 4: DISPLAY CONTROL COMMANDS

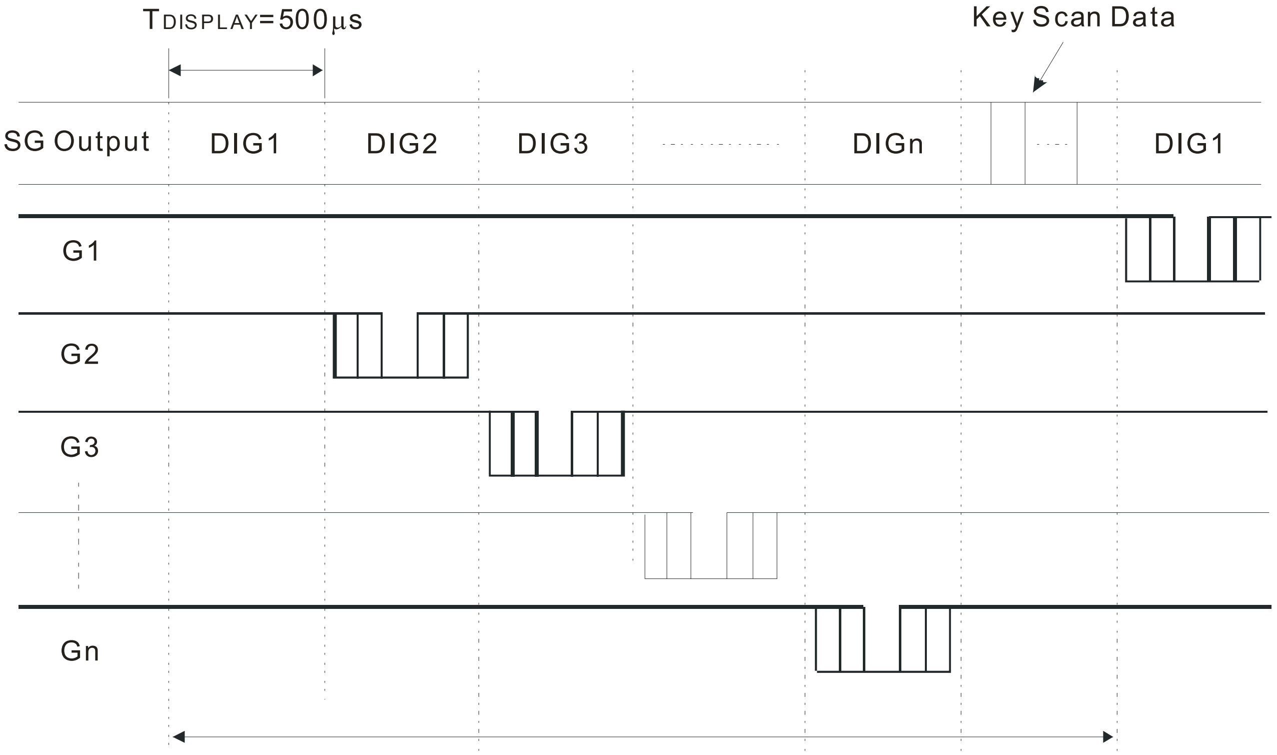
The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF (the key scanning is started).



Dimming quantity settings:
000: Pulse width=1/16
001: Pulse width=2/16
010: Pulse width=4/16
011: Pulse width=10/16
100: Pulse width=11/16
101: Pulse width=12/16
110: Pulse width=13/16
111: Pulse width=14/16

Display settings:
0: Display off (Key scan continues)
1: Display on

SCANNING AND DISPLAY TIMING

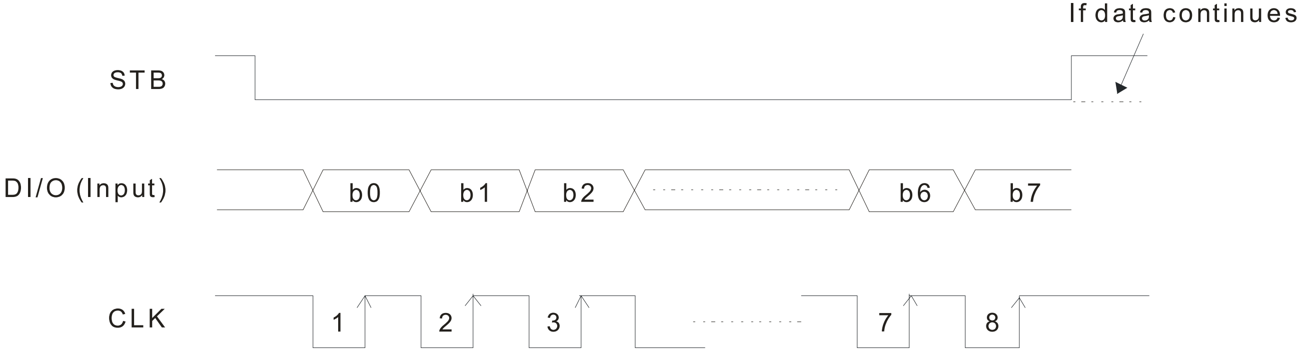

TDISPLAY=500μs
Key Scan Data
SG Output
DIG1
DIG2
DIG3
DIGn
DIG1
G1
G2
G3
Gn

1 Frame = TDISPLAY x (n +1)

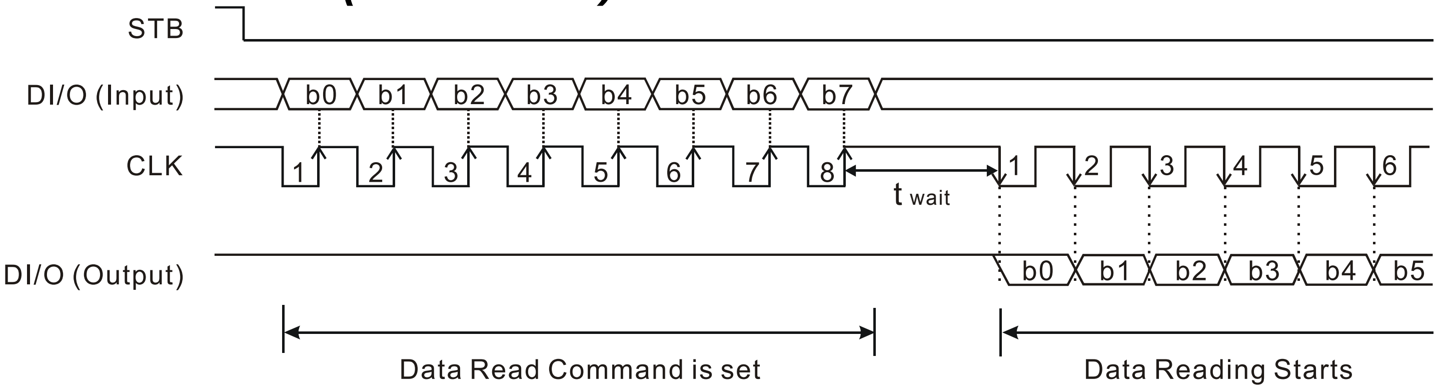
SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6964 serial communication format. The DI/O Pin is an N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor (1KΩ to 10KΩ) must be connected to DI/O.

RECEPTION (DATA/COMMAND WRITE)


If data continues
STB
DI/O (Input)
b0
b1
b2
b6
b7
CLK
1
2
3
7
8

TRANSMISSION (DATA READ)

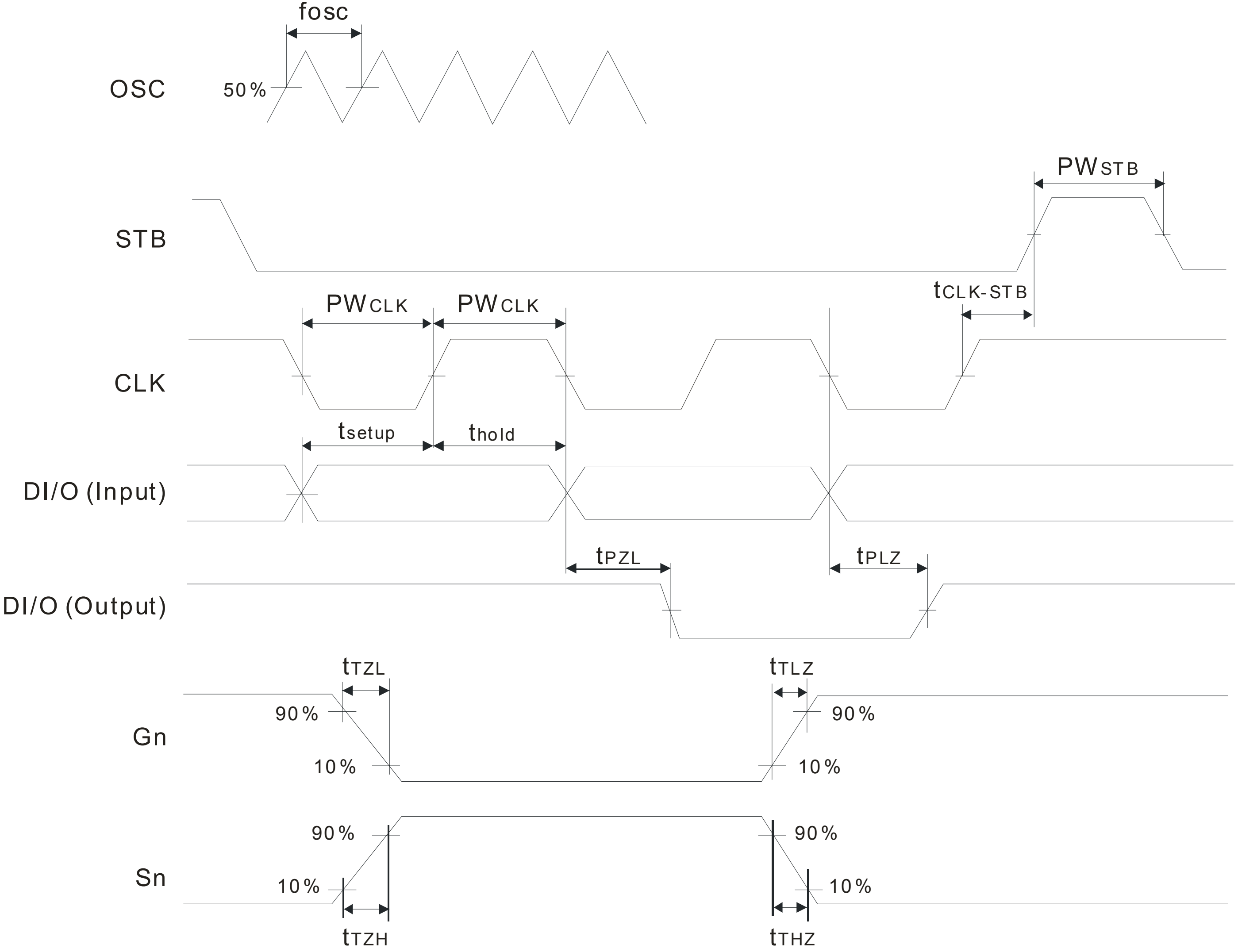

STB
DI/O (Input)
b0
b1
b2
b3
b4
b5
b6
b7
CLK
1
2
3
4
5
6
7
8
t wait
1
2
3
4
5
6
DI/O (Output)
b0
b1
b2
b3
b4
b5
Data Read Command is set
Data Reading Starts

where: twait (waiting time) ≥ 1μs

It must be noted that when the data is read, the waiting time (twait) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1μs.

SWITCHING CHARACTERISTIC WAVEFORM

PT6964 Switching Characteristics Waveform is given below.


fosc
OSC
50%
PWSTB
STB
tCLK-STB
PWCLK
PWCLK
CLK
tsetup
thold
DI/O (Input)
tPZL
tPLZ
DI/O (Output)
tTZL
tTLZ
90%
90%
Gn
10%
10%
90%
90%
Sn
10%
10%
tTZH
tTHZ

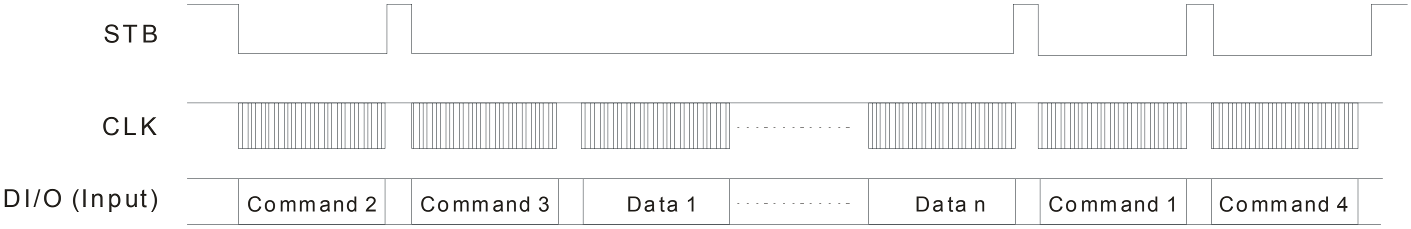
where:

PW_{CLK} (Clock Pulse Width) ≥ 400ns	PW_{STB} (Strobe Pulse Width) ≥ 1μs
t_{setup} (Data Setup Time) ≥ 100ns	t_{hold} (Data Hold Time) ≥ 100ns
$t_{CLK-STB}$ (Clock - Strobe Time) ≥ 1μs	t_{THZ} (Fall Time) ≤ 10μs
t_{TZH} (Rise Time) ≤ 1 μs	t_{PZL} (Propagation Delay Time) ≤ 100ns
fosc = Oscillation Frequency	t_{PLZ} (Propagation Delay Time) ≤ 300ns
t_{TZL} ≤ 1μs	t_{TLZ} ≤ 10 μs

Note:
Test Condition Under
t_{THZ} (Pull low resistor=10KΩ, Loading capacitor=300pF)
t_{TLZ} (Pull high resistor=10KΩ, Loading capacitor=300pF)

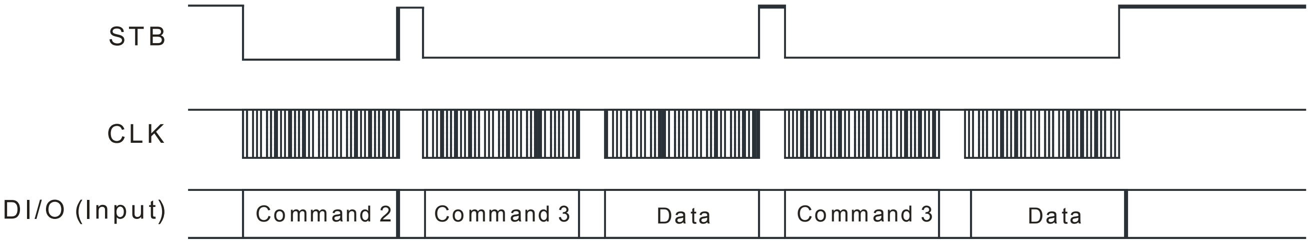
APPLICATIONS

Display memory is updated by incrementing addresses. Please refer to the following diagram.


STB
CLK
DI/O (Input)
Command 2
Command 3
Data 1
Data n
Command 1
Command 4

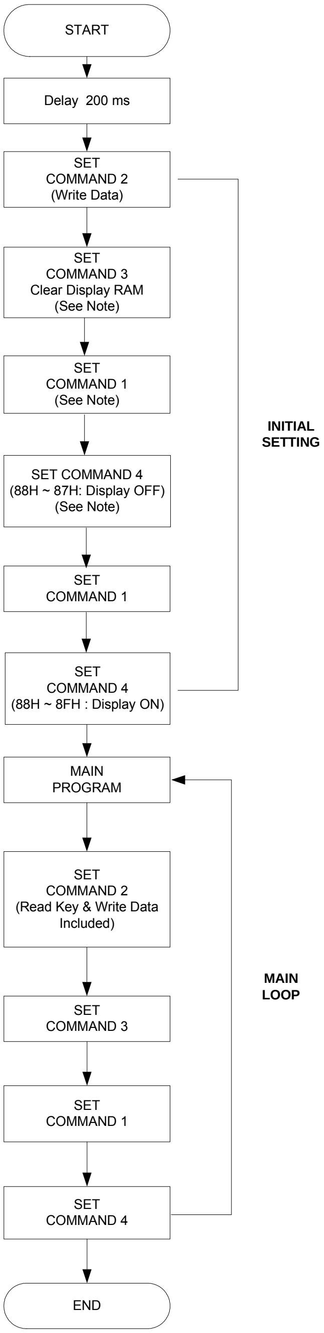
where:
Command 1: Display mode setting command
Command 2: Data setting command
Command 3: Address setting command
Data 1 to n: Transfer display data (14 bytes max.)
Command 4: Display control command

The following diagram shows the waveforms when updating specific addresses.


STB
CLK
DI/O (Input)
Command 2
Command 3
Data
Command 3
Data

where:
Command 2: Data setting command
Command 3: Address setting command
Data display data

RECOMMENDED SOFTWARE FLOWCHART

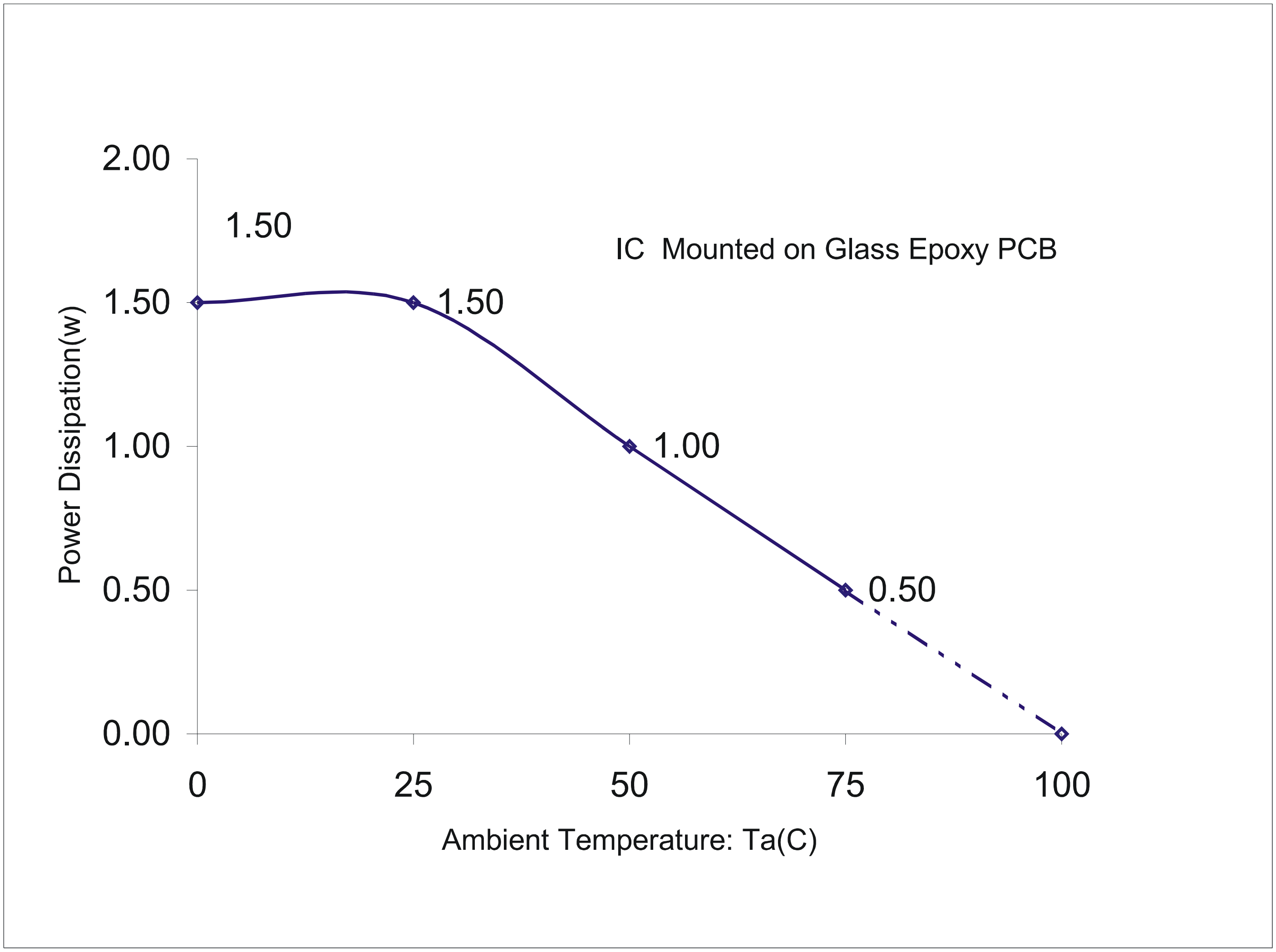

START
Delay 200 ms
SET
COMMAND 2
(Write Data)
SET
COMMAND 3
Clear Display RAM
(See Note)
SET
COMMAND 1
(See Note)
SET COMMAND 4
(88H ~ 87H: Display OFF)
(See Note)
SET
COMMAND 1
SET
COMMAND 4
(88H ~ 8FH : Display ON)
INITIAL
SETTING
MAIN
PROGRAM
SET
COMMAND 2
(Read Key & Write Data
Included)
SET
COMMAND 3
SET
COMMAND 1
SET
COMMAND 4
MAIN
LOOP
END

Notes:

1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM is not defined; thus, it is strongly suggested that the contents of the Display RAM be cleared during the initial setting.

SOP 28 (300MIL) THERMAL PERFORMANCE IN STILL AIR

JUNCTION TEMPERATURE: 100℃



ABSOLUTE MAXIMUM RATING

(Unless otherwise stated, Ta=25℃, GND=0V)

Parameter	Symbol	Rating	Unit
Supply voltage	VDD	-0.3 to +7	V
Logic input voltage	VI	-0.3 to VDD+0.3	V
Driver output current	IOLGR	+200	mA
	IOHSG	-50	mA
Maximum driver output current/total	ITOTAL	400	mA
Operating temperature	Topr	-40 ~ +85	℃
Storage temperature	Tstg	-65 ~ +150	℃

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta=25℃, GND=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD	4.5	5	5.5	V
Dynamic current (see Note)	IDDdyn	-	-	5	mA
High-level input voltage	VIH	0.8VDD	-	VDD	V
Low-level input voltage	VIL	0	-	0.3VDD	V

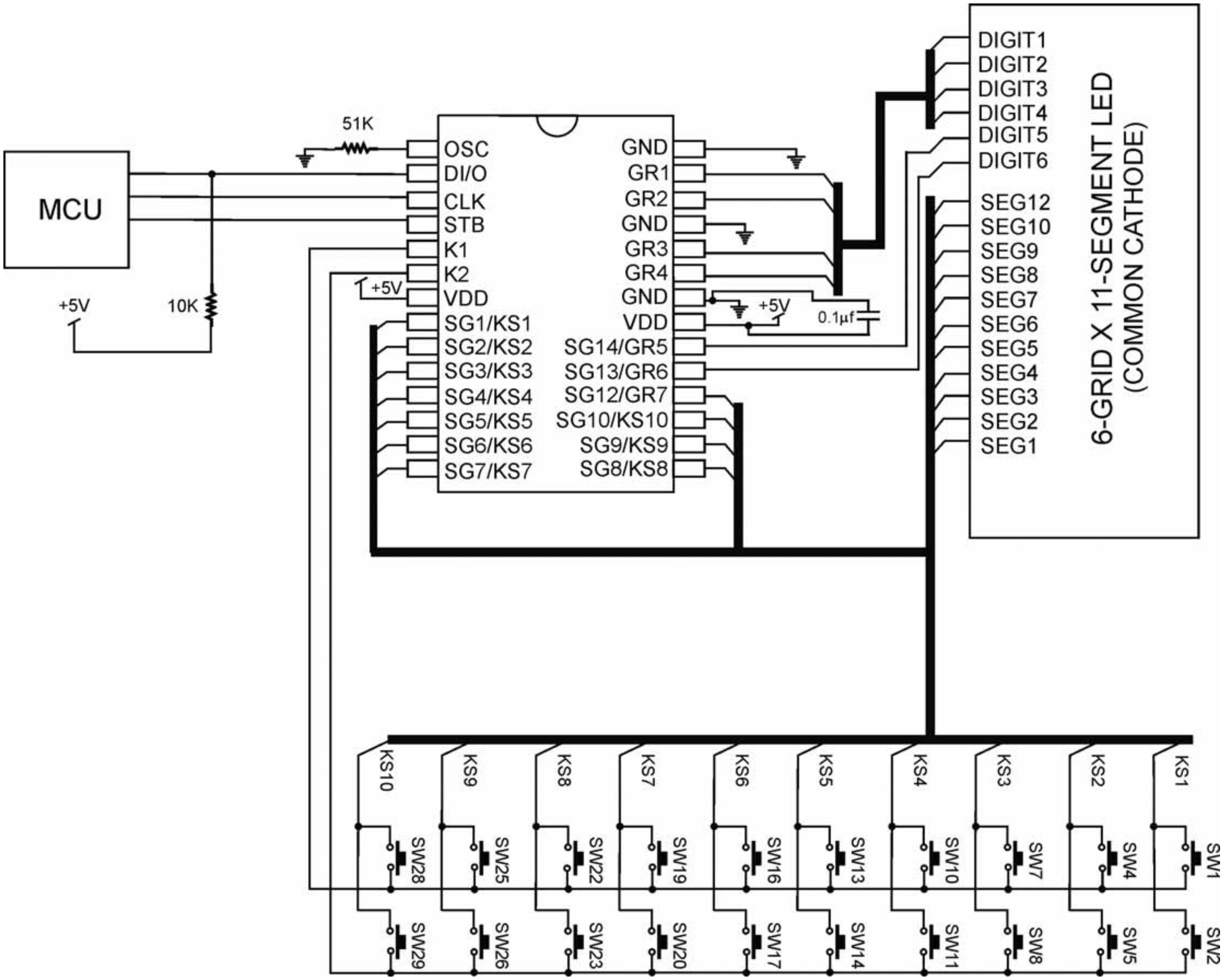
Note: Test Condition: Set Display Control Commands=80H (Display Turn OFF State & under no load)

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD=5V, GND=0V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-level output current	IOHSG(1)	VO=VDD-2V SG1/KS1 to SG10/KS10, SG12/GR7 to SG14/GR5	-20	-25	-40	mA
	IOHSG(2)	VO=VDD-3V SG1/KS1 to SG10/KS10, SG12/GR7 to SG14/GR5	-25	-30	-50	mA
Low-level output current	IOLGR	VO=0.3V GR1 to GR4 SG14/GR5 to SG12/GR7	100	140	-	mA
Low-level output current	IOLDI/O	VO=0.4V	4	-	-	mA
Segment high-level output current tolerance	ITOLSG	VO=VDD-3V SG1/KS1 to SG10/KS10, SG12/GR7 to SG14/GR5	-	-	±5	%
High-level input voltage	VIH	-	0.8VDD	-	5	V
Low-level input voltage	VIL	-	0	-	0.3VDD	V
Oscillation frequency	fosc	R=51KΩ	350	500	650	KHz
K1 to K3 pull down resistor	RKN	K1 to K2 VDD=5V	40	-	100	KΩ

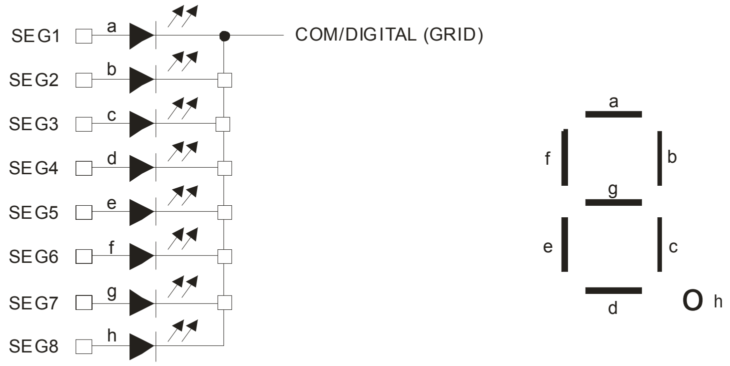
APPLICATION CIRCUIT


MCU
51K
10K
+5V
OSC
DI/O
CLK
STB
K1
K2
VDD
SG1/KS1
SG2/KS2
SG3/KS3
SG4/KS4
SG5/KS5
SG6/KS6
SG7/KS7
GND
GR1
GR2
GND
GR3
GR4
GND
VDD
SG14/GR5
SG13/GR6
SG12/GR7
SG10/KS10
SG9/KS9
SG8/KS8
+5V
0.1µf
DIGIT1
DIGIT2
DIGIT3
DIGIT4
DIGIT5
DIGIT6
SEG12
SEG10
SEG9
SEG8
SEG7
SEG6
SEG5
SEG4
SEG3
SEG2
SEG1
6-GRID X 11-SEGMENT LED
(COMMON CATHODE)
KS10
KS9
KS8
KS7
KS6
KS5
KS4
KS3
KS2
KS1
SW28
SW25
SW22
SW19
SW16
SW13
SW10
SW7
SW4
SW1
SW29
SW26
SW23
SW20
SW17
SW14
SW11
SW8
SW5
SW2

Notes:

1. The capacitor (0.1μF) connected between the GND and the VDD pins must be located as close as possible to the PT6964 chip.
2. The PT6964 power supply is separate from the application system power supply.

COMMON CATHODE TYPE LED PANEL

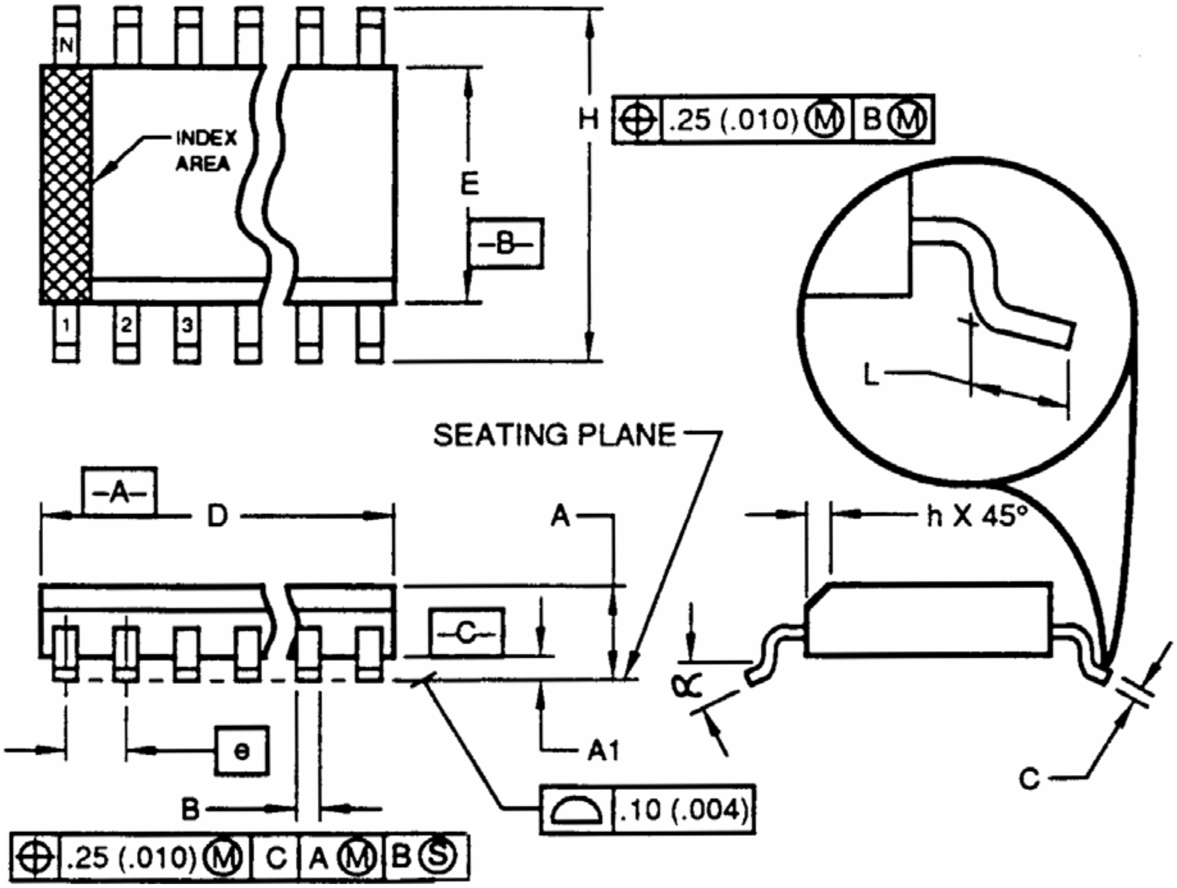

SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG7
SEG8
a
b
c
d
e
f
g
h
COM/DIGITAL (GRID)
a
f
b
g
e
c
d
h

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6964-S	28 Pins, SOP, 300mil	PT6964-S

PACKAGE INFORMATION

28 PINS, SOP, 300MIL


N
INDEX AREA
1
2
3
E
-B-
H
.25 (.010) M B M
L
SEATING PLANE
-A-
D
A
-C-
A1
h X 45°
α
C
e
B
.10 (.004)
.25 (.010) M C A M B S

Symbol	Min.	Nom.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	17.70		18.10
E	7.40		7.60
e	1.27 BSC.		
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
α	0°		8°

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5-1982.
2. Dimension “D” does not include mold flash , protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15mm (0.006 in) per side.
3. Dimension “E” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. “L” is the length of the terminal for soldering to a substrate.
6. “N” is the number of terminal positions. (N=28)
7. The lead width “B” as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in).
8. Controlling dimension: MILLIMETER.
9. Refer to JEDEC MS-013 Variation AE

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