MxL608

Low Cost Digital Cable and Terrestrial Silicon Tuner Product Brief

Introduction

The MxL608 is a high performance, low power digital terrestrial and cable television silicon tuner that is targeted at price-sensitive Set-Top Boxes (STBs).

Based on MaxLinear's market-proven 65nm digital CMOS technology, the MxL608 is software configurable for all global terrestrial and cable reception standards without the need for any hardware modifications. Supported standards include:

- DVB-T/T2
- ISDB-T
- ATSC
- DTMB
- DVB-C
- J.83 Annex A/B/C

The MxL608 converts a single-ended 75Ω RF input signal to an IF output frequency that is software programmable between 4MHz and 44MHz. All channel selection filters are fully integrated and software configurable for 6MHz, 7MHz, or 8MHz channel bandwidths.

The MxL608 includes an accurate input power detector and channel scan algorithm that offers significant improvement in channel scan time, especially under blind-scan conditions. Channel filtering, Low Noise Amplifier (LNA), and loop-through output are completely integrated. The external Bill Of Materials (BOM) is limited to a small number of standard value discrete components.

The MxL608 has a typical power consumption of ~350mW in Digital Terrestrial mode. In Low Power Standby mode, the MxL608 consumes just 110mW, while still able to pass through the RF signal to an analog TV through the loop-through output.

The MxL608 uses an API-based software architecture, which reduces the programming effort and eliminates the need for complicated register calls. The MxL608 is pin-compatible with the market-leading MxL603 tuner, which enables current customers to leverage their existing designs and achieve faster time-to-market with minimal engineering investment.

A complete Reference Design Kit (RDK) is available for cable and terrestrial applications, including a reference PCB schematic and layout files, detailed BOM, hardware design guide, software programming guide, source code, and standard-specific performance test reports. The RDK supports a dual layout configuration, with or without an external balun, to enable manufacturers to trade-off cost vs sensitivity performance using the same hardware design.

Applications

- Digital terrestrial and cable STBs
- Integrated Digital Televisions (iDTVs)
- Tuner modules
- Portable TVs and media players
- Blu-Ray recorders
- Multi-tuner Personal Video Recorder (PVRs)

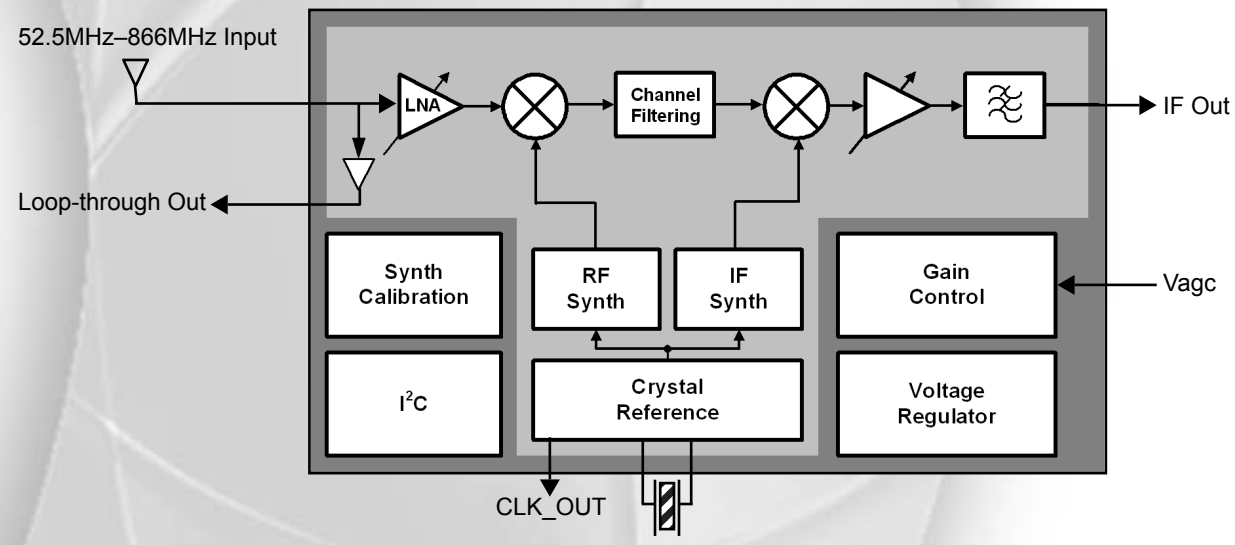
Features

- Pin-compatible with the MxL603
- Optional no balun (single-ended input) configuration
- 52.5MHz to 866MHz tuning range
- Programmable channel selection filter (6MHz/ 7MHz/8MHz)
- Programmable low/high IF interface
- Programmable IF Automatic Gain Control (AGC) interface
- Self AGC calibration
- Programmable IF spectrum inversion
- Highly accurate input power level reporting
- Reference clock output
- I^2C-compatible control interface
- Integrated loop-through output
- API-based software interface
- 4x4mm^2 QFN24 package

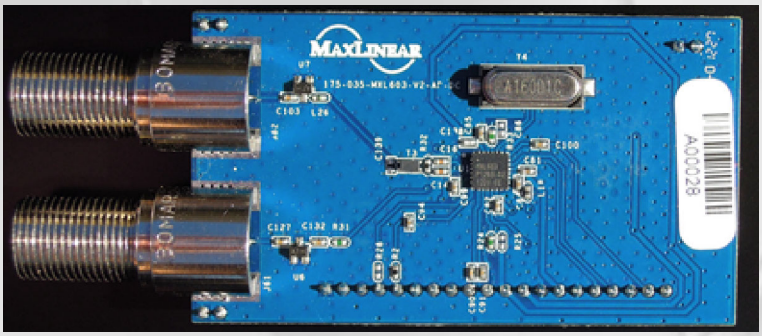
Benefits

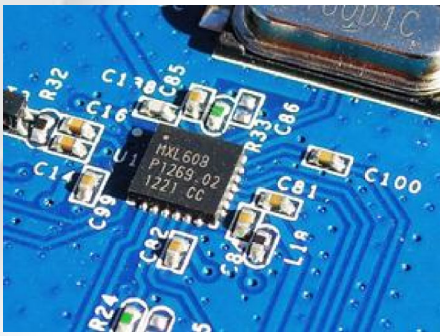
- Single hardware design for all global digital terrestrial applications
- Ultra low power, 350mW (Active), or 110mW (Standby)
- Simple two-layer PCB design
- No external Surface Acoustic Wave (SAW) filters
- Low BOM cost

MxL608 Block Diagram



Reference Design PCB





Ordering Information

Part Number	Description	Package
MxL608-AG-T	Global Digital Cable and Terrestrial STB Tuner	QFN24
MxL9608K01	MxL608 Evaluation Kit (EVK) for STB Applications	-

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Revision History

Document/Revision No.	Release Date	Change Description
001_608-02DSR	10/11/12	**Updated:** ■ Title and minor text changes. ■ Input tuning range. ■ "Tuner General Specifications."
001_608-01DSR	09/28/12	**Updated:** ■ "MxL608 IC Block Diagram" figure. ■ "Digital Supported IF Frequencies" table.
001_608-00DSR	09/19/12	Initial release.

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Introduction

The MxL608 is a highly integrated, low power silicon tuner IC that targets low cost terrestrial set-top box applications. The MxL608 is compliant with DVB-T and DTMB specifications for RF performance. The MxL608 is a subset of the MxL603 tuner, which is fully compliant with all global terrestrial standards. The following table lists the complete description of the standards compliance.

Table 1: Standards Compliance Matrix

Broadcast Standard	MxL603	MxL608
DVB-T2, ISDB-T	•	-
DVB-T, DTMB	•	•
ATSC	•	-
J.83 annex A, C (DVB-C)	•	-
J.83 annex B	•	-

The MxL608 supports an input tuning range from 52.5MHz to 866MHz. A signal at the 75Ω RF input is filtered and converted to a programmable IF output up to 44MHz. The AGC, LO generation, channel selection, and LT output functions are completely integrated on the chip, which simplifies board-level design. All functions of the IC can be controlled via an I^2C interface. Driver integration is made easy through the use of simple software APIs.

The high level of integration enables a very compact, cost-effective design with few external components, low BOM costs and low power consumption.

The MxL608 is available in a 4mm x $4mm^2$ 24-pin QFN package.

Glossary

Table 2: Glossary

Acronym/Abbreviation	Description
°	Degree
µ	Micro
µW	MicroWatt
kΩ	kiloOhm
Ω	Ohm
AC	Alternating Current
AGC	Automatic Gain Control
API	Application Programming Interface
AS	Address Selection
ATSC	Advanced Television Systems Committee
BE	Back-End
BOM	Bill Of Materials
BW	Band Width

Table 2: Glossary (Continued)

Acronym/Abbreviation	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
dB	deciBel
dBc	deciBels relative to the carrier
DTMB	Digital Terrestrial Multimedia Broadcast
DVB-C	Digital Video Broadcasting—Cable
DVB-T	DVB—Terrestrial
DVB-T2	DVB—Terrestrial Second Generation
EMI	Electro-Magnetic Interference
ESD	Electro-Static Discharge
FBE	Filter Band Edge
FEC	Forward Error Correction
GD	Group Delay
GHz	GigaHertz
GND	Ground
GPIO	General Purpose Input/Output
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
IF	Intermediate Frequency
I/O	Input/Output
I/Q	In-phase and Quadrature
ITU-T	International Telecommunication Union—Telecommunications
kHz	kiloHertz
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
LT	Loop Through
LTE	Long Term Evolution
mA	milliAmp
MHz	MegaHertz
mm	millimeter
MoCA	Multimedia over Coax Alliance
MSB	Most Significant Bit
mW	milliWatt
NF	Noise Figure
NTSC	National Television System Committee
PAL	Phase Alternating Line
pF	picoFarad
PLL	Phase Locked Loop

Table 2: Glossary (Continued)

Acronym/Abbreviation	Description
ppm	parts per million
PVR	Personal Video Recorder
QAM	Quadrature Amplitude Modulation
QEF	Quasi Error Free
QFN	Quad Flat No-leads
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RSSI	Received Signal Strength Indication
SAW	Surface Acoustic Wave
SoC	System on a Chip
TS	Transport Stream
V	Volt
W	Watt
WiFi	Wireless Fidelity
Xtal	Crystal oscillator

IC Block Diagram

Figure 1 illustrates the architecture of the MxL608 tuner. The chip utilizes a proprietary architecture, which achieves the required channel selection using a multistage channel filter. The RF input is mixed to a fixed frequency, followed by channel filtering, and then mixed to a programmable IF frequency. Anti-alias filtering after the second mixing stage removes any out-of-band harmonics. A tunable IF LO allows for programmable IF frequencies. The AGC is distributed throughout the signal path for optimum noise and linearity performance through one AGC line.

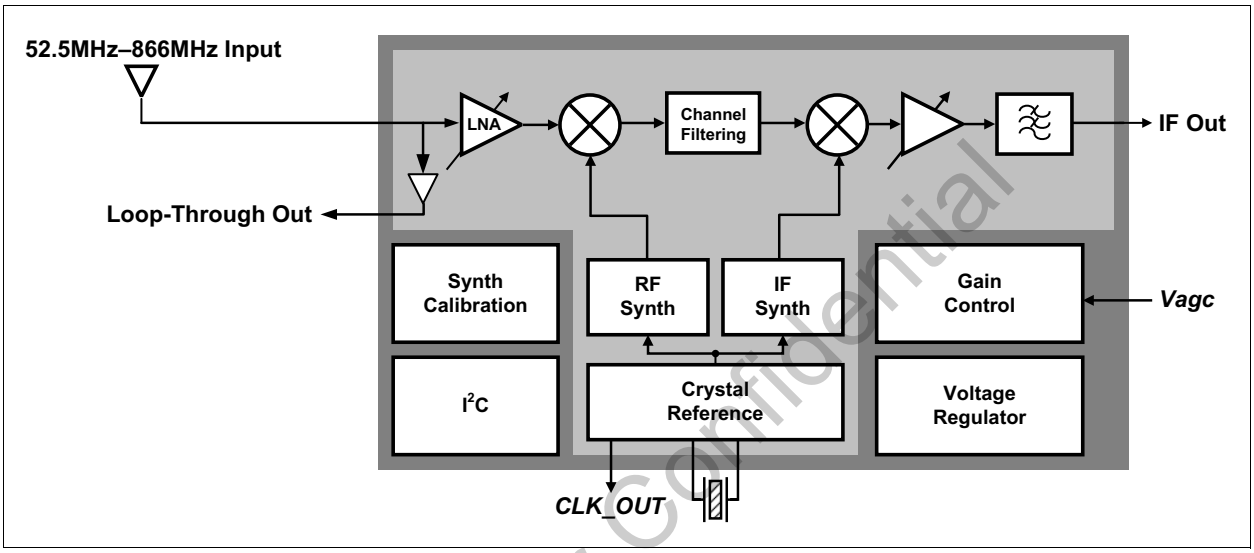

Figure 1: MxL608 IC Block Diagram

Pin Information

Pin Configuration

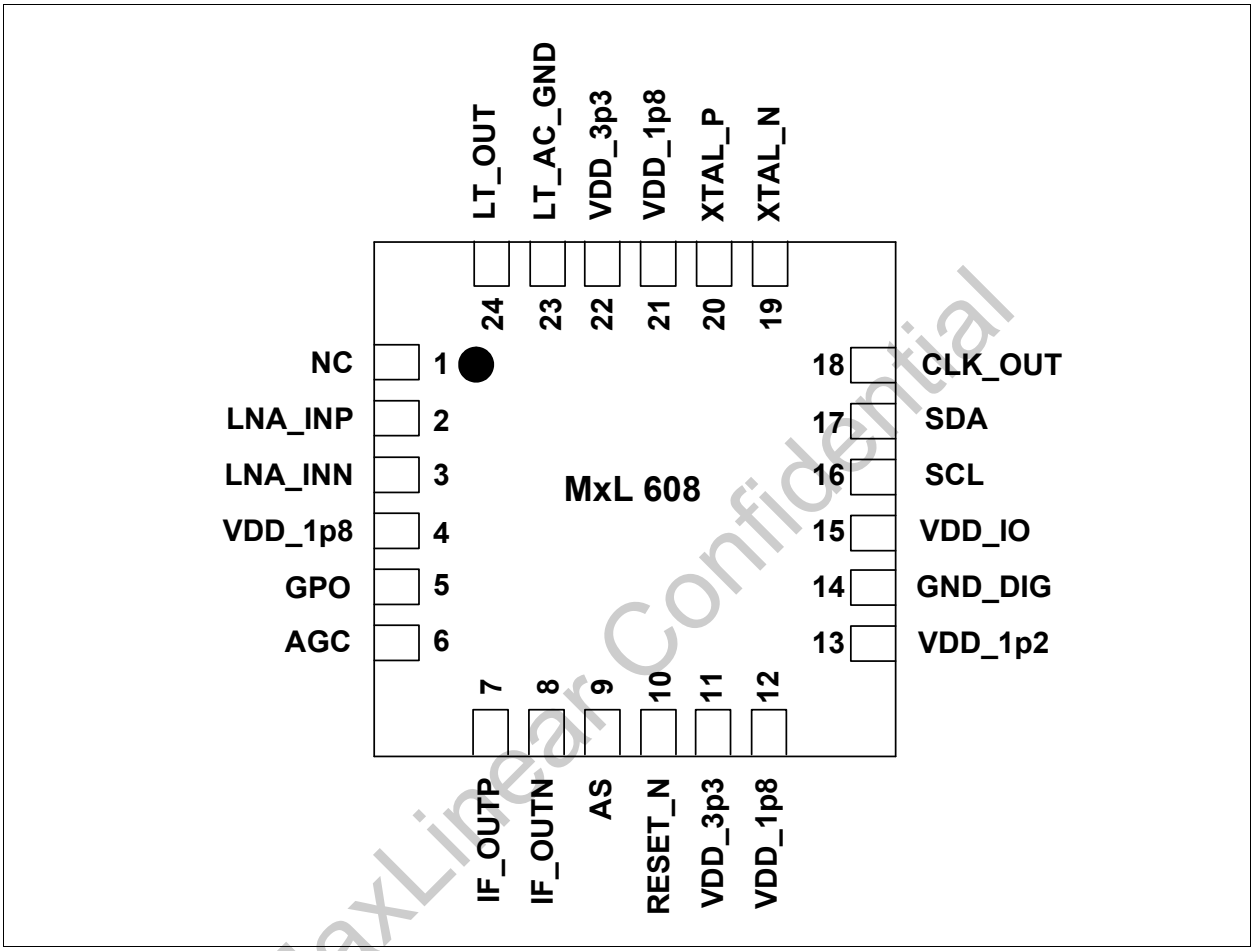

Figure 2: Pin Configuration

Pin Description

Table 3: Pin Names

Pin #	Pin Name	Pin #	Pin Name
1	NC	13	VDD_1p2
2	LNA_INP	14	GND_DIG
3	LNA_INN	15	VDD_IO
4	VDD_1p8	16	SCL
5	GPO	17	SDA
6	AGC	18	CLK_OUT
7	IF_OUTP	19	XTAL_N
8	IF_OUTN	20	XTAL_P
9	AS	21	VDD_1p8
10	RESET_N	22	VDD_3p3
11	VDD_3p3	23	LT_AC_GND
12	VDD_1p8	24	LT_OUT

RF Interface

Table 4: RF Interface

Pin Name	Direction	Description
LNA_INP LNA_INN	Input	Differential RF inputs; differential input impedance of 75Ω.
LT_OUT	Output	Single-ended, loop through output.
LT_AC_GND	Output	AC ground for LT.

I^2C Interface

Table 5: I^2C Interface

Pin Name	Direction	Description
SCL	Input	Clock.
SDA	Bidirectional	Pull-down data pin.
AS	Input	Address selection (see "AS Pin Hardware Configuration and Resistor Tolerance Requirement" on page 16 for details).

Supply and Ground

Table 6: Supply and Ground

Pin Name	Direction	Description
VDD_3p3	Input	Supply voltage for 3.3V.
VDD_1p8	Input	Supply voltage for 1.8V.
VDD_IO	Input	Supply voltage for I/O interface.
GND	Input	Connect to ground.
GND_DIG	Input	Ground for digital circuit blocks.

Analog and Digital I/O

Table 7: Analog and Digital I/O

Pin Name	Direction	Description
CLK_OUT	Output	Clock output is programmable to div-by-1 or div-by-6 of the crystal for clock re-use.
RESET_N	Input	Reset.
IF_OUTP IF_OUTN	Output	IF output.
GPO	Output	General purpose output (see "GPO Control" on page 17 for details).
AGC	Input	Automatic gain control.
XTAL_P	Input	Crystal positive input.
XTAL_N	Input	Crystal negative input; can be used as an external system clock input pin if no crystal is used.

Electrical Specifications

Absolute Maximum Ratings

Important! The stresses above what is listed under the following table may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under the following table or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above the recommended extended periods of time may affect device reliability.

Table 8: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
VDD_3p3	–0.3	3.6	V
VDD_1p8	–0.3	2.0	V
VDD_IO	–0.3	3.6	V
AGC	–0.3	3.6	V
SDA, SCL	–0.3	3.6	V
AS	–0.3	3.6	V
GPO	–0.3	3.6	V
RF Input Power	-	15	dBm
Storage Temperature	–65	150	°C
Soldering Temperature	-	265	°C

Operating Conditions

Table 9: Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
3.3V Supply	VDD_3p3	3.1	3.3	3.6	V
1.8V Supply	VDD_1p8	1.7	1.8	1.9	V
I/O Supply (1.8V Mode)	VDD_IO	1.7	1.8	1.9	V
I/O Supply (3.3V Mode)	VDD_IO	3.1	3.3	3.6	V
AGC Range (see "AGC Voltage Range" on page 17)	AGC	0	-	3.3	V
AS	AS	0	-	3.6	V
Reset Voltage Supply	RESET_N	0	-	VDD_IO	V
Operating Temperature	T	0	25	85	°C
Junction Temperature	Tj	-	-	125	°C

Digital I/O Specifications

Table 10: Digital I/O Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Units
3.3V Configuration (VDD_IO = 3.3V)					
Output Logic Voltage on All Digital I/O Pins	V_{OH} (@ 3mA source)	VDD_IO –0.4	-	-	V
	V_{OL} (@ 3mA sink)	-	-	0.4	V
Input Logic Voltage on All Digital I/O Pins	V_{IH}	2.2	-	-	V
	V_{IL}	-	-	0.8	V
1.8V Configuration (VDD_IO = 1.8V)					
Output Logic Voltage on All Digital I/O Pins	V_{OH} (@ 3mA source)	VDD_IO –0.2	-	-	V
	V_{OL} (@ 3mA sink)	-	-	0.2	V
Input Logic Voltage on All Digital I/O Pins	V_{IH}	1.1	-	-	V
	V_{IL}	-	-	0.4	V

Tuner General Specifications

All specifications apply to the conditions defined in "Operating Conditions" on page 8, measured at IF = 7/8MHz and across the RF frequency range.

Table 11: Tuner General Specifications

Parameter		Symbol	Minimum	Typical	Maximum	Units
System						
Input Return Loss 75Ω System		S_{11}	-	–8	-	dB
RF Frequency Range		f_{RF}	44	-	866	MHz
Channel Bandwidth		-	-	7, 8	-	MHz
Maximum Voltage Gain (LT Off)		G_{max}	90	94	-	dB
Gain Control Range (LT Off)		AGC	110	114	-	dB
Noise Figure (LT Off)		NF	-	4.2	-	dB
Output 1dB Compression		-	112	115	-	dBuVrms
IF LO Feed-through Rejection	RF input > –70dBm	DCOS	-	-	–45	dBc
I/Q Imbalance	RF input > –70dBm	IQI	-	-	–45	dBc
Supply Ripple Susceptibility (1kHz–500kHz, see "Supply Ripple Susceptibility" on page 17)		-	-	-	20	mVpp
RF Input Leakage		-	-	–90	-	dBm
LT Output						
RF Frequency Range		f_{LT}	52.5	-	866	MHz
Gain		G_{LT}	–2	1	3	dB
Noise Figure (LT only)		NF_{LT}	-	9	-	dB
LT Output Return Loss		$S22_{LT}$	-	–10	-	dB

Table 11: Tuner General Specifications (Continued)

Parameter			Symbol	Minimum	Typical	Maximum	Units
Channel Select Filter for Digital Terrestrial							
Channel Select FBE Frequency Definition (measured at the offset from the center of the band; see "FBE and In-Band Ripple Definition" on page 18)		BW=7MHz	FBE	-	3.25	-	MHz
		BW=8MHz	FBE	-	3.75	-	MHz
GD Across ± Band Edge (Peak-to-Peak)		BW=7MHz	GD	-	-	50	ns
		BW=8MHz	GD	-	-	50	ns
In-Band Amplitude Variation		BW=7MHz	-	-	2	-	dB
		BW=8MHz	-	-	2	-	dB
Attenuation of Adjacent Analog Channel (measured at the offset from the center of the band)	BW= 7MHz	Picture (4.75MHz)	-	-	85	-	dB
		Sound (3.75MHz)	-	-	60	-	dB
	BW= 8MHz	Picture (5.25MHz)	-	-	85	-	dB
		Sound (4.75MHz)	-	-	85	-	dB
Synthesizer							
Phase Noise	at 250Hz Offset	-	-	–77	–82	-	dBc/Hz
	at 1kHz Offset	-	-	–77	–82	-	dBc/Hz
	at 10kHz Offset	-	-	-	–87	-	dBc/Hz
	at 100kHz Offset	-	-	-	–99	-	dBc/Hz
Crystal Oscillator							
Negative Resistance (see "Negative Resistance" on page 16)			-	-	350	-	Ω
Input Level to the XTAL_N Pin when using an External Clock			-	-	600	-	mVpp
Others							
IF Output Impedance (Single-ended)	High IF (>=36MHz)		-	-	153	-	Ω
	Low IF		-	-	305	-	Ω
IF Output Level (Programmable)	Low IF		-	400	800	1250	mVp-p
AGC Input Impedance			-	-	55K	-	Ω
Clock Output Swing			-	-	600	-	mVpp

Current Consumption

The current consumption accounts for temperature and process variations. The typical condition applies to typical conditions defined in the recommended "Operating Conditions" on page 8.

Note: When LT is on, add an additional 20mA current consumption on the VDD_3p3 supply pin to the values in the following table.

Table 12: Current Consumption

Mode	Operating Frequency	Supply Pin	Minimum	Typical	Maximum	Units
Digital Terrestrial	RF=52.5MHz–866MHz	VDD_3p3		54	65	mA
		VDD_1p8		125	150	mA

Crystal Requirements

The MxL608 only supports the fundamental mode crystals. The default crystal frequency used is 16MHz.

Table 13: Crystal Requirements

Parameter	Minimum	Typical	Maximum	Units
ESR	-	25	50	Ω
Frequency Accuracy (including Temperature and Tolerance)	–60	-	+60	ppm
Aging	-	±3	-	ppm/year
Load Capacitance	-	18	-	pF
Drive Level	-	250	-	µW

Supported Crystal Frequencies

Table 14: Supported Crystal Frequencies

Crystal Frequencies	Units	Comment
16	MHz	Default.
24	MHz	Optional.

Supported IF Frequencies

The MxL608 also supports other IF frequencies not listed in the following table—contact MaxLinear's Sales and Application for other support.

Table 15: Digital Supported IF Frequencies

Item	Low IF (MHz)	Standard IF (MHz)	Bandwidth (MHz)	Comment
DVB-T	5	36.15, 44.0	7.8	Programmable channel BW.
DTMB	-	36.15	8	-

Supply Voltage Ramp-Up Rules

The MxL608 chip is designed to support an arbitrary power-up sequence for the three power supplies, as illustrated in the following figure. The three supplies can be powered up in an arbitrary order. The only requirement is to keep RESET_N low during the power-up. The RESET_N signal can be released after all voltage supplies have been stable for at least 10µs ($T_1 \geq 10\mu s$).

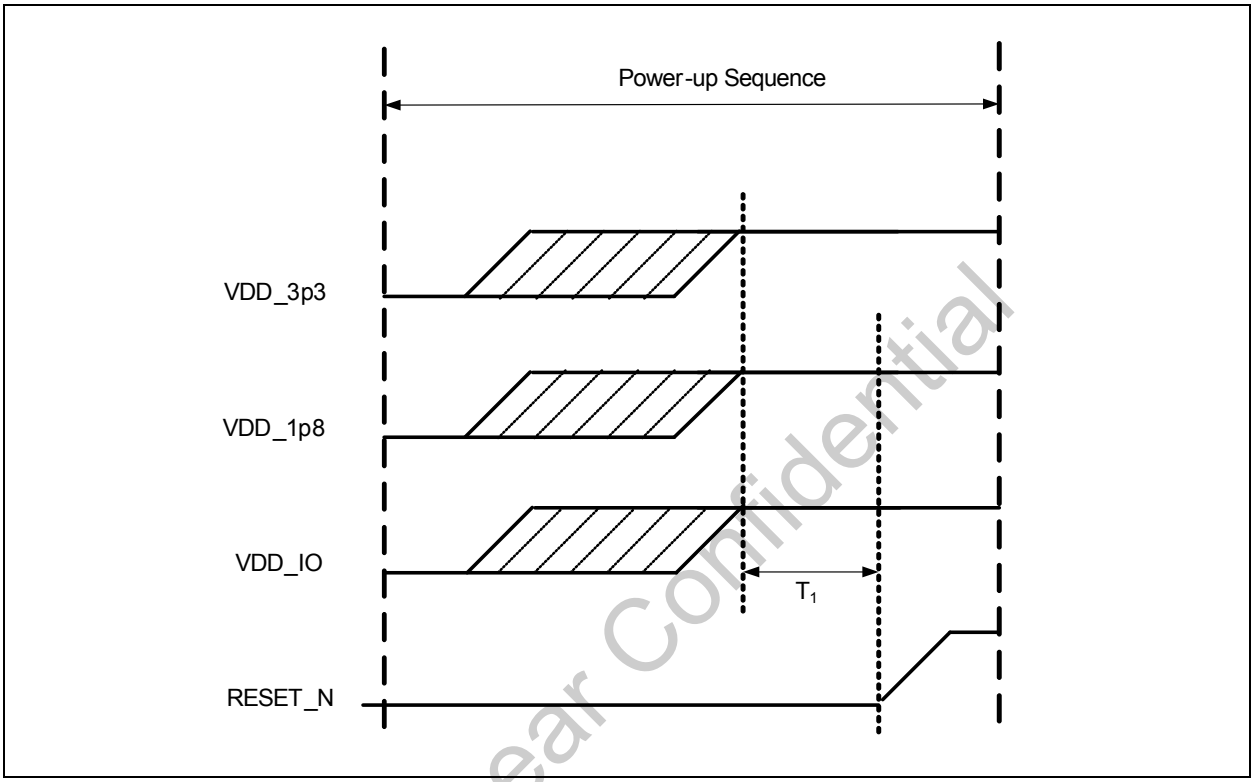

Figure 3: Supply Voltage Ramp-Up Rule

Reset Timing Rules

If the IC needs to reset while the chip is in a fully operational mode, the minimum timing (tRST) for the low state is 10µs.

Table 16: Reset Timing Rules

Parameter	Symbol	Minimum	Typical	Maximum	Units
Reset Timing	tRST	10	-	-	µs

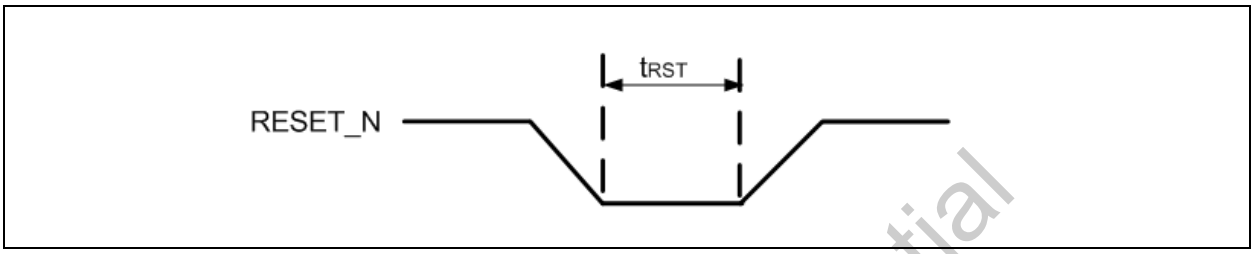

Figure 4: Reset Timing Rule

Operating Modes

For more details, see "Operating Modes Control" on page 17.

Note: The LT can be on or off for all operation modes. When LT is on, add an additional 67mW power consumption to the values in the following table.

Table 17: Operating Modes

Mode	Control	Typical Power	Description
Sleep	Upon reset	26mW	■ On-chip digital regulator is on. ■ Xtal and clock-out are on. ■ I^2C is active. ■ Register value is at default. ■ RF section is inactive. ■ LT is not enabled.
Standby	I^2C control	26mW	■ On-chip digital regulator is on. ■ Xtal oscillator and clock-out are on. ■ I^2C is active. ■ Register value is the same as the previous state. ■ RF section is inactive. ■ LT is not enabled.
Active	I^2C control	403mW	■ Tuner is fully operational in the digital terrestrial mode. ■ LT is not enabled.

ESD Performance

All pins pass the ESD performance of 2000V using the HBM and of 250V using the CDM.

Packaging

- **QFN24 package dimensions** = 4mm x 4mm x 0.85mm^3.
- **Thermal resistance (junction to ambient)** = 43^{o}C/W.

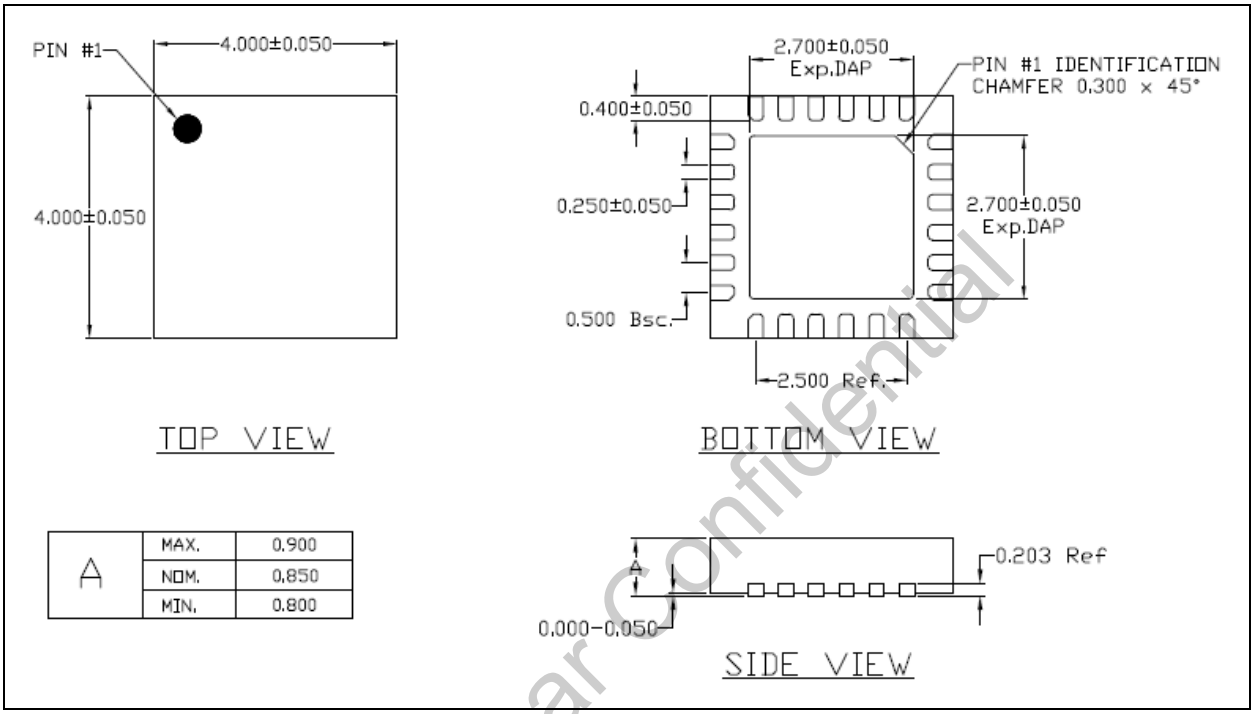

Figure 5: Packaging

Thermal Via Design

To take full advantage of the QFN thermal performance, thermal vias are needed to provide a thermal path from the top to the inner/bottom layers of the PCB board for heat transfer.

Important! MaxLinear recommends following the thermal via design described in Figure 5.

Thermal Information

$T_{Junction} = T_{Ambient} + ThetaJa \times Power\ Dissipation$

Table 18: Thermal Information

Parameter	Value/Condition	Unit
Thermal Resistance (Junction to Ambient)	43	$^{o}C/W$
PCB Condition (Thermal Resistance Calculation)	JEDEC JESD 51-5	-
Air Flow Condition	0	ms
Number of Vias	4 to 9	-
Via Pitch	1–1.2	mm
Via Size (Diameter)	0.25–0.33	mm

Ordering Information

Table 19: Ordering Information

Marketing Part Number	Ordering Part Number	Package	Dimension	Shipping
MxL608	MxL608-AG-T	SAWN QFN24	4mm x 4mm x 0.85mm^3	Tray
MxL608	MxL608-AG-R	SAWN QFN24	4mm x 4mm x 0.85mm^3	Tape and Reel

Appendix

AS Pin Hardware Configuration and Resistor Tolerance Requirement

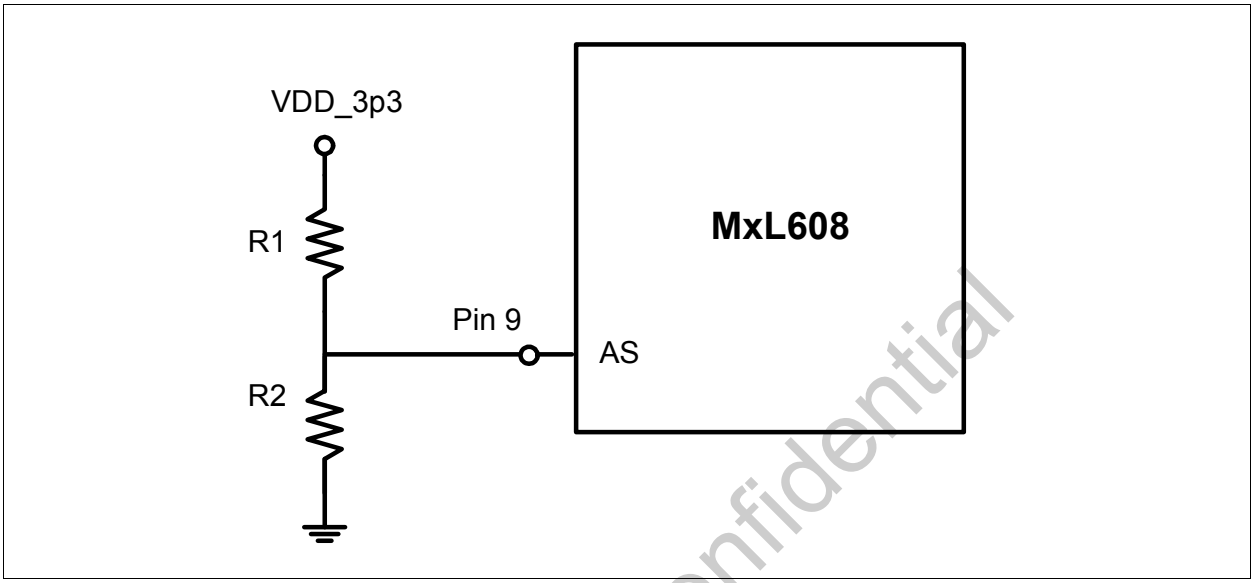

Figure 6: AS Pin Hardware Configuration and Resistor Tolerance Requirement

Table 20: AS Pin Hardware Configuration and Resistor Tolerance Requirement

I^2C Address	R1	R2
96	Open	Short
97	30kΩ ± 5%	15kΩ ± 5%
98	30kΩ ± 5%	60kΩ ± 5%
99	Short	Open

Negative Resistance

The negative resistance is specified for the crystal oscillator of the tuner in the following configuration:

- Uses a 16MHz (ABLS2-16.000MHz-D4Y-T) crystal from Abracon, a crystal manufacturer.
- On-chip crystal loading capacitors is programmed to 25pF.

GPO Control

The MxL608 provides one GPO pin for external circuit control. The GPO pin is open drain and requires an external pull-up resistor. The VDD voltage range can be supported from 1.8V to 3.3V.

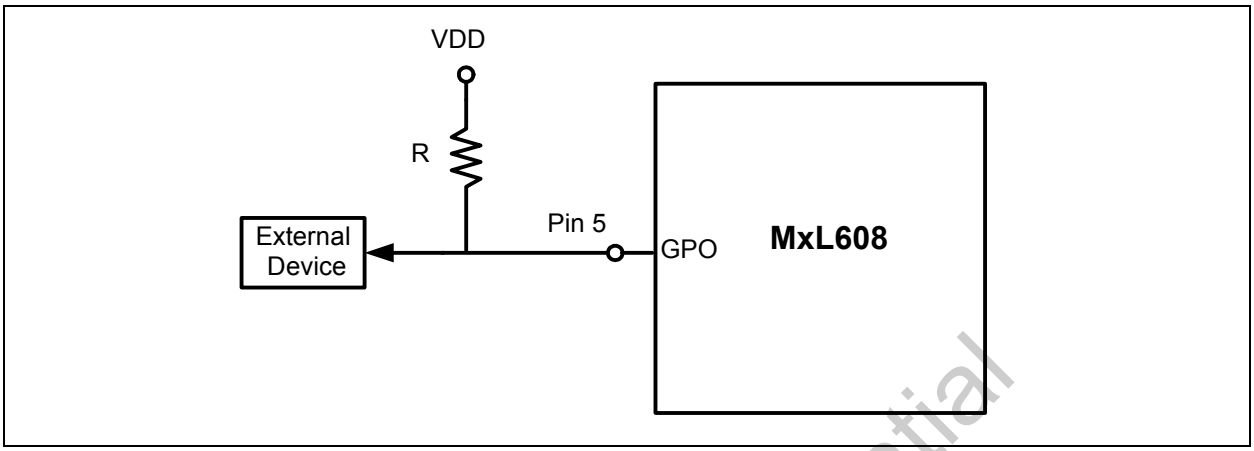

Figure 7: GPO Control

Operating Modes Control

The MxL608 supports the three operating modes of Sleep, Standby, and Active. The MxL608 is in the Sleep mode after the reset signal asserts. All the registers are in the default value. After a certain tuning sequence (e.g., channel frequency, BW, IF, etc.), the MxL608 operates in the Active mode. To save power while not in use, program the MxL608 into the Standby mode. In Standby mode, all the registers are stored from the Active mode and unnecessary blocks are shut off. During the switch of Active and Standby modes, the clock output has no disturbance and the GPO status remains the same.

AGC Voltage Range

The maximum voltage AGC pin can support is up to 3.6V, but the effective range is from 0 to approximately 2.4V.

Supply Ripple Susceptibility

For details, refer to the *MxL608 Digital Tuner Reference Design Guide (001-DGR)*.

FBE and In-Band Ripple Definition

The FBE and in-band ripple are defined in the plot illustrated in the following figure.

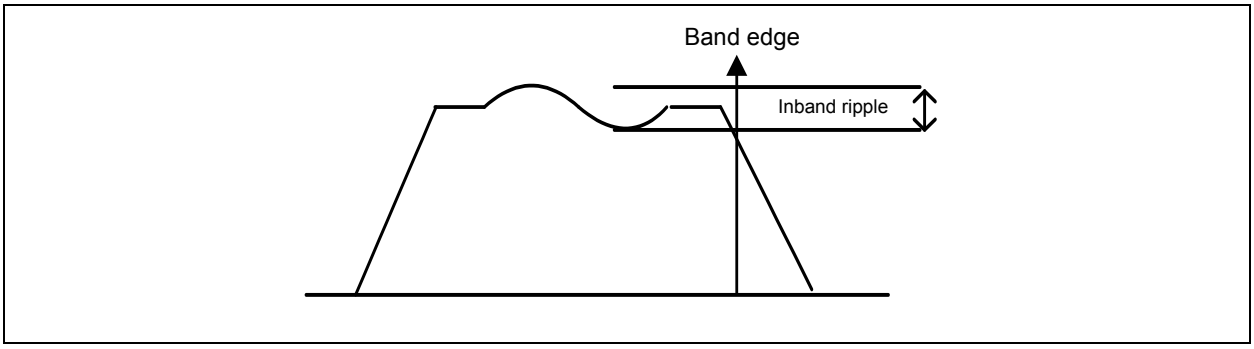

Figure 8: FBE and In-Band Ripple Definition

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