N-Channel Enhancement Mode MOSFET

GENERAL DESCRIPTION

The ME2302 is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 85m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leqq 115m\Omega @ V_{GS}=2.5V$
- $R_{DS(ON)} \leqq 135m\Omega @ V_{GS}=1.8V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Notebook
- Portable Equipment
- Load Switch
- DSC

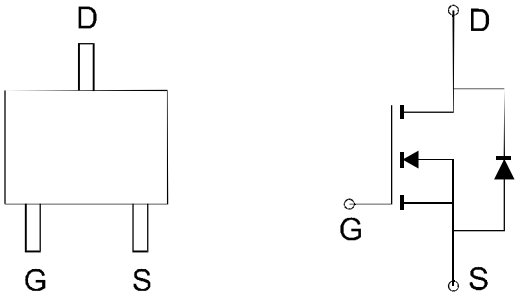
ORDER INFORMATION

Device	Package
ME2302	SOT-23

PIN CONFIGURATION

(SOT-23)

Top View



PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	5 sec	Steady State	Unit
Drain-Source Voltage		V_{DSS}	20		V
Gate-Source Voltage		V_{GSS}	±8		V
Continuous Drain Current(tJ=150℃)	T_A=25℃	I_D	2.8		A
	T_A=70℃		2.2		
Pulsed Drain Current		I_{DM}	10		
Maximum Body-Diode Continuous Current		I_S	1.6		A
Maximum Power Dissipation	T_A=25℃	P_D	1.25		W
	T_A=70℃		0.8		
Operating Junction Temperature		T_J	150		℃
Maximum Junction-to-Ambient		R_{thJA}	T≦10 sec	77	℃/W
			Steady State	105	
Thermal Resistance-Junction to Case		$R_{\theta JC}$	70		℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

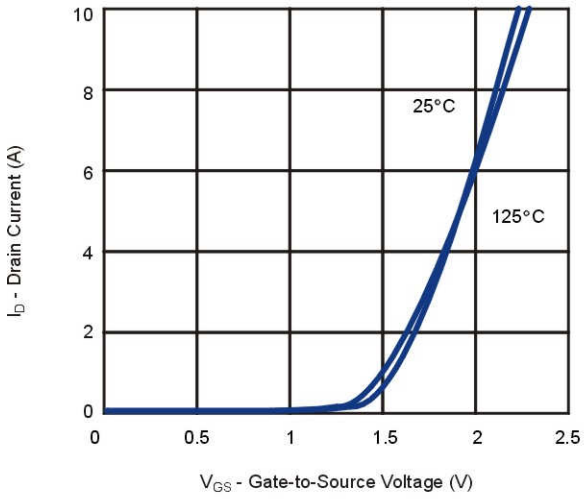
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC PARAMETERS						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.6	0.9	1.2	
I_{GSS}	Gate-Body Leakage Current	V_{DS}=0V, V_{GS}=±8V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V			1	μA
		V_{DS}=20V, V_{GS}=0V T_J=55℃			10	
$I_{D(ON)}$	On-State Drain Current [a]	V_{DS}≧5V, V_{GS}= 4.5V	6			A
		V_{DS}≧5V, V_{GS}= 2.5V	4			
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=4.5V, I_D= 2.8A		55	85	mΩ
		V_{GS}=2.5V, I_D= 2.5A		65	115	
		V_{GS}=1.8V, I_D= 2.2A		80	130	
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.75	1.2	V
DYNAMIC PARAMETERS						
Qg	Total Gate Charge	V_{DS}=10V, V_{GS}=4.5V, I_D=2.8A		9		nC
Qgs	Gate-Source Charge			2.2		
Qgd	Gate-Drain Charge			3		
Ciss	Input Capacitance	V_{DS}=10V, V_{GS}=0V, f=1MHz		350		pF
Coss	Output Capacitance			90		
Crss	Reverse Transfer Capacitance			20		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=10V, R_L=10Ω V_{GEN}=4.5Ω, R_G=6Ω		9		ns
tr	Rise Time			23		
$t_{d(off)}$	Turn-Off Delay Time			38		
t_f	Fall Time			3		

Notes:

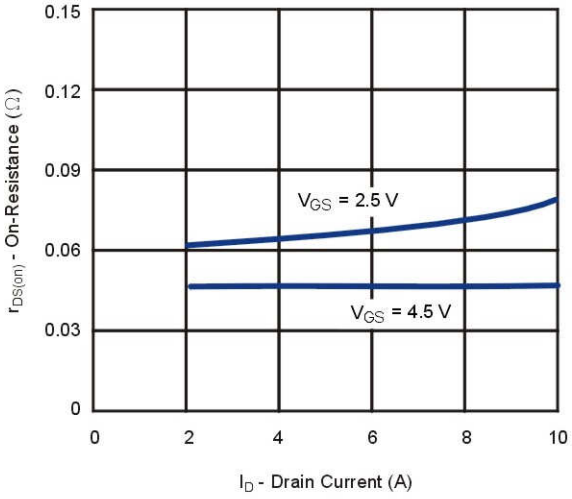
a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

Typical Characteristics (T_J =25℃ Noted)

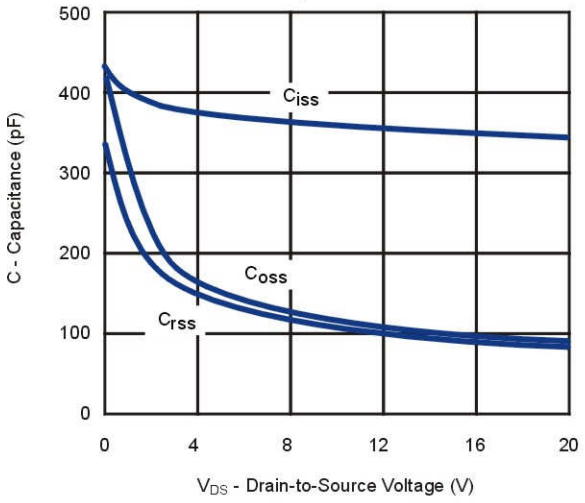
Transfer Characteristics



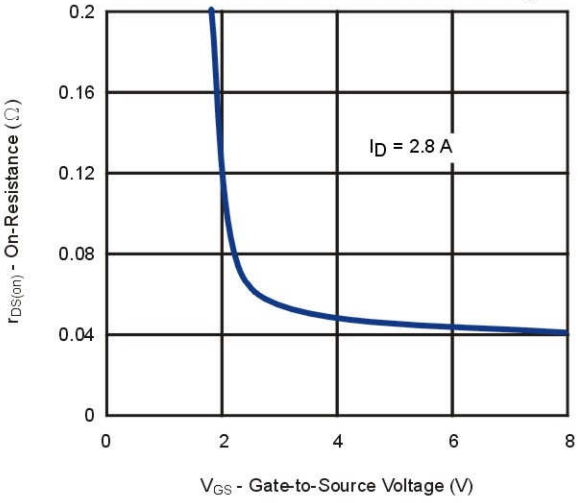
On-Resistance vs. Drain Current



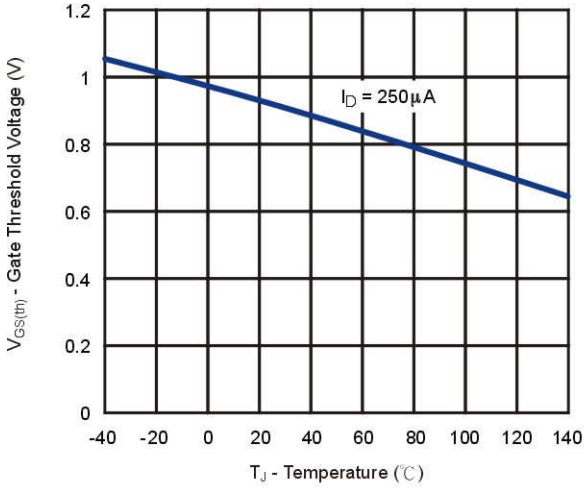
Capacitance



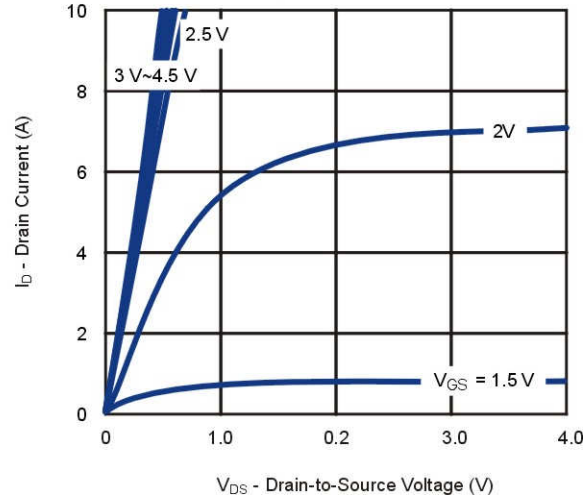
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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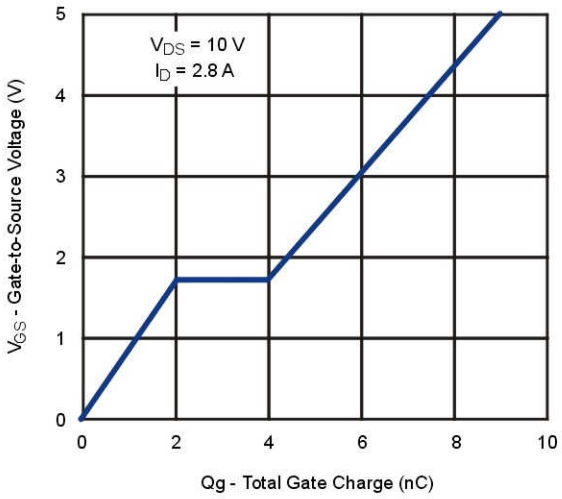
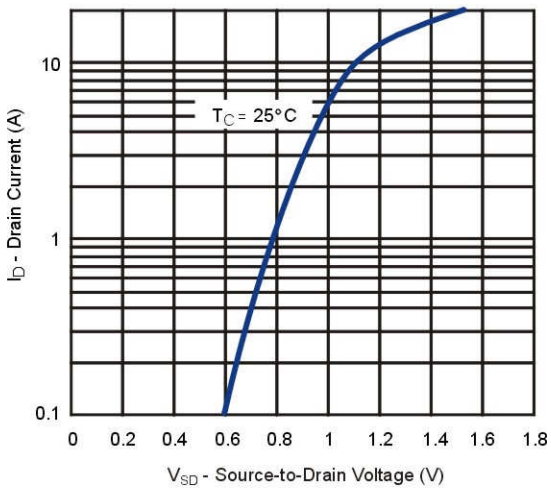
Typical Characteristics (T_J =25℃ Noted)

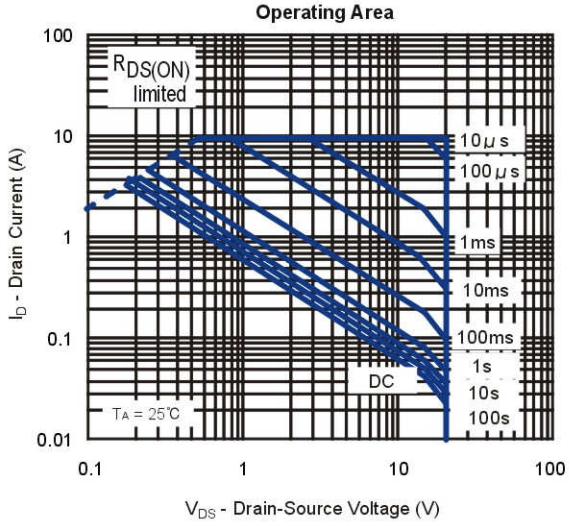
Gate Charge



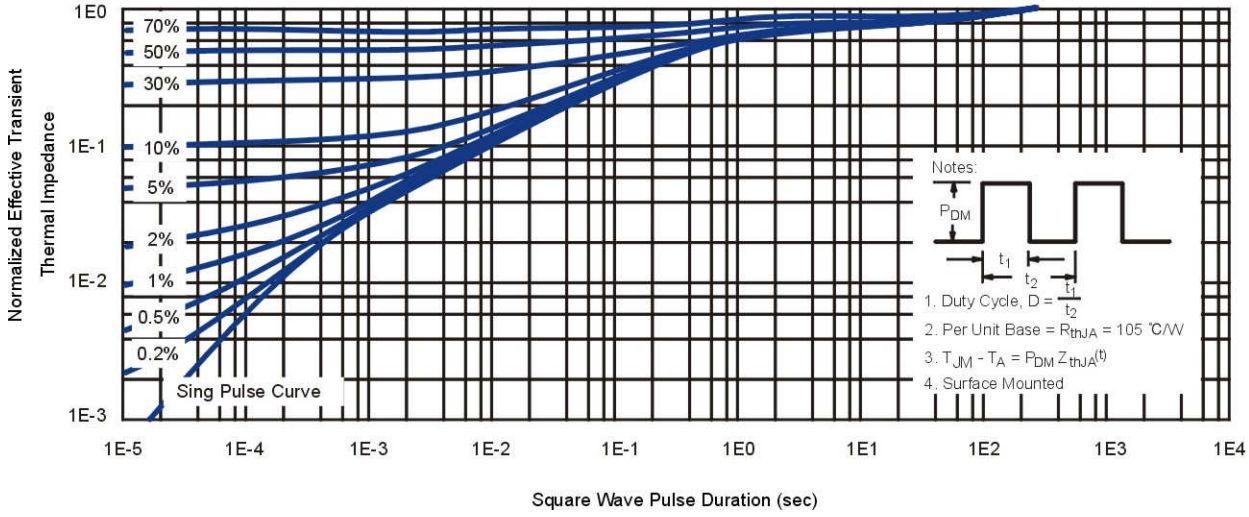
On-Resistance vs. Drain Current



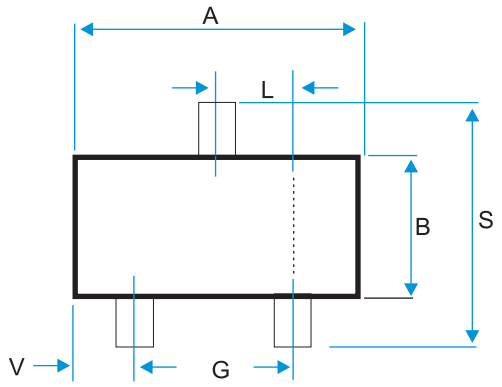
Maximum Forward Biased Safe Operating Area

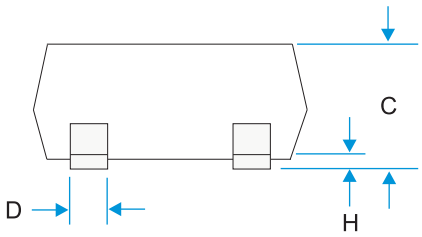


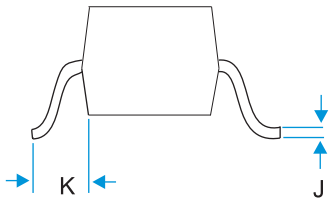
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline







DIM	MILLIMETERS	
	MIN	MAX
A	2.80	3.1
B	1.20	1.7
C	0.89	1.3
D	0.37	0.50
G	1.78	2.04
H	0.013	0.15
J	0.085	0.2
K	0.45	0.7
L	0.89	1.02
S	2.10	3
V	0.45	0.60