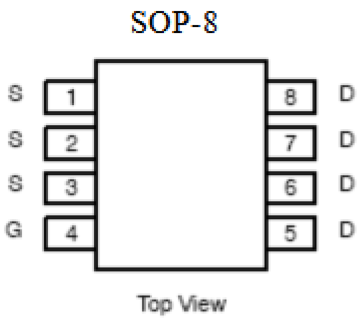
1. Features

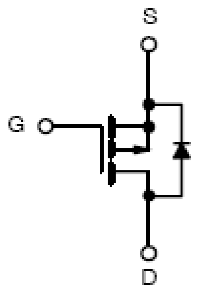
- $R_{DS(on)}$=40mΩ(typ)@ V_{GS}=-10 V
- Super low gate charge
- Green device available
- Excellent Cdv/dt effect decline
- Advanced high cell density trench technology

2.Description

The KIA9435A is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KIA9435A meet the RoHs and Green Product requirement.

3.Symbol





P-Channel MOSFET

4.Absolute maximum ratings

(T_A=25°C,unless otherwise noted)

Parameter		Symbol	Rating	Units
Drain-source voltage		V_{DSS}	-30	V
Gate-source voltage		V_{GS}	±20	V
Continuous drain current V_{GS}@10V[1]	T_A=25ºC	I_D	-5.3	A
	T_A=70ºC		-3.9	
Pulsed drain current[2]		I_{DM}	-25	A
Single pulse avalanche energy[3]		EAS	18.1	mJ
Avalanche current		I_{AS}	-19	A
Total power dissipation[4]	T_A=25ºC	P_D	1.5	W
Junction and storage temperature range		T_J,T_{STG}	-55 to150	ºC
Thermal resistance-junction to ambient[1]		$R_{θJA}$	85	ºC/W
Thermal resistance-junction to case[1]		$R_{θJC}$	25	ºC/W

5.Electrical characteristics

(T_J=25°C,unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-30	-	-	V
BV_{DSS} Temperature coefficient	△BV_{DSS}/△T_J	Reference to 25 ºC, I_D=-1mA	-	-0.023	-	V/ ºC
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-24V,V_{GS}=0V, T_J=25°C	-	-	1	μA
		V_{DS}=-24V,V_{GS}=0V, T_J=55°C	-	-	5	
Gate-source leakage current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	-1.2	-	-2.5	V
$V_{GS(th)}$Temperature coefficient	△$V_{GS(th)}$		-	4	-	mV/ºC
Static drain-source on- resistance[2]	$R_{DS(on)}$	V_{GS}=-10V,I_D=-4A	-	40	45	mΩ
		V_{GS}=-4.5V,I_D=-3A	-	62	78	
Forward transcend ductance	g_{FS}	V_{DS}=-5V, I_D=-4A	-	11	-	S
Total gate charge(-4.5V)	Q_g	V_{DS}=-15V, V_{GS}=-4.5V I_D =-4A	-	6.4	-	nC
Gate-source charge	Q_{gs}		-	2.3	-	
Gate-drain charge	Q_{gd}		-	2	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=-15V, R_G=3.3Ω, V_{GS}=-10V I_D=-4A	-	2.8	-	ns
Rise time	t_r		-	8.4	-	
Turn-off delay time	$t_{d(off)}$		-	39	-	
Fall time	t_f		-	6	-	
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-15V F=1.0MHZ	-	585	-	pF
Output capacitance	C_{oss}		-	100	-	
Reverse transfer capacitance	C_{rss}		-	85	-	
Diode characteristics						
Continuous source current[1,5]	I_S	V_G=V_D=0V,Force current	-	-	-5.3	A
Pulsed source current[2,5]	I_{SM}		-	-	-25	A
Diode forward voltage[2]	V_{SD}	V_{GS}=0V,I_S=-1A, T_J=25°C	-	-	1.2	V
Reverse recovery time	t_{rr}	I_F=-4A,dl/dt=100A/us, T_J=25°C	-	7.8	-	nS
Reverse recovery charge	Q_{rr}		-	2.5	-	nC

Note:1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2. The data tested by pulsed, pulse width ≤300us,duty cycle ≤2%.

3. The EAS data shows Max.rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-19A.

4. The power dissipation is limited by 150 ºC junction temperature.

5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

6. Test circuits and waveforms

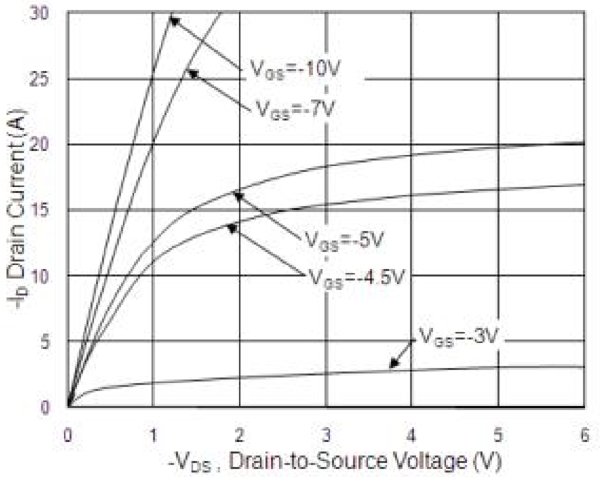


Fig.1 Typical Output Characteristics

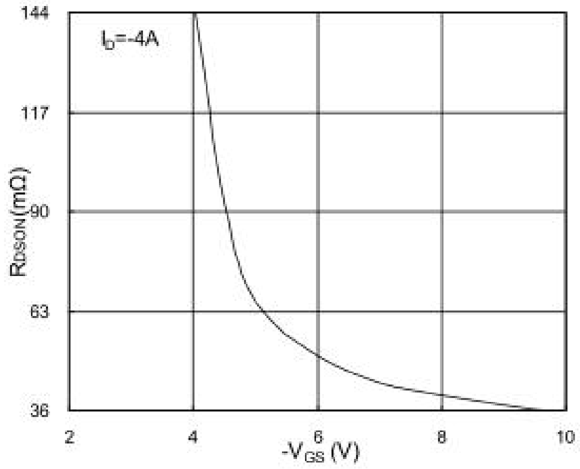


Fig.2 On-Resistance vs. Gate-Source

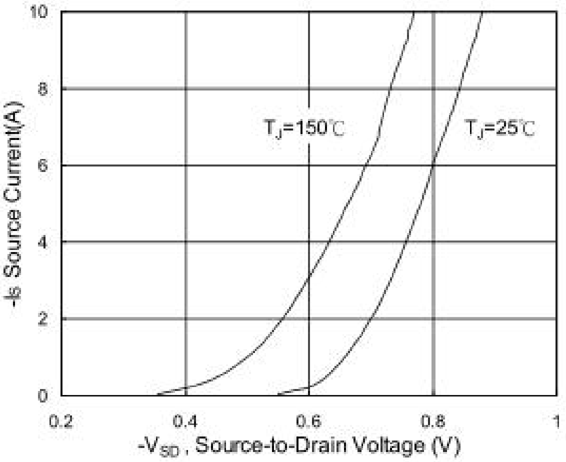


Fig.3 Forward Characteristics of Reverse

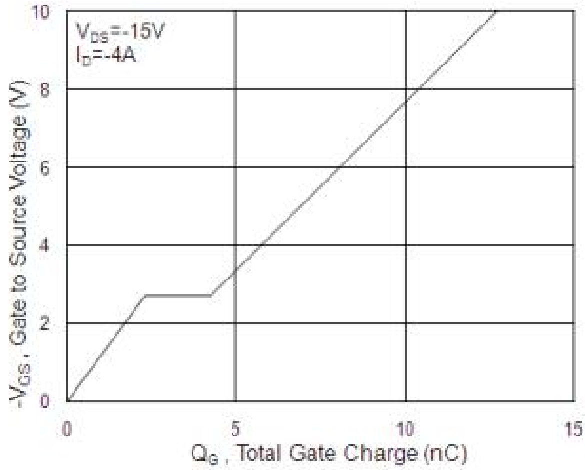


Fig.4 Gate-Charge Characteristics

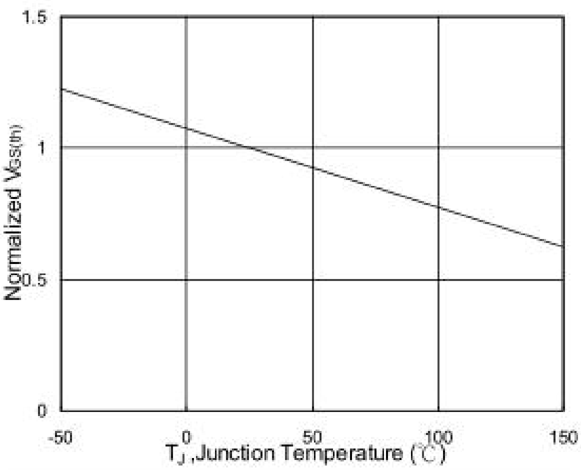


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

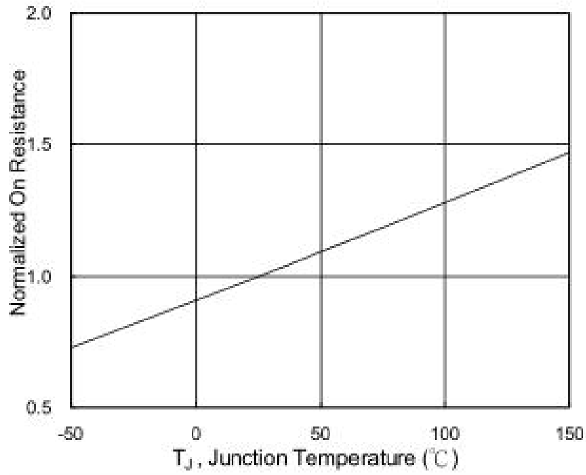


Fig.6 Normalized R_{DSON} vs. T_J

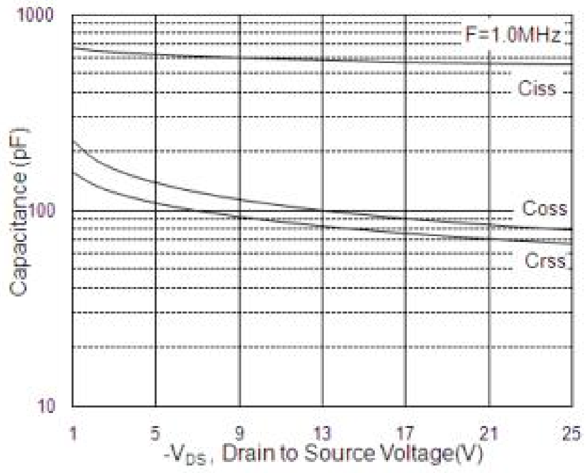


Fig.7 Capacitance

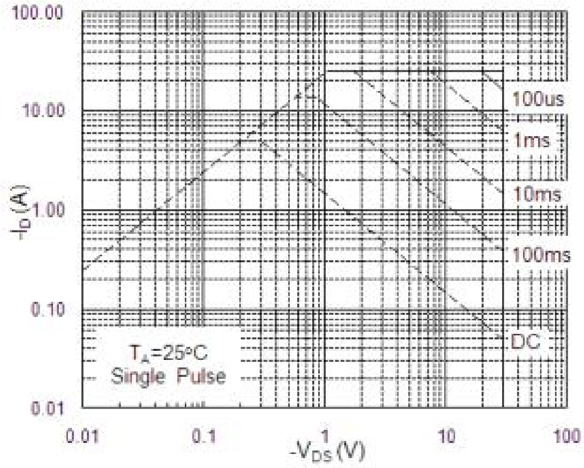


Fig.8 Safe Operating Area

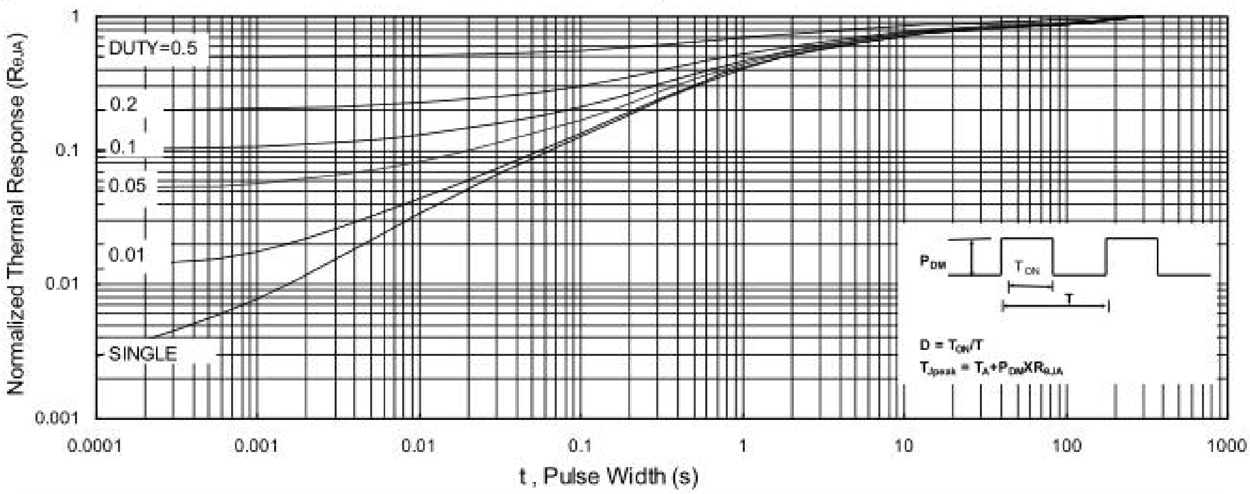


Fig.9 Normalized Maximum Transient Thermal Impedance

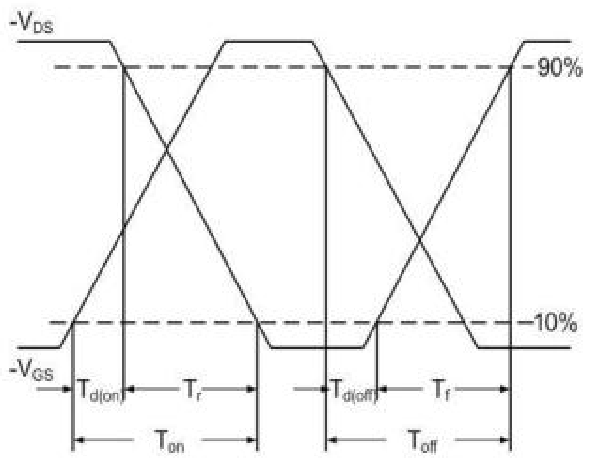


Fig.10 Switching Time Waveform

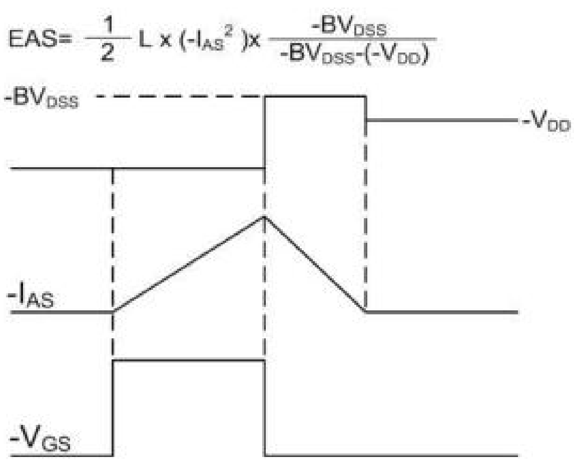


Fig.11 Unclamped Inductive Switching Waveform