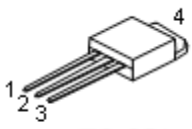
## 1. Description

KIA7610A designed by the trench processing techniques to achieve extremely low on-resistance. ATditional features of this design are a 175℃ junction operating temperature,fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in DC-DC Converters and Off-line UPS and a wide variety of other applications.

## 2. Features

- $R_{DS(on)}$ =32mΩ
- Low On-resistance
- Fast switching
- 100% avalanche tested
- Repetitive avalanche allowed up to tjmax
- LeAT-Free,RoHS compliant

## 3. Pin configuration



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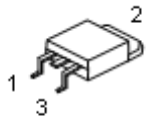

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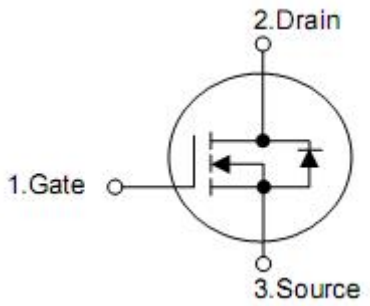


| Pin | Function |
|---|---|
| 1 | Gate |
| 2 | Drain |
| 3 | Source |
| 4 | Drain |

## 4. Absolute maximum ratings

($T_C$=25ºC , unless otherwise noted)

| Parameter | | Symbol | Rating | Units |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DSS}$ | 100 | V |
| Drain current continuous | $T_C$=25ºC | $I_D$ | 25 | A |
| | $T_C$=100ºC | | 16 | A |
| Drain current pulsed (note1) | $T_C$=25ºC | $I_{DM}$ | 100 | A |
| Gate-source voltage | | $V_{GSS}$ | ±20 | V |
| Single Pulse avalanche energy (note2) | | $E_{AS}$ | 90 | mJ |
| Power dissipation | $T_C$=25ºC | $P_D$ | 60 | W |
| Maximum junction temperature | | $T_J$ | 175 | ºC |
| Operating and storage temperature range | | $T_{STG}$ | -55~+175 | ºC |
| Diode continuous forward current (note1) | $T_C$=25ºC | $I_S$ | 25 | A |

## 5. Thermal characteristics

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Thermal resistance junction-case | $R_{thJC}$ | - | 1.8 | ºC/W |
| Thermal resistance junction-ambient | $R_{thJA}$ | - | 75 | |

## 6. Electrical characteristics

($T_J$=25°C,unless otherwise noted)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Off characteristics | | | | | | | |
| Drain-source breakdown voltage | | $BV_{DSS}$ | $V_{GS}$=0V,$I_D$=250μA | 100 | - | - | V |
| Zero gate voltage drain current | $T_C$=25°C | $I_{DSS}$ | $V_{DS}$=100V,$V_{GS}$=0V | - | - | 10 | μA |
| | $T_C$=125°C | | $V_{DS}$=100V,$V_{GS}$=0V | - | - | 100 | μA |
| Gate-body leakage current | | $I_{GSS}$ | $V_{GS}$=±20V,$V_{DS}$=0V | - | - | ±100 | nA |
| On characteristics | | | | | | | |
| Gate threshold voltage | | $V_{GS(TH)}$ | $V_{DS}$=$V_{GS}$,$I_D$=250μA | 1.0 | 1.5 | 3.0 | V |
| Static drain-source on-resistance | | $R_{DS(ON)}$ | $V_{GS}$=10V,$I_D$=14A | - | 32 | 38 | mΩ |
| Dynamic characteristics | | | | | | | |
| Input capacitance | | $C_{ISS}$ | $V_{DS}$=50V,$V_{GS}$=0V, f=1MHz | - | 2020 | - | pF |
| Output capacitance | | $C_{OSS}$ | | - | 450 | - | pF |
| Reverse transfer capacitance | | $C_{RSS}$ | | - | 255 | - | pF |
| Switching characteristics | | | | | | | |
| Turn-on delay time | | $t_{D(ON)}$ | $V_{DD}$=50V,$R_G$=6.8Ω, $I_D$=1A ,$V_{GS}$=10V, $R_L$=25Ω, | - | 25 | - | ns |
| Rise time | | $t_R$ | | - | 19 | - | ns |
| Turn-off delay time | | $t_{D(OFF)}$ | | - | 58 | - | ns |
| Fall time | | $t_F$ | | - | 75 | - | ns |
| Total gate charge | | $Q_G$ | $V_{DS}$=50V,$V_{GS}$=10V $I_D$=10A | - | 55 | - | nC |
| Gate-source charge | | $Q_{GS}$ | | - | 13.6 | - | nC |
| Gate-drain charge | | $Q_{GD}$ | | - | 11.2 | - | nC |
| Drain-source diode characteristics | | | | | | | |
| Continuous drain-source current | | $I_S$ | | - | - | 25 | A |
| Drain-source diode forward voltage | | $V_{SD}$ | $V_{GS}$=0V,$I_S$=12A | - | 0.82 | 1.3 | V |
| Reverse recovery time | | $t_{RR}$ | $V_{GS}$=0V,$I_F$=12A, $di_F/dt$=100A/μs | - | 60 | - | nS |
| Reverse recovery charge | | $Q_{RR}$ | | - | 95 | - | nC |

Note:1. Pulse width ≤300μs, duty cycle≤2% pulse width limited by maximum junction temperature

2. Limited by Tjmax,starting TJ=25℃,L=0.5mH,RG=25Ω,IAS=19A,VGS=10V

## 7. Test circuits and waveforms

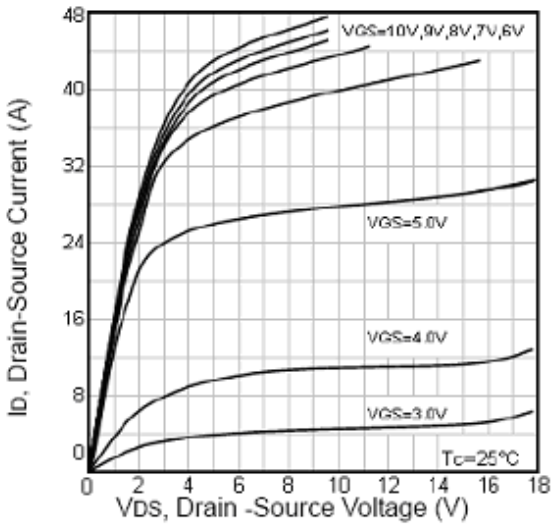


Fig1. Typical Output Characteristics

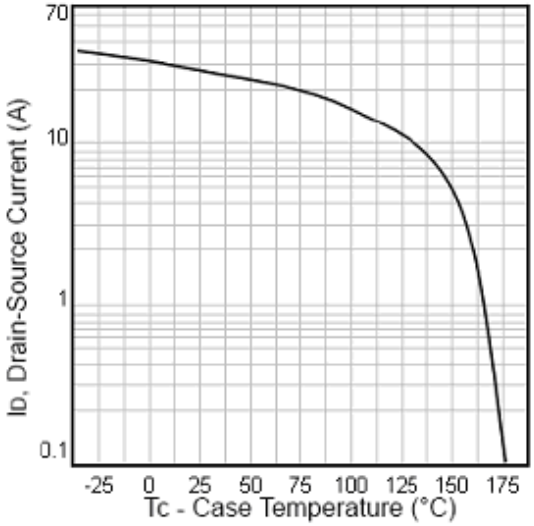


Fig2. Maximum Drain Current Vs.Case Temperature

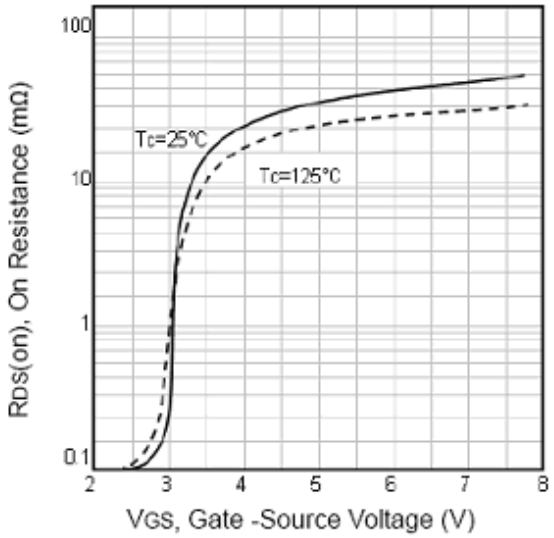


Fig3. Typical On Resistance Vs. Gate -Source

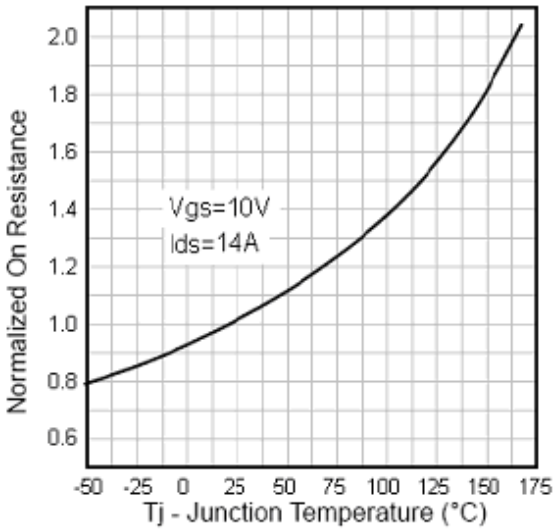


Fig4. Normalized On-Resistance Vs. Temperature

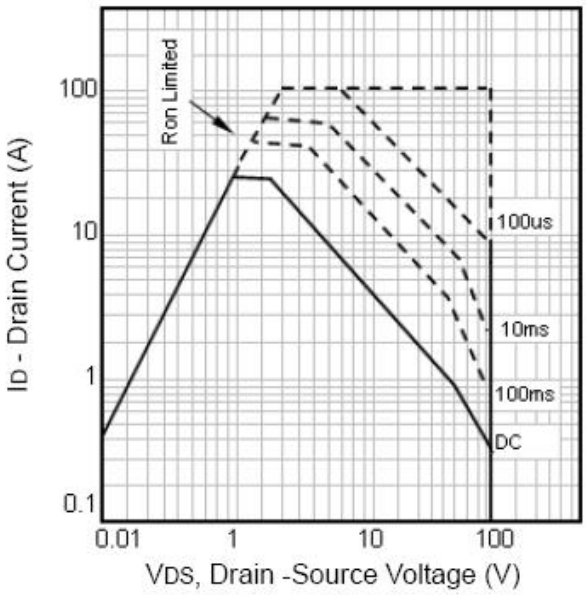


Fig5. Maximum Safe Operating Area

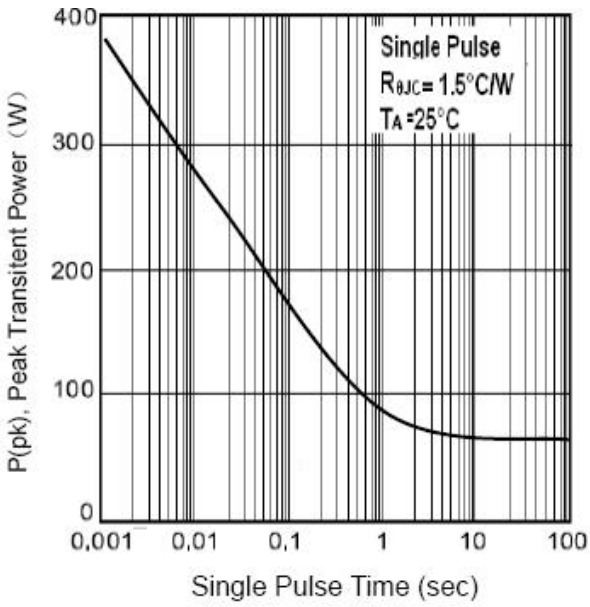


Fig6. Typical Transitent Power

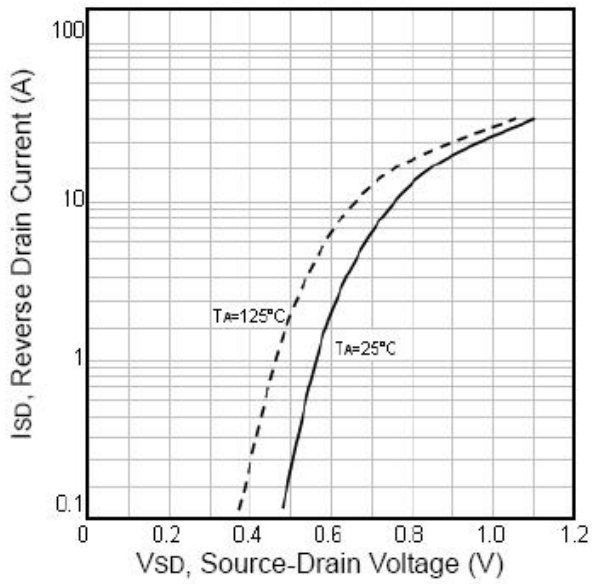


Fig7. Typical Source-Drain Diode Forward Voltage

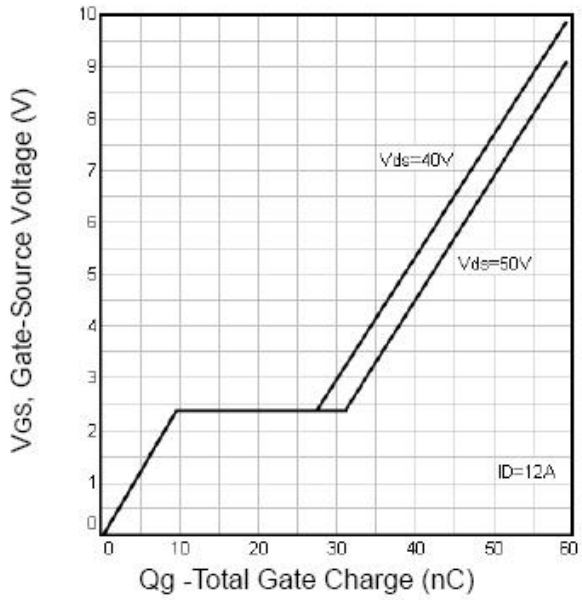


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

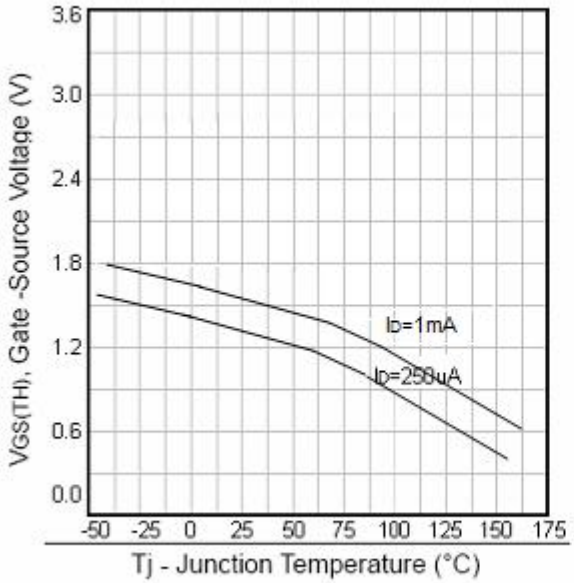


Fig9. Threshold Voltage Vs. Temperature

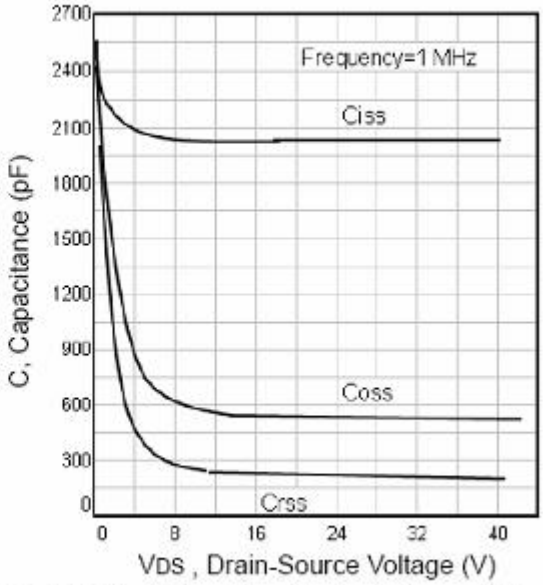


Fig10. Typical Capacitance Vs.Drain-Source Voltage

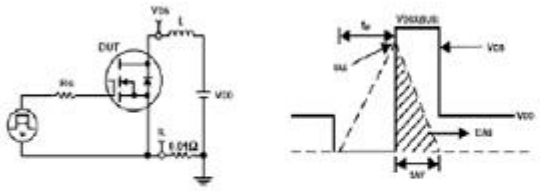

Fig11. Unclamped Inductive Test Circuit and waveforms

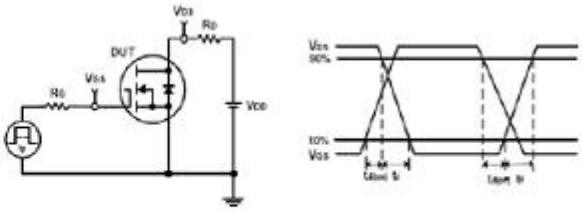

Fig12. Switching Time Test Circuit and waveforms