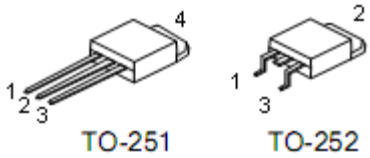
1. Features

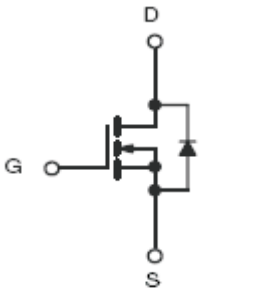
- $R_{DS(on)}$=77mΩ @ V_{GS}=10V
- Super low gate charge
- Green device available
- Excellent Cdv/dt effect decline
- Advanced high cell density trench technology

2.Description

The KIA7115A is the highest performance trenched N-ch MOSFETs with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KIA7115A meet the RoHs and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

3.Symbol





4.Absolute maximum ratings

(T_A=25°C,unless otherwise noted)

Parameter		Symbol	Rating	Units
Drain-source voltage		V_{DSS}	150	V
Gate-source voltage		V_{GS}	±20	V
Continuous drain current V_{GS}@10V[1]	T_C=25ºC	I_D	20	A
	T_C=100ºC		14	
	T_A=25ºC		3	
	T_A=70ºC		2.5	
Pulsed drain current[2]		I_{DM}	40	A
Single pulse avalanche energy[3]		EAS	53	mJ
Avalanche current		I_{AS}	18	A
Total power dissipation[3]	T_C=25ºC	P_D	72.6	W
	T_A=25ºC		2.1	W
Junction and storage temperature range		T_J ,T_{STG}	-55 to150	ºC
Thermal resistance-junction to ambient[1]		$R_{θJA}$	60	ºC/W
Thermal resistance-junction to case[1]		$R_{θJC}$	1.72	ºC/W

5.Electrical characteristics

(T_J=25°C,unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	150	-	-	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=120V,V_{GS}=0V, T_J=25°C	-	-	1	μA
		V_{DS}=120V,V_{GS}=0V, T_J=55°C	-	-	5	
Gate-source leakage current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.2	-	2.5	V
Static drain-source on- resistance[2]	$R_{DS(on)}$	V_{GS}=10V,I_D=10A	-	77	88	mΩ
		V_{GS}=4.5V,I_D=10A	-	82	100	
Forward transcend ductance	g_{FS}	V_{DS}=5V, I_D=10A	-	33	-	S
Total gate charge(10V)	Q_g	V_{DS}=75V, V_{GS}=4.5V I_D =10A	-	25.1	-	nC
Gate-source charge	Q_{gs}		-	6.8	-	
Gate-drain charge	Q_{gd}		-	12.6	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=75V, R_G=3.3Ω, V_{GS}=10V I_D=10A	-	13	-	ns
Rise time	t_r		-	8.2	-	
Turn-off delay time	$t_{d(off)}$		-	25	-	
Fall time	t_f		-	11	-	
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V F=1.0MHZ	-	2285	-	pF
Output capacitance	C_{oss}		-	110	-	
Reverse transfer capacitance	C_{rss}		-	83	-	
Diode characteristics						
Continuous source current[1.5]	I_S	V_G=V_D=0V,Force current	-	-	20	A
Pulsed source current[2.5]	I_{SM}		-	-	40	A
Diode forward voltage[2]	V_{SD}	V_{GS}=0V,I_S=-1A, T_J=25°C	-	-	1.2	V
Reverse recovery time	t_{rr}	I_F=10A,dI/dt=100A/us, T_J=25°C	-	37	-	nS
Reverse recovery charge	Q_{rr}		-	263	-	nC

Note:1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2. The data tested by pulsed, pulse width ≤300us,duty cycle ≤2%.

3. The EAS data shows Max.rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.3mH, I_{AS}=18A.

4. The power dissipation is limited by 150 ºC junction temperature.

5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

6. Test circuits

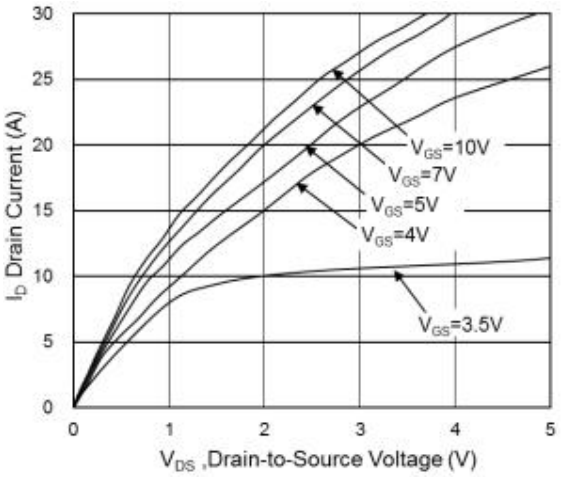


Fig.1 Typical Output Characteristics

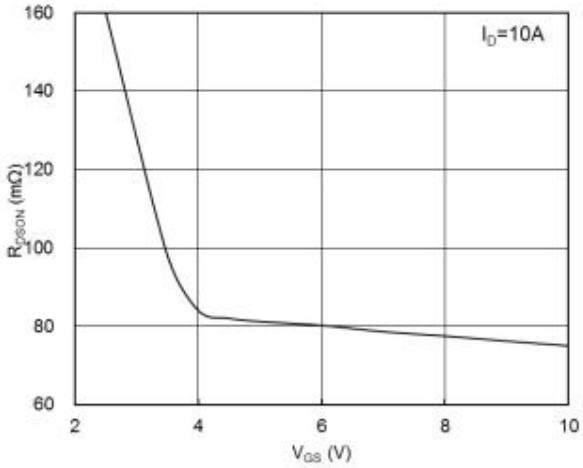


Fig.2 On-Resistance vs. Gate-Source Voltage

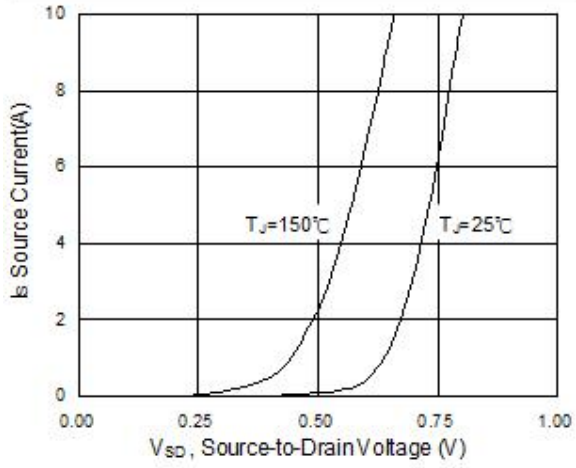


Fig.3 Forward Characteristics of Reverse

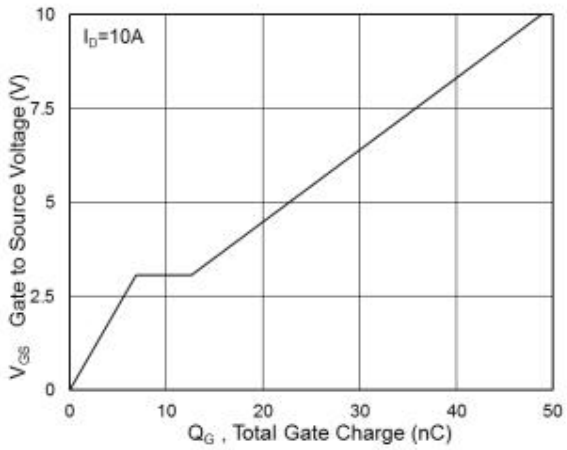


Fig.4 Gate-Charge Characteristics

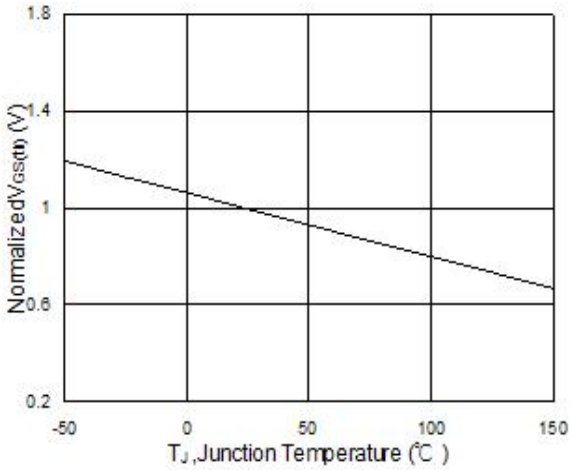


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

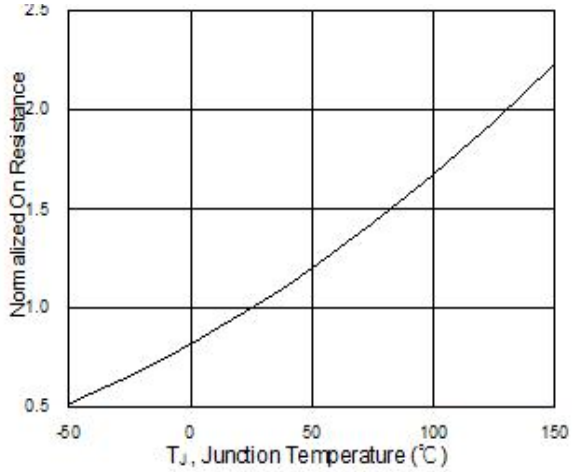


Fig.6 Normalized R_{DSON} vs. T_J

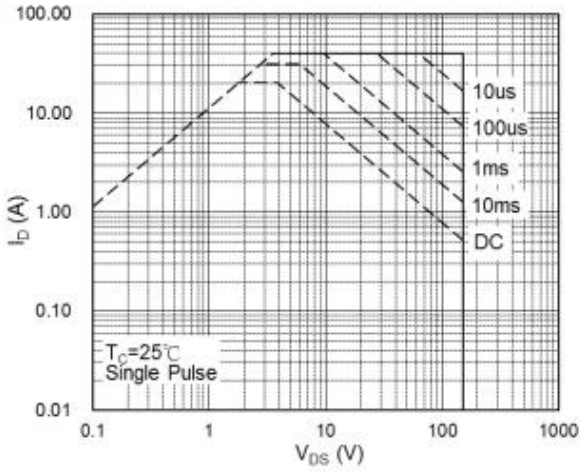


Fig.7 Capacitance

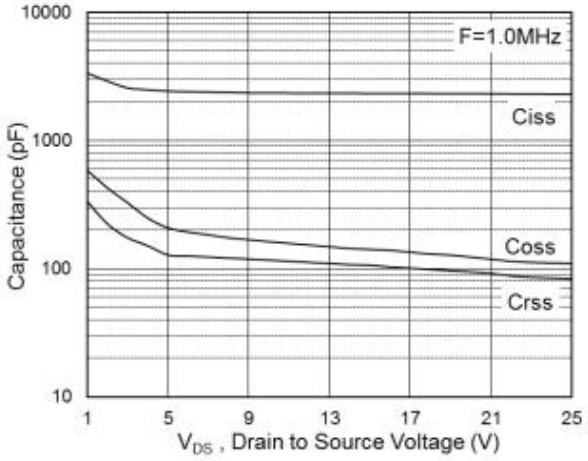


Fig.8 Safe Operating Area

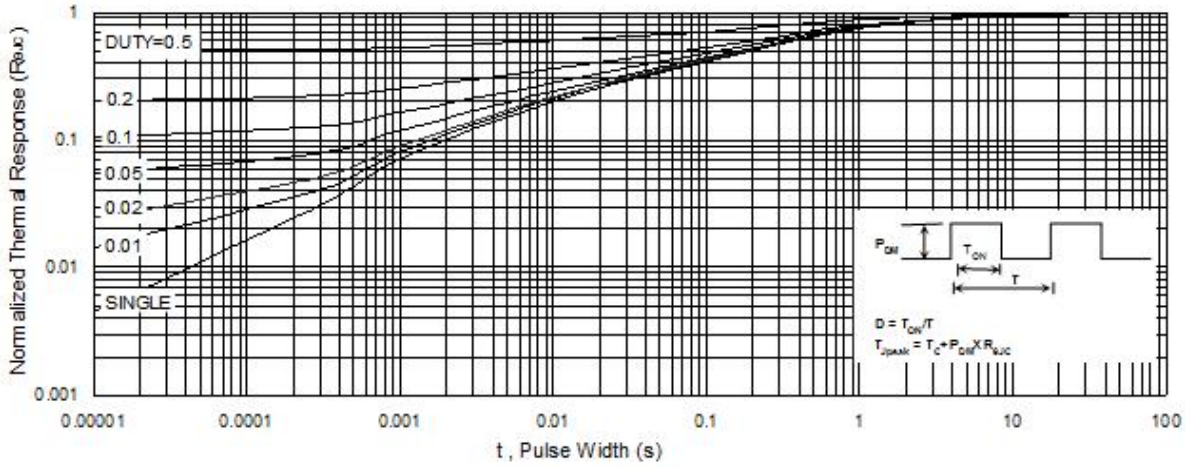


Fig.9 Normalized Maximum Transient Thermal Impedance

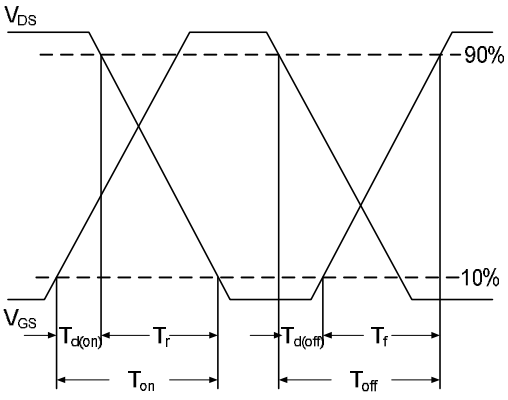


Fig.10 Switching Time Waveform

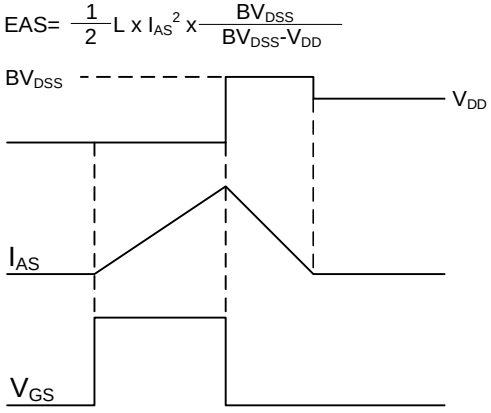


Fig.11 Unclamped Inductive Switching Waveform