Universal High Brightness LED Driver

Halogen Free

General Description

The FP7171 is an open loop, current mode, control LED driver IC. The FP7171 can be programmed to operate in either a constant frequency or constant off-time mode. It includes an 8.5 - 450V linear regulator which allows it to work from a wide range of input voltages without the need for an external low voltage supply. The FP7171 includes a PWM dimming and 0 - 250mV linear dimming input which can be used for linear dimming of the LED current. The FP7171 is ideally suited for buck LED drivers. Since the FP7171 operates in open loop current mode control, the controller achieves good output current regulation without the need for any loop compensation.

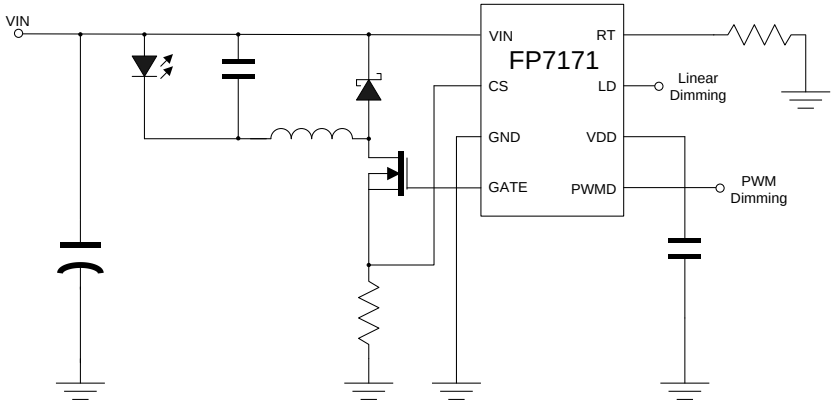
Features

- Switch mode controller for single switch LED drivers
- Enhanced drop-in replacement to the FP7171
- Open loop peak current controller
- Internal 8.5 to 450V linear regulator
- Constant frequency or constant off-time operation
- Linear and PWM dimming capability
- Requires few external components for operation

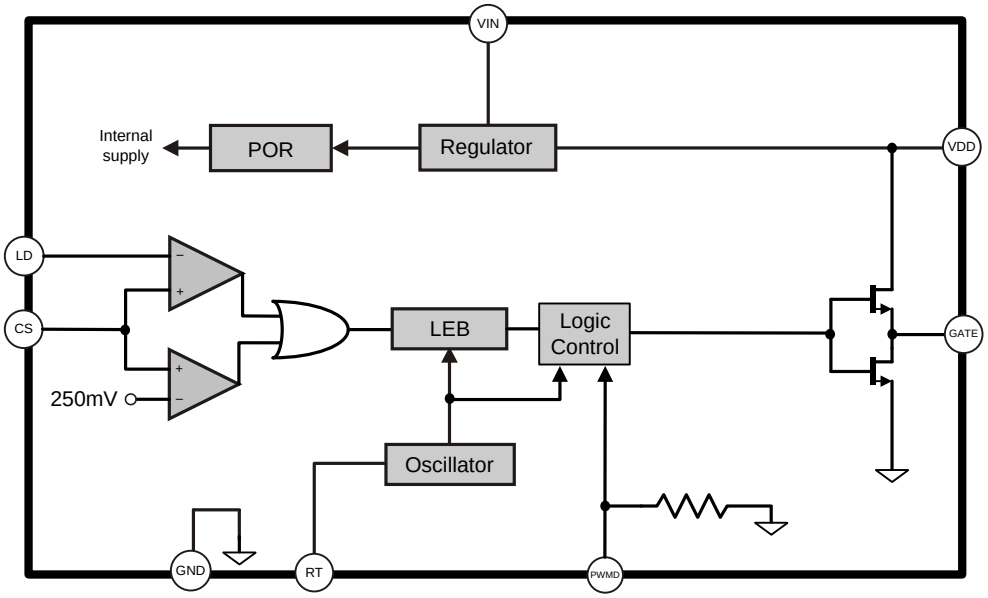
Applications

- DC/DC or AC/DC LED driver applications
- RGB backlighting LED driver
- Back lighting of flat panel displays
- General purpose constant current source
- Signage and decorative LED lighting
- Chargers

Typical Application Circuit

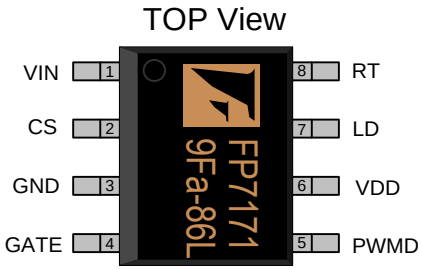


Function Block Diagram



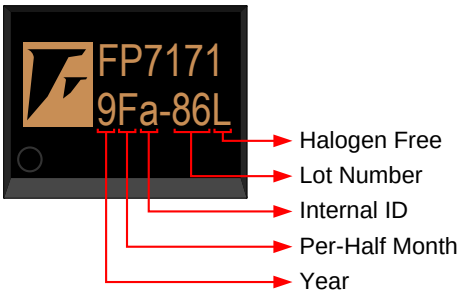
Pin Descriptions

SOP-8L



Name	No.	I / O	Description
VIN	1	I	This pin is the input of an 8.5 - 450V linear regulator.
CS	2	I	This pin is the current sense pin used to sense the FET current by means of an external sense resistor.
GND	3	P	Ground return for all internal circuitry.
GATE	4	O	This pin is the output GATE driver for an external N-channel power MOSFET.
PWMD	5	I	This is the PWM dimming input of the IC.
VDD	6	I	This is the power supply pin for all internal circuits.
LD	7	I	This pin is the linear dimming input of the IC.
RT	8	I	This pin sets the oscillator frequency. When a resistor is connected between RT and GND, the FP7171 operates in constant frequency mode. When the resistor is connected between RT and GATE, the IC operates in constant off-time mode.

Marking Information



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Internal ID: Internal Identification Code

Per-Half Month: Production period indicated in half month time unit

For Example: January → A (Front Half Month), B (Last Half Month)

February → C (Front Half Month), D (Last Half Month)

Year: Production year's last digit

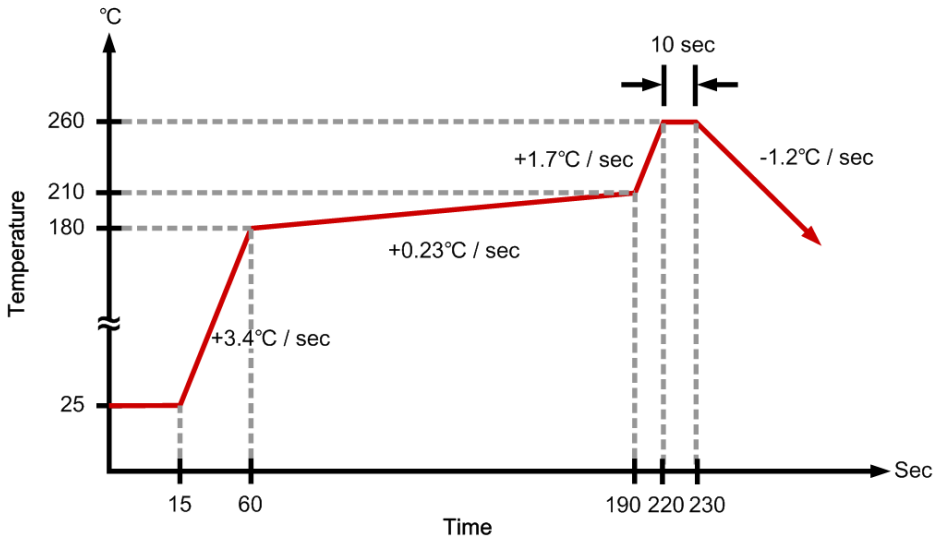
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP7171DR-G1	-25°C ~ +85°C	SOP-8L	2500 EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{IN}	V_{IN} to GND			470	V
	VDD	VDD to GND			8.5	V
CS, LD, PWMD, GATE, RT			-0.3		V_{DD}-0.3V	V
Allowable Power Dissipation	P_D	SOP-8L $T_A \leqq +25°C$			630	mW
Junction to Ambient Thermal Resistance	θ_{JA}			128		°C / W
Junction Temperature	T_J				+125	°C
Operating Temperature			-25		+85	°C
Storage Temperature	T_S	SOP-8L	-40		+150	°C
SOP-8L Lead Temperature		(soldering, 10 sec)			+260	°C

IR Re-flow Soldering Curve



Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		8.5		450	V
Operating Temperature Range	T_A		-25		85	°C

DC Electrical Characteristics (V_{CC}=8.5V,T_A = 25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Internal Regulator						
Internally regulated voltage	V_{DD}	VIN = 8.5V, $I_{DD(ext)}$= 0, 500pF at GATE; RT = 207kΩ , PWMD = VDD	7	7.5	8	V
Line regulation of VDD	Δ V_{DD}	VIN = 8.5 – 450V, $I_{DD(ext)}$=0, 500pF at GATE; RT = 207kΩ , PWMD = VDD	0	-	1.0	V
Internal Regulator						
Load regulation of V_{DD}	Δ $V_{DD,load}$	$I_{DD(ext)}$ = 0 - 1.0mA, 500pF at GATE; RT = 207kΩ , PWMD = VDD	0		100	mV
V_{DD} undervoltage lockout threshold	UVLO	V_{DD} rising	6.45	6.7	6.95	V
V_{DD} undervoltage lockout hysteresis	Δ UVLO	V_{DD} falling		500		mV
PWM Dimming						
Pin PWMD input low voltage	$V_{EN(lo)}$	V_{IN} = 10 - 450V			0.9	
Pin PWMD input high voltage	$V_{EN(hi)}$	V_{IN} = 10 - 450V	1.8			
Pin PWMD pull-down resistance at PWMD	R_{EN}	V_{PWMD} = 5.0V	50	100	150	kΩ
Current Sense Comparator						
Current sense pull-in threshold voltage	$V_{CS,TH}$	-25°C < T_A < +85°C	245	250	255	mV
Offset voltage for LD comparator	V_{OFFSET}		-12		12	mV
Current sense blanking interval	T_{BLANK}	0 < T_A < +85°C, V_{LD} = V_{DD}, V_{CS} = $V_{CS,TH}$ + 50mV after T_{BLANK}	150	215	280	ns
		-25 < T_A < +125°C, V_{LD} = V_{DD}, V_{CS} = $V_{CS,TH}$ + 50mV after T_{BLANK}	145	215	315	
Delay to output	t_{DELAY}			80	150	ns
Oscillator						
Oscillator frequency	f_{OSC}	R_T = 1.00MΩ	20	25	30	kHz
		R_T = 207kΩ	80	100	120	
GATE Driver						
GATE sourcing current	I_{SOURCE}	V_{GATE} = 0V, V_{DD} = 7.5V	165			mA
GATE sinking current	I_{SINK}	V_{GATE} = V_{DD}, V_{DD} = 7.5V	165			mA
GATE output rise time	t_{RISE}	C_{GATE} = 500pF, V_{DD} = 7.5V		30	50	ns
GATE output fall time	t_{FALL}	C_{GATE} = 500pF, V_{DD} = 7.5V		30	50	ns

Function Description

Input Voltage Regulator

The FP7171 can be powered directly from its VIN pin and can work from 8.5 - 450VDC at its VIN pin. When a voltage is applied at the VIN pin, the FP7171 maintains a constant 7.5V at the VDD pin. This voltage is used to power the IC and any external resistor dividers needed to control the IC. The VDD pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the output GATE driver.

The FP7171 can also be operated by supplying a voltage at the VDD pin greater than the internally regulated voltage. This will turn off the internal linear regulator of the IC and the FP7171 will operate directly off the voltage supplied at the VDD pin. Please note that this external voltage at the VDD pin should not exceed 8.5V.

Although the VIN pin of the FP7171 is rated up to 450V, the actual maximum voltage that can be applied is limited by the power dissipation in the IC. For example, if an 8-pin SOIC (junction to ambient thermal resistance Rθ,j-a = 128°C/ W) FP7171 draws about I_{IN} = 2.0mA from the VIN pin, and has a maximum allowable temperature rise of the junction temperature limited to about ΔT = 100°C, the maximum voltage at the VIN pin would be:

$$V_{IN(MAX)} = \frac{\Delta T}{R_{\theta,j\ a}} \times \frac{1}{I_{in}} = \frac{100^{o}C}{128^{o}C/W} \times \frac{1}{2mA} = 390V$$

In these cases, to operate the FP7171 from higher input voltages, a Zener diode can be added in series with the VIN pin to divert some of the power loss from the FP7171 to the Zener diode. In the above example, using a 100V zener diode will allow the circuit to easily work up to 450V.

The input current drawn from the VIN pin is a sum of the 1.0mA current drawn by the internal circuit and the current drawn by the GATE driver (which in turn depends on the switching frequency and the GATE charge of the external FET).

$$I_{IN} \approx 0.5mA + Q_G \times f_S$$

In the above equation, f_S is the switching frequency and QG is the GATE charge of the external FET (which can be obtained from the datasheet of the FET).

Current Sense

The current sense input of the FP7171 goes to the noninverting inputs of two comparators. The inverting terminal of one comparator is tied to an internal 250mV reference whereas the inverting terminal of the other comparator is connected to the LD pin. The outputs of both these comparators are fed into an OR GATE and the output of the OR GATE is fed into the reset pin of the flip-flop. Thus, the comparator which has the lowest voltage at the inverting terminal determines when the GATE output is turned off.

The outputs of the comparators also include a 150-280ns blanking time which prevents spurious turn-offs of the external FET due to the turn-on spike normally present in peak current mode control. In rare cases, this internal blanking might not be enough to filter out the turn-on spike. In these cases, an external RC filter needs to be added between the external sense resistor (R_{CS}) and the CS pin.

Please note that the comparators are fast (with a typical 80ns response time). Hence these comparators are more susceptible to be triggered by noise than the comparators of the FP7171. A proper layout minimizing external inductances will prevent false triggering of these comparators.

Oscillator

The oscillator in the FP7171 is controlled by a single resistor connected at the RT pin. The equation governing the oscillator frequency f_{OSC} is given by:

$$f_{OSC}(kHz)=\frac{20700}{R_T(k\Omega)}$$

If the resistor is connected between RT and GND, FP7171 operates in a constant frequency mode and the above equation determines the time-period. If the resistor is connected between RT and GATE, the FP7171 operates in a constant off-time mode and the above equation determines the offtime.

Linear Dimming

The Linear Dimming pin is used to control the LED current. There are two cases when it may be necessary to use the Linear Dimming pin.

- In some cases, it may not be possible to find the exact RCS value required to obtain the LED current when the internal 250mV is used. In these cases, an external voltage divider from the VDD pin can be connected to the LD pin to obtain a voltage (less than 250mV) corresponding to the desired voltage across RCS.

- Linear dimming may be desired to adjust the current level to reduce the intensity of the LEDs. In these cases, an external 0-250mV voltage can be connected to the LD pin to adjust the LED current during operation.

To use the internal 250mV, the LD pin can be connected to VDD.

Note:

Although the LD pin can be pulled to GND, the output current will not go to zero. This is due to the presence of a minimum on-time (which is equal to the sum of the blanking time and the delay to output time) which is about 450ns. This will cause the FET to be on for a minimum of 450ns and thus the LED current when LD = GND will not be zero. This current is also dependent on the input voltage, inductance value, forward voltage of the LEDs and circuit parasitics. To get zero LED current, the PWMD pin has to be used.

PWM Dimming

PWM Dimming can be achieved by driving the PWMD pin with a low frequency square wave signal. When the PWM signal is zero, the GATE driver is turned off and when the PWMD signal if high, the GATE driver is enabled. Since the PWMD signal does not turn off the other parts of the IC, the response of the FP7171 to the PWMD signal is almost instantaneous. The rate of rise and fall of the LED current is thus determined solely by the rise and fall times of the inductor current.

To disable PWM dimming and enable the FP7171 permanently, connect the PWMD pin to VDD.

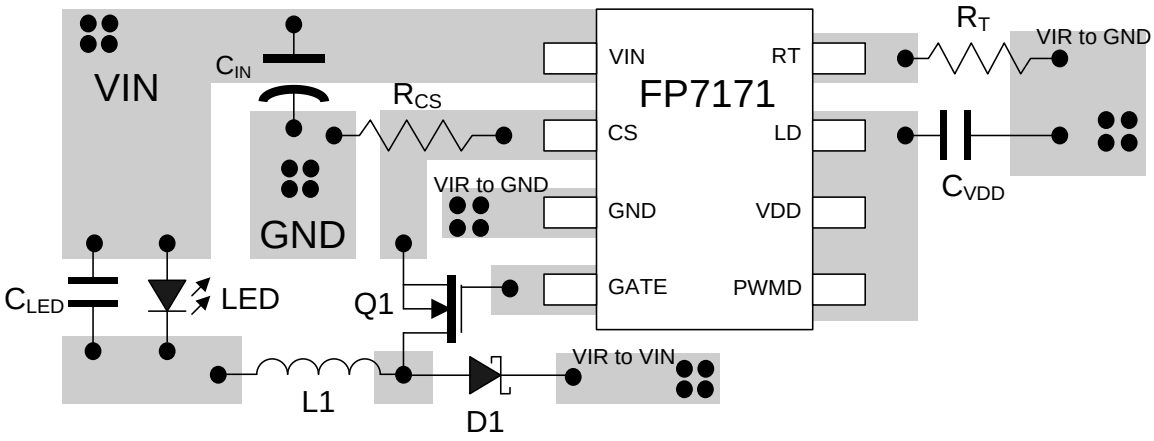
Application Information

The FP7171 is optimized to drive buck LED drivers using open-loop peak current mode control. This method of control enables fairly accurate LED current control without the need for high side current sensing or the design of any closed loop controllers. The IC uses very few external components and enables both Linear and PWM dimming of the LED current.

A resistor connected to the RT pin programs the frequency of operation (or the off-time). The oscillator produces pulses at regular intervals. These pulses set the SR flip-flop in the FP7171 which causes the GATE driver to turn on. The same pulses also start the blanking timer which inhibits the reset input of the SR flip flop and prevent false turn-offs due to the turn-on spike. When the FET turns on, the current through the inductor starts ramping up. This current flows through the external sense resistor R_{CS} and produces a ramp voltage at the CS pin. The comparators are constantly comparing the CS pin voltage to both the voltage at the LD pin and the internal 250mV. Once the blanking timer is complete, the output of these comparators is allowed to reset the flip flop. When the output of either one of the two comparators goes high, the flip flop is reset and the GATE output goes low. The GATE goes low until the SR flip flop is set by the oscillator. Assuming a 30% ripple in the inductor, the current sense resistor R_{CS} can be set using:

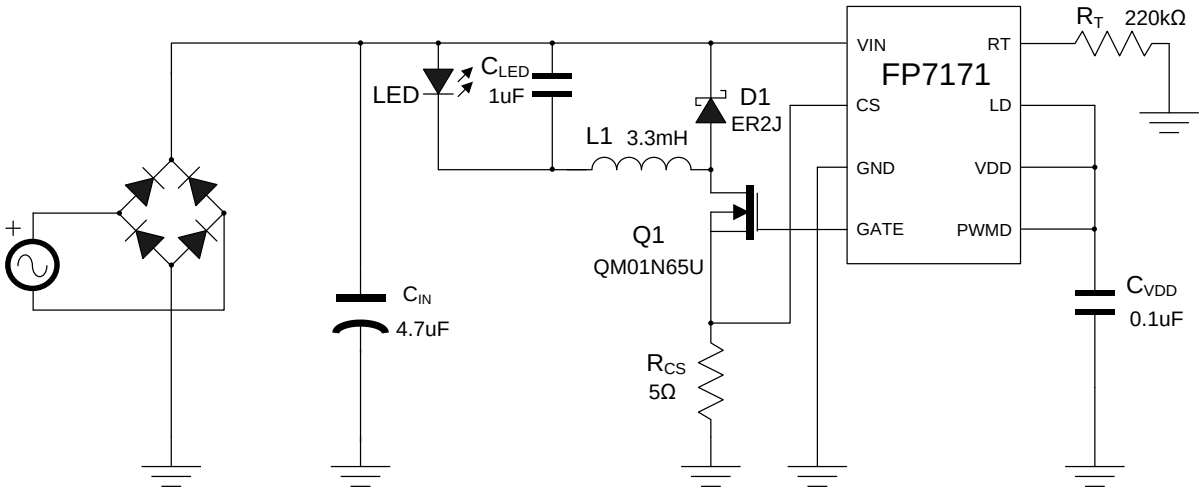
$$R_{CS} = \frac{0.25V(or V_{LD})}{1.15 \quad I_{LED}(A)}$$

Constant frequency peak current mode control has an inherent disadvantage – at duty cycles greater than 0.5, the control scheme goes into subharmonic oscillations. To prevent this, an artificial slope is typically added to the current sense waveform. This slope compensation scheme will affect the accuracy of the LED current in the present form. However, a constant off-time peak current control scheme does not have this problem and can easily operate at duty cycles greater then 0.5 and also gives inherent input voltage rejection making the LED current almost insensitive to input voltage variations. But, it leads to variable frequency operation and the frequency range depends greatly on the input and output voltage variation. FP7171 makes it easy to switch between the two modes of operation by changing one connection (see oscillator section).



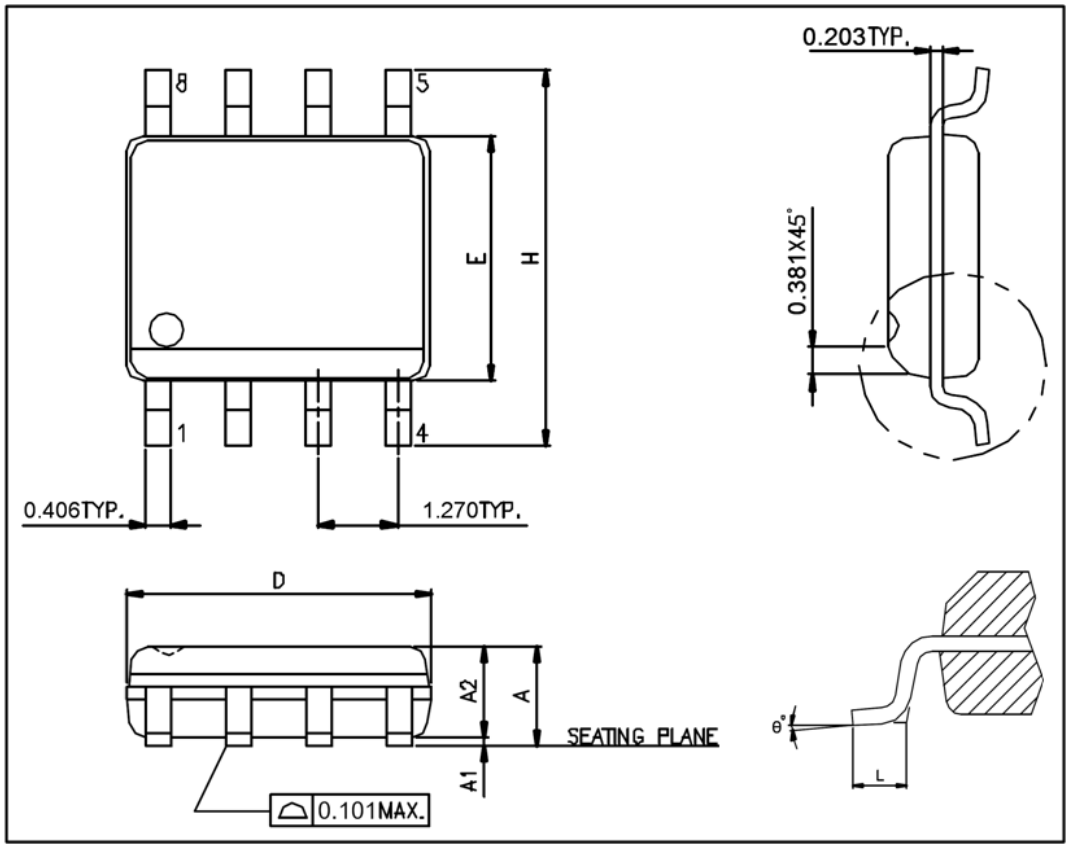
Suggested Layout

Typical Application



Package Outline

SOP-8L



UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.101	0.254
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Note:

1. Package dimensions are in compliance with JEDEC Outline: MS-012 AA.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E” does not include inter-lead flash, or protrusions.