

DRV5053-Q1 汽车类数字锁存霍尔效应传感器

1 特性

- 数字双极锁存霍尔传感器
- 符合汽车类应用的 AEC-Q100 标准
 - 1 级: $T_A = -40$ 至 125°C (Q, 请参见图 23)
 - 0 级: $T_A = -40$ 至 150°C (E, 请参见图 23)
- 出色的温度稳定性
 - 在温度范围内 $B_{OP} \pm 10\%$
- 多种灵敏度选项 (B_{OP}/B_{RP})
 - 1.3/-1.3mT (FA, 请参见图 23)
 - 2.7/-2.7mT (AD, 请参见图 23)
 - 6/-6mT (AG, 请参见图 23)
 - 12/-12mT (BC, 请参见图 23)
- 支持宽电压范围
 - 2.7V 至 38V
 - 无需外部稳压器
- 开漏输出 (30mA 灌电流)
- 35 μs 短暂上电时间
- 小型封装尺寸
 - 表面贴装 3 引脚小外形尺寸晶体管 (SOT)-23 (DBZ)
 - 2.92mm x 2.37mm
 - 插入式 3 引脚 TO-92 (LPG)
 - 4.00mm x 3.15mm
- 保护 特性
 - 反向电源保护 (高达 -22V)
 - 支持高达 40V 抛负载
 - 输出短路保护
 - 输出电流限制
 - 电池输出短路保护

2 应用

- 电动工具
- 流量计
- 阀门和螺线管状态
- 无刷直流电机
- 接近感测
- 转速计

3 说明

DRV5013-Q1 器件是一款斩波稳定霍尔效应传感器，能够在整个温度范围内提供具有出色灵敏度稳定性和集成保护特性的磁场感测 解决方案。

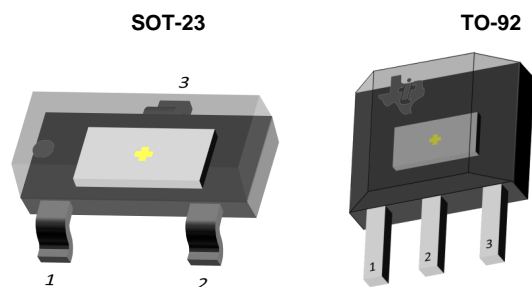
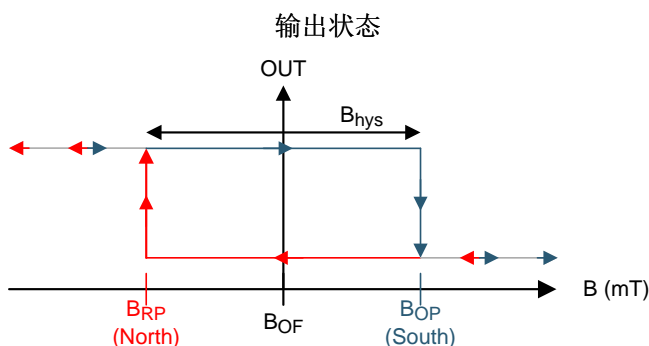
磁场由数字双极锁存输出表示。该集成电路 (IC) 配有一个灌电流能力达 30mA 的漏极开路输出级。反向极性保护高达 -22V 的宽工作电压范围 (2.7 至 38V) 使得此器件广泛适用于各种汽车 简单方法。

提供针对反向电源情况、抛负载和输出短路或者过流的内部保护功能。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
DRV5013-Q1	SOT-23 (3)	2.92mm x 1.30mm
	TO-92 (3)	4.00mm x 3.15mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (May 2016) to Revision D	Page
• Revised preliminary limits for the FA version	5

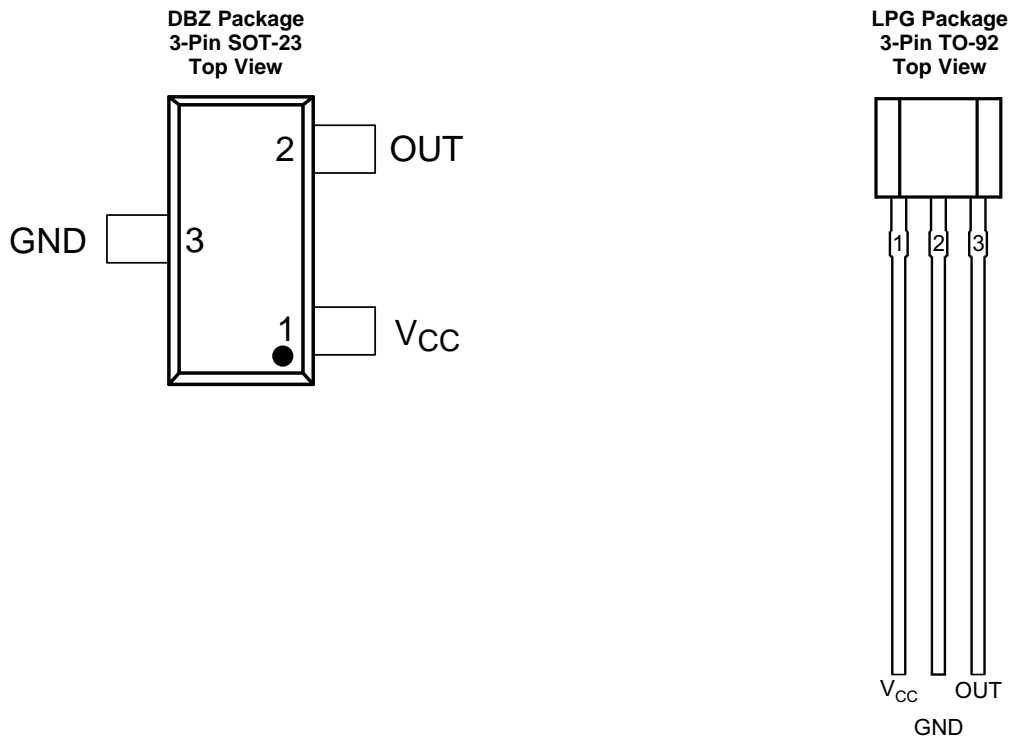
Changes from Revision B (February 2016) to Revision C	Page
• Revised preliminary limits for the FA version	5

Changes from Revision A (December 2015) to Revision B	Page
• 已添加 FA 器件选项	1
• Added the typical bandwidth value to the <i>Magnetic Characteristics</i> table	5

Changes from Original (December 2014) to Revision A	Page
• 已更正 SOT-23 封装体尺寸并将 SIP 封装名称更正为 TO-92	1
• Added B _{MAX} to <i>Absolute Maximum Ratings</i>	4
• Removed table notes regarding testing for the operating junction temperature in <i>Absolute Maximum Ratings</i>	4
• 已更新封装卷带选项 M 和空白	18
• 已添加 社区资源	19

5 Pin Configuration and Functions

For additional configuration information, see [器件标记](#) and [机械、封装和可订购信息](#).



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBZ	LPG		
GND	3	2	GND	Ground pin
OUT	2	3	Output	Hall sensor open-drain output. The open drain requires a resistor pullup.
V _{CC}	1	1	PWR	2.7 to 38 V power supply. Bypass this pin to the GND pin with a 0.01-μF (minimum) ceramic capacitor rated for V _{CC} .

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Power supply voltage	V _{CC}	-22 ⁽²⁾	40	V
	Voltage ramp rate (V _{CC}), V _{CC} < 5 V		Unlimited	
	Voltage ramp rate (V _{CC}), V _{CC} > 5 V		0	2
Output pin voltage		-0.5	40	V
Output pin reverse current during reverse supply condition		0	100	mA
Magnetic flux density, B _{MAX}		Unlimited		
Operating junction temperature, T _J	Q, see 图 23	-40	150	°C
	E, see 图 23	-40	175	
Storage temperature, T _{stg}		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Ensured by design. Only tested to -20 V.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2500	V
	Charged-device model (CDM), per AEC Q100-011	±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V _{CC}	Power supply voltage	2.7	38	V	
V _O	Output pin voltage (OUT)	0	38	V	
I _{SINK}	Output pin current sink (OUT) ⁽¹⁾	0	30	mA	
T _A	Operating ambient temperature	Q, see 图 23	-40	125	°C
		E, see 图 23	-40	150	

- (1) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DRV5013-Q1		UNIT
		DBZ (SOT-23)	LPG (TO-92)	
		3 PINS	3 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	333.2	180	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	99.9	98.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	66.9	154.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	4.9	40	°C/W
ψ _{JB}	Junction-to-board characterization parameter	65.2	154.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_{CC})						
V _{CC}	V _{CC} operating voltage		2.7		38	V
I _{CC}	Operating supply current	V _{CC} = 2.7 to 38 V, T _A = 25°C		2.7		mA
		V _{CC} = 2.7 to 38 V, T _A = T _{A, MAX} ⁽¹⁾		3	3.5	
t _{on}	Power-on time			35	50	μs
OPEN DRAIN OUTPUT (OUT)						
r _{DS(on)}	FET on-resistance	V _{CC} = 3.3 V, I _O = 10 mA, T _A = 25°C		22		Ω
		V _{CC} = 3.3 V, I _O = 10 mA, T _A = 125°C		36	50	
I _{lkg(off)}	Off-state leakage current	Output Hi-Z			1	μA
PROTECTION CIRCUITS						
V _{CCR}	Reverse supply voltage		-22			V
I _{OCP}	Overcurrent protection level	OUT shorted V _{CC}	15	30	45	mA

(1) T_{A, MAX} is 125°C for Q Grade 1 devices and 150°C for E Grade 0 devices (see [Fig 23](#))

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN DRAIN OUTPUT (OUT)						
t _d	Output delay time	B = B _{RP} – 10 mT to B _{OP} + 10 mT in 1 μs		13	25	μs
t _r	Output rise time (10% to 90%)	R1 = 1 kΩ, C _O = 50 pF, V _{CC} = 3.3 V		200		ns
t _f	Output fall time (90% to 10%)	R1 = 1 kΩ, C _O = 50 pF, V _{CC} = 3.3 V		31		ns

6.7 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT ⁽¹⁾
f _{BW}	Bandwidth ⁽²⁾		20	30		kHz
DRV5013FA: 1.3 / –1.3 mT						
B _{OP}	Operate point; see Figure 12		–0.6	1.3	3	mT
B _{RP}	Release point; see Figure 12		–3	–1.3	0.6	mT
B _{hys}	Hysteresis; B _{hys} = (B _{OP} – B _{RP})		1.2	2.6		mT
B _O	Magnetic offset; B _O = (B _{OP} + B _{RP}) / 2		–1.5	0	1.5	mT
DRV5013AD: 2.7 / –2.7 mT						
B _{OP}	Operate point; see Figure 12		1	2.7	5	mT
B _{RP}	Release point; see Figure 12		–5	–2.7	–1	mT
B _{hys}	Hysteresis; B _{hys} = (B _{OP} – B _{RP})			5.4		mT
B _O	Magnetic offset; B _O = (B _{OP} + B _{RP}) / 2		–1.5	0	1.5	mT
DRV5013AG: 6 / –6 mT						
B _{OP}	Operate point; see Figure 12		3	6	9	mT
B _{RP}	Release point; see Figure 12		–9	–6	–3	mT
B _{hys}	Hysteresis; B _{hys} = (B _{OP} – B _{RP})			12		mT
B _O	Magnetic offset; B _O = (B _{OP} + B _{RP}) / 2		–1.5	0	1.5	mT

(1) 1 mT = 10 Gauss

(2) Bandwidth describes the fastest changing magnetic field that can be detected and translated to the output.

Magnetic Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT ⁽¹⁾
DRV5013BC: 12 / -12 mT						
B _{OP}	Operate point; see Figure 12		6	12	18	mT
B _{RP}	Release point; see Figure 12		-18	-12	-6	mT
B _{hys}	Hysteresis; B _{hys} = (B _{OP} - B _{RP})			24		mT
B _O	Magnetic offset; B _O = (B _{OP} + B _{RP}) / 2		-1.5	0	1.5	mT

6.8 Typical Characteristics

T_A > 125°C data is valid for Grade 0 devices only (E, see Figure 23)

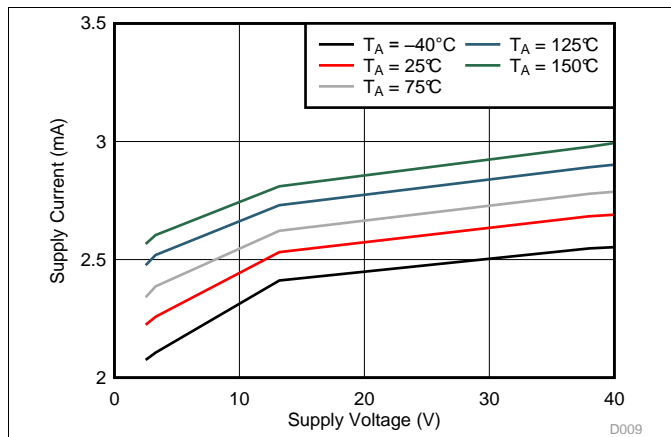


Figure 1. I_{CC} vs V_{CC}

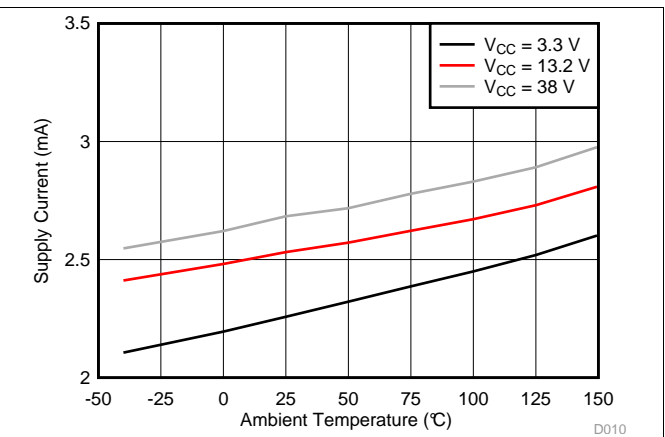


Figure 2. I_{CC} vs Temperature

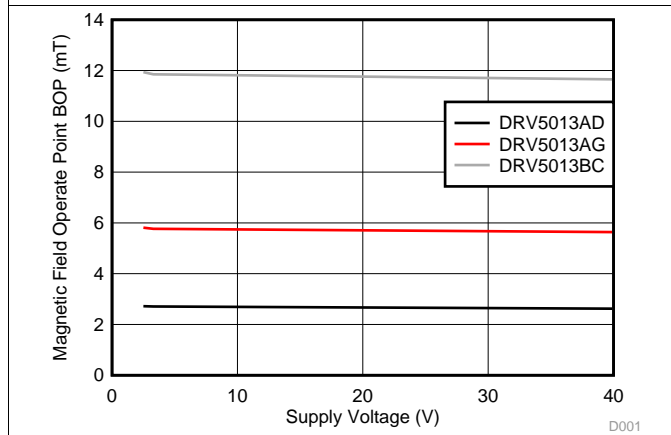


Figure 3. B_{OP} vs V_{CC}

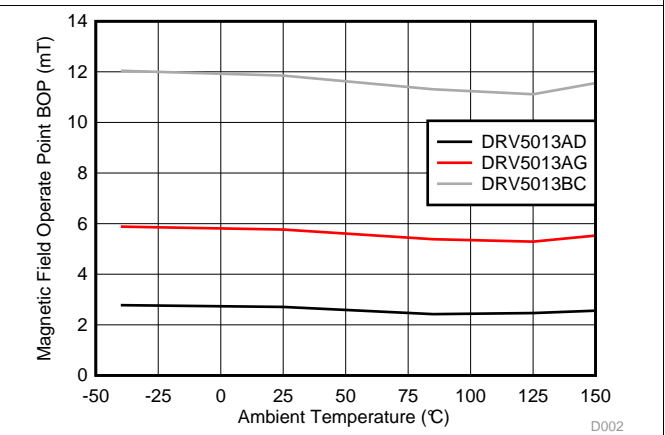
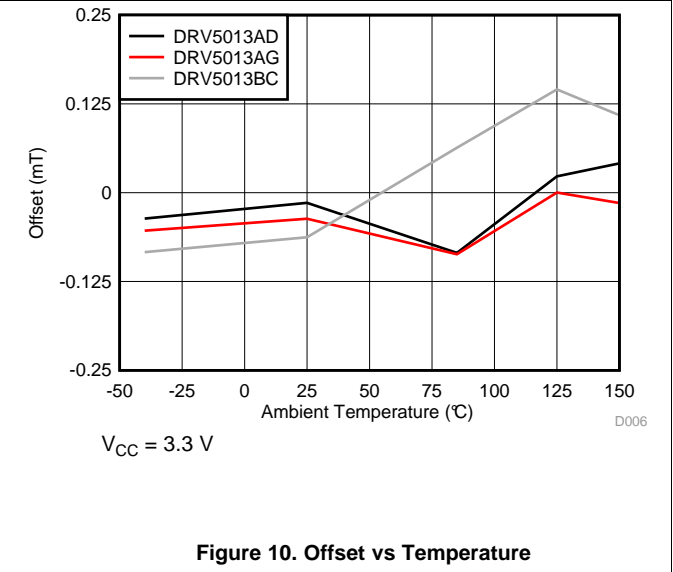
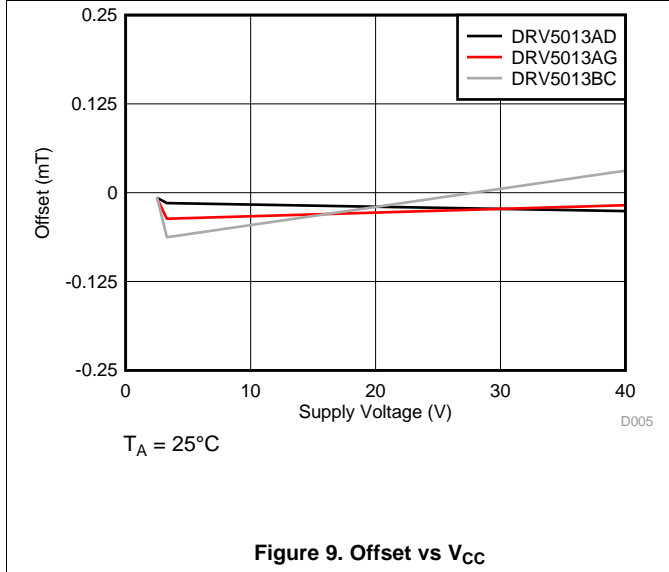
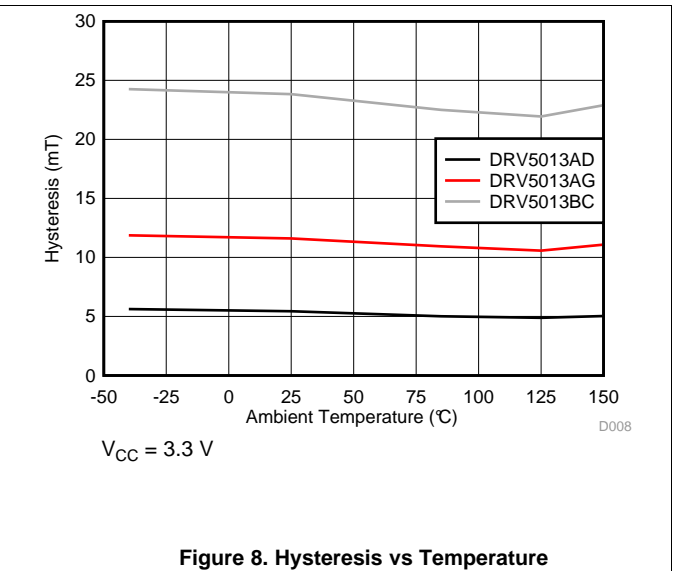
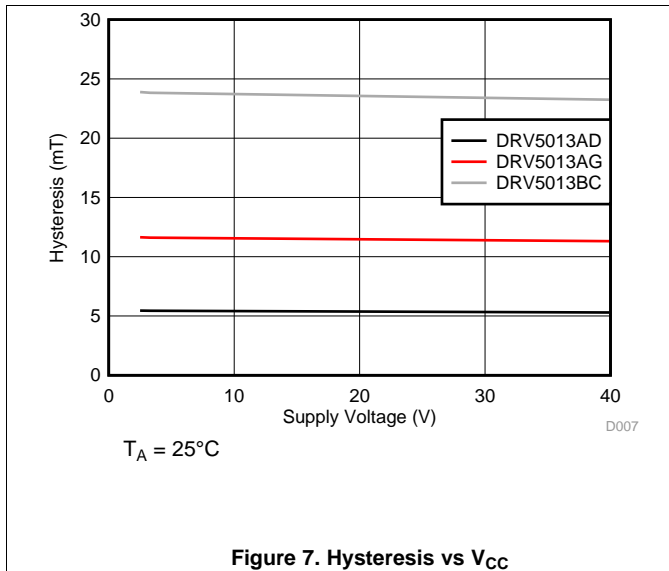
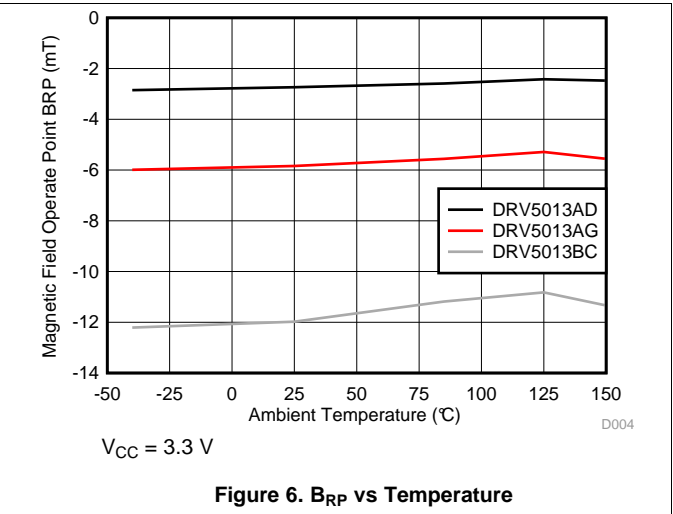
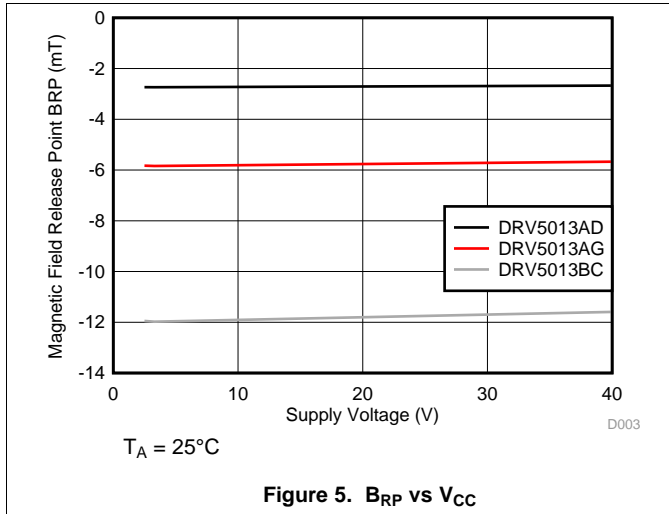


Figure 4. B_{OP} vs Temperature

Typical Characteristics (continued)

T_A > 125°C data is valid for Grade 0 devices only (E, see [Figure 23](#))



7 Detailed Description

7.1 Overview

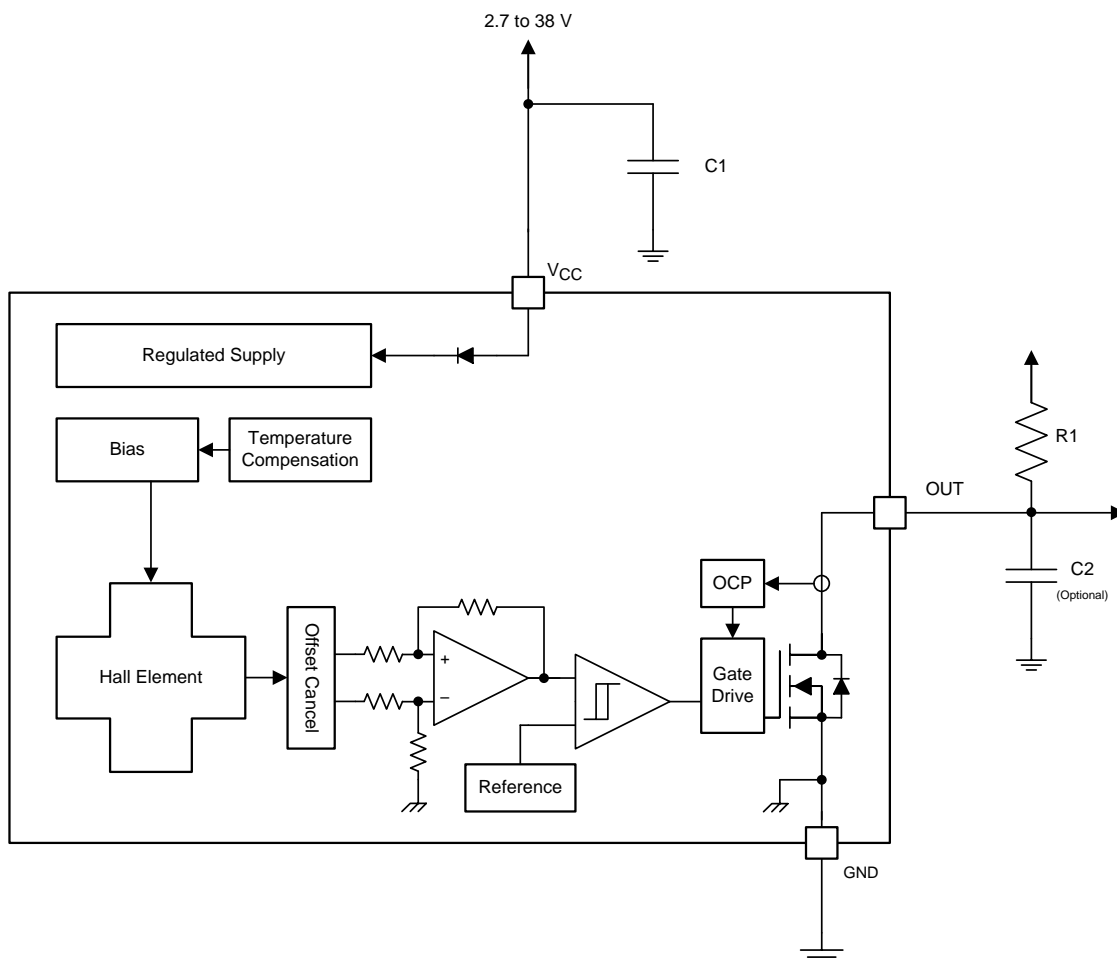
The DRV5013-Q1 device is a chopper-stabilized Hall sensor with a digital latched output for magnetic sensing applications. The DRV5013-Q1 device can be powered with a supply voltage between 2.7 and 38 V, and continuously survives continuous -22-V reverse-battery conditions. The DRV5013-Q1 device does not operate when -22 to 2.4 V is applied to the V_{CC} pin (with respect to the GND pin). In addition, the device can withstand voltages up to 40 V for transient durations.

The field polarity is defined as follows: a **south pole** near the marked side of the package is a positive magnetic field. A **north pole** near the marked side of the package is a negative magnetic field.

The output state is dependent on the magnetic field perpendicular to the package. A **south pole** near the marked side of the package causes the output to pull low (operate point, B_{OP}), and a **north pole** near the marked side of the package causes the output to release (release point, B_{RP}). Hysteresis is included in between the operate point and the release point therefore magnetic-field noise does not accidentally trip the output.

An external pullup resistor is required on the OUT pin. The OUT pin can be pulled up to V_{CC} , or to a different voltage supply. This allows for easier interfacing with controller circuits.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Field Direction Definition

A positive magnetic field is defined as a **south pole** near the marked side of the package as shown in [Figure 11](#).

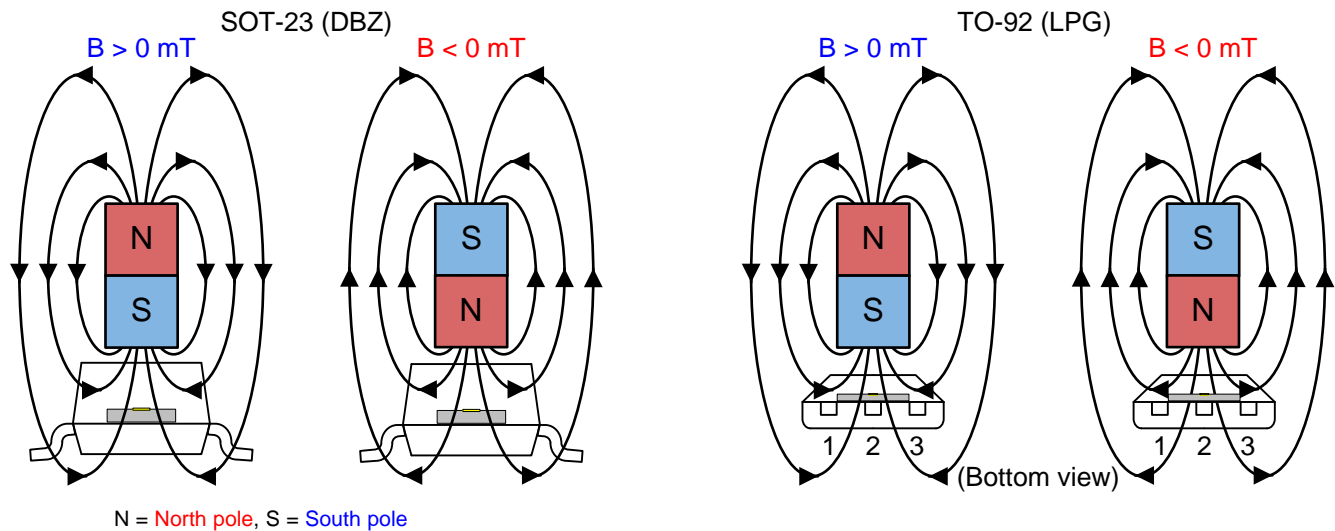


Figure 11. Field Direction Definition

7.3.2 Device Output

If the device is powered on with a magnetic field strength between B_{RP} and B_{OP} , then the device output is indeterminate and can either be Hi-Z or Low. If the field strength is greater than B_{OP} , then the output is pulled low. If the field strength is less than B_{RP} , then the output is released.

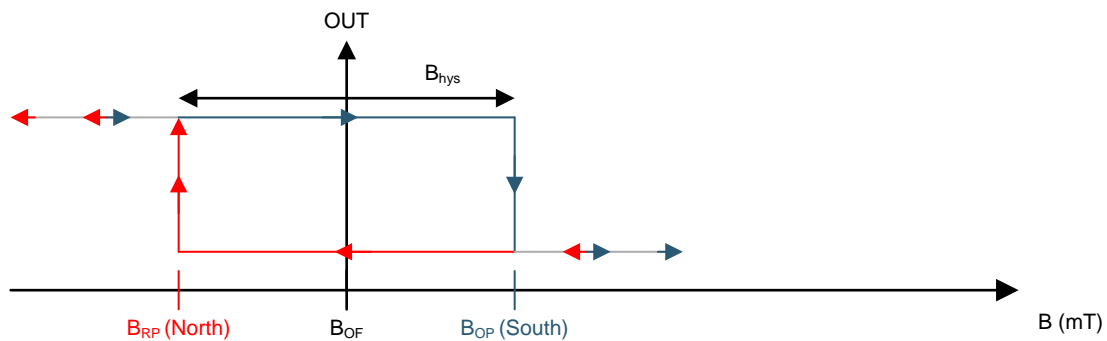


Figure 12. DRV5013-Q1— $B_{OP} > 0$

Feature Description (continued)

7.3.3 Power-On Time

After applying V_{CC} to the DRV5013-Q1 device, t_{on} must elapse before the OUT pin is valid. During the power-up sequence, the output is Hi-Z. A pulse as shown in Figure 13 and Figure 14 occurs at the end of t_{on} . This pulse can allow the host processor to determine when the DRV5013-Q1 output is valid after startup. In Case 1 (Figure 13) and Case 2 (Figure 14), the output is defined assuming a constant magnetic field $B > B_{OP}$ and $B < B_{RP}$.

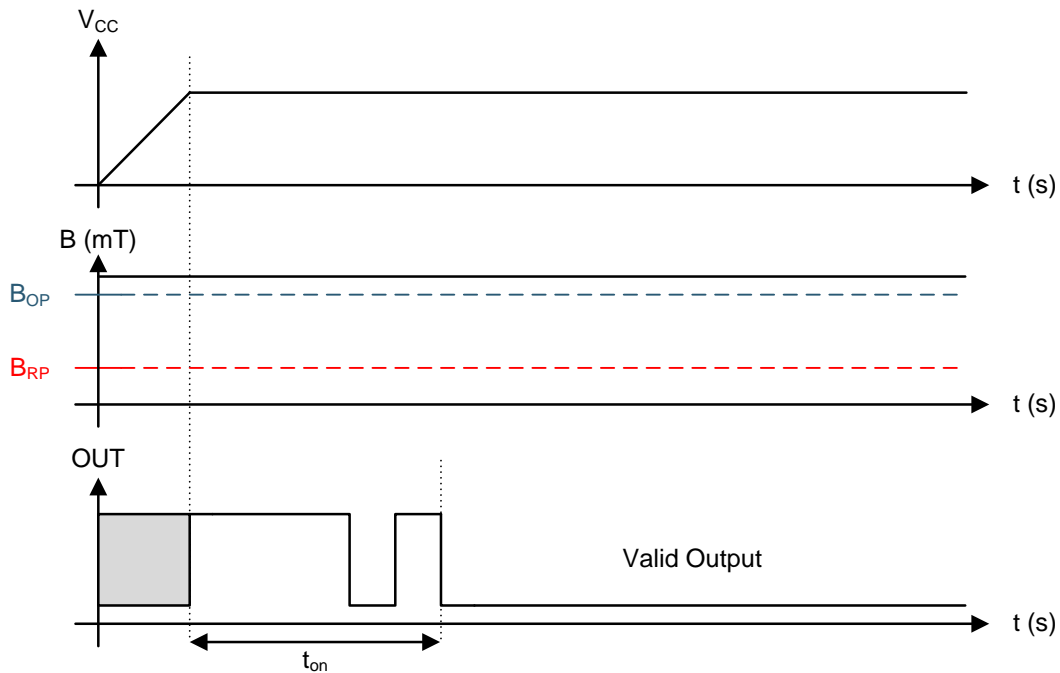


Figure 13. Case 1: Power On When $B > B_{OP}$

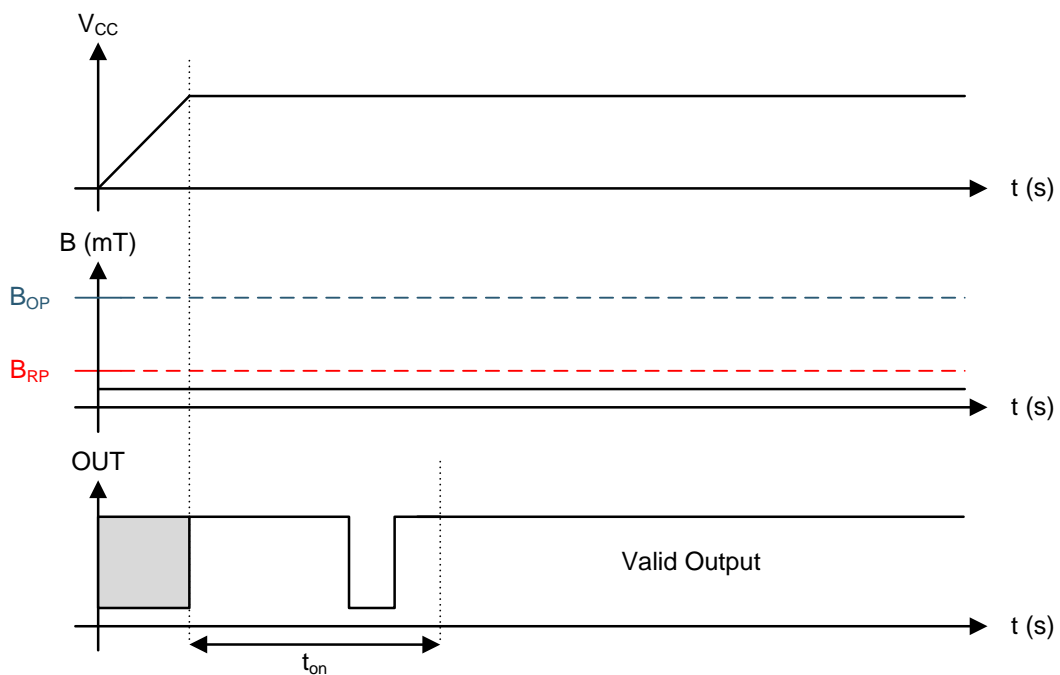


Figure 14. Case 2: Power On When $B < B_{RP}$

Feature Description (continued)

If the device is powered on with the magnetic field strength $B_{RP} < B < B_{OP}$, then the device output is indeterminate and can either be Hi-Z or pulled low. During the power-up sequence, the output is held Hi-Z until t_{on} has elapsed. At the end of t_{on} , a pulse is given on the OUT pin to indicate that t_{on} has elapsed. After t_{on} , if the magnetic field changes such that $B_{OP} < B$, the output is released. Case 3 (Figure 15) and Case 4 (Figure 16) show examples of this behavior.

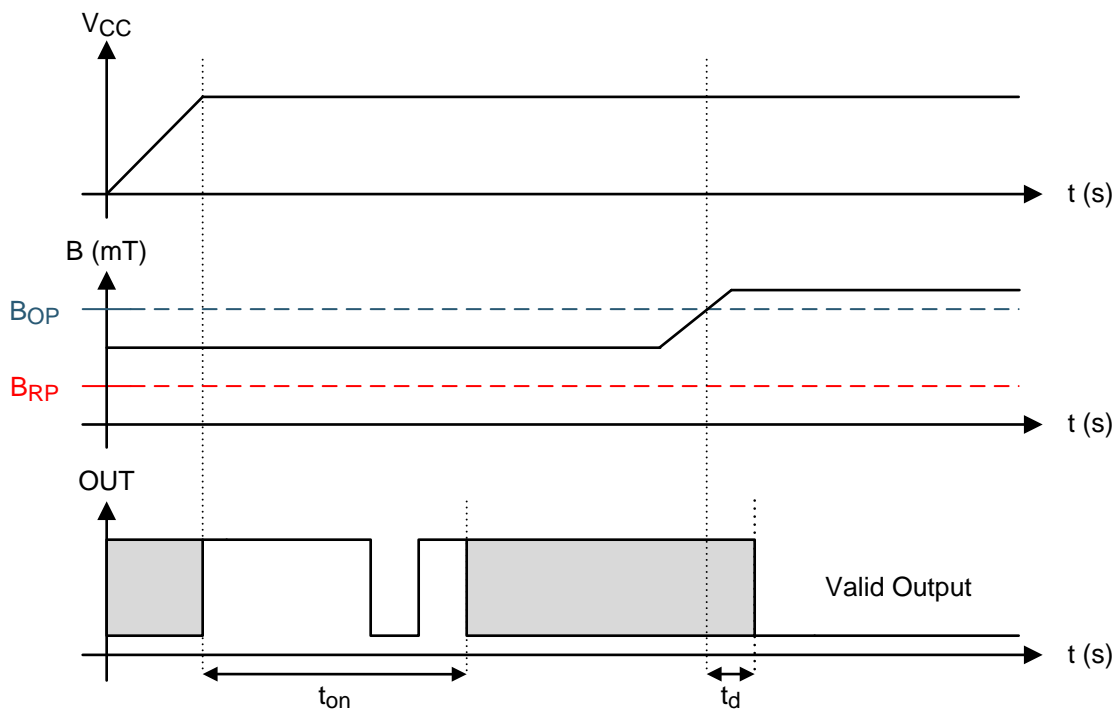


Figure 15. Case 3: Power On When $B_{RP} < B < B_{OP}$, Followed by $B > B_{OP}$

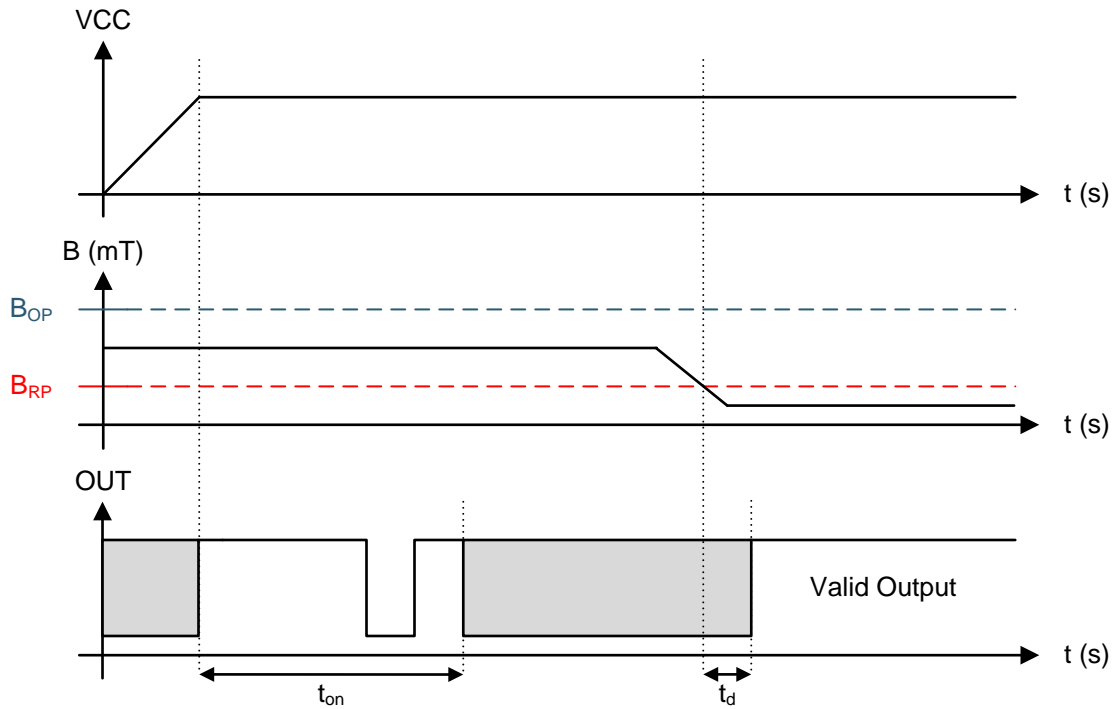
Feature Description (continued)


Figure 16. Case 4: Power On When $B_{RP} < B < B_{OP}$, Followed by $B < B_{RP}$

7.3.4 Output Stage

The DRV5013-Q1 output stage uses an open-drain NMOS, and it is rated to sink up to 30 mA of current. For proper operation, calculate the value of the pullup resistor R1 using [Equation 1](#).

$$\frac{V_{ref \max}}{30 \text{ mA}} \leq R1 \leq \frac{V_{ref \min}}{100 \mu\text{A}} \quad (1)$$

The size of R1 is a tradeoff between the OUT rise time and the current when OUT is pulled low. A lower current is generally better, however faster transitions and bandwidth require a smaller resistor for faster switching.

In addition, ensure that the value of $R1 > 500 \Omega$ to ensure the output driver can pull the OUT pin close to GND.

NOTE

V_{ref} is not restricted to V_{CC} . The allowable voltage range of this pin is specified in the [Absolute Maximum Ratings](#).

Feature Description (continued)

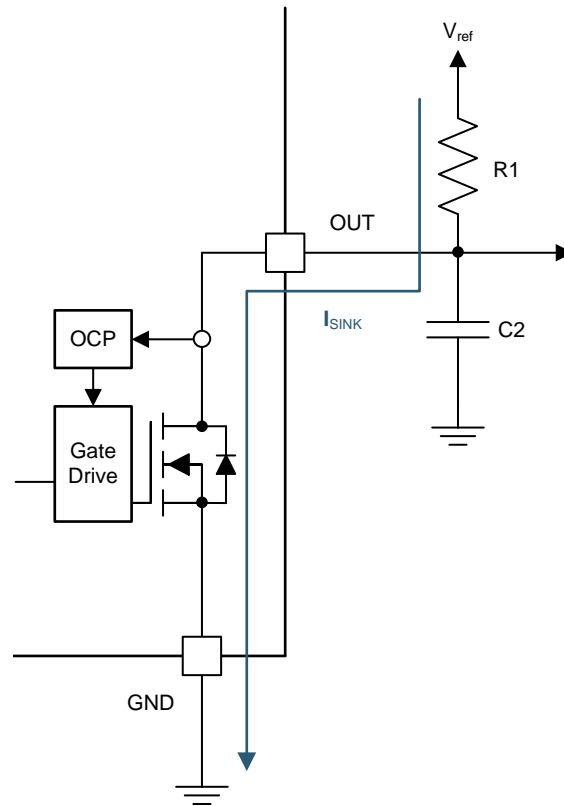


Figure 17.

Select a value for C2 based on the system bandwidth specifications as shown in Equation 2.

$$2 \times f_{BW} \text{ (Hz)} < \frac{1}{2\pi \times R1 \times C2} \quad (2)$$

Most applications do not require this C2 filtering capacitor.

Feature Description (continued)

7.3.5 Protection Circuits

The DRV5013-Q1 device is fully protected against overcurrent and reverse-supply conditions.

7.3.6 Overcurrent Protection (OCP)

An analog current-limit circuit limits the current through the FET. The driver current is clamped to I_{OCP} . During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

7.3.7 Load Dump Protection

The DRV5013-Q1 device operates at DC V_{CC} conditions up to 38 V nominally, and can additionally withstand $V_{CC} = 40$ V. No current-limiting series resistor is required for this protection.

7.3.8 Reverse Supply Protection

The DRV5013-Q1 device is protected in the event that the V_{CC} pin and the GND pin are reversed (up to -22 V).

NOTE

In a reverse supply condition, the OUT pin reverse-current must not exceed the ratings specified in the [Absolute Maximum Ratings](#).

Table 1.

FAULT	CONDITION	DEVICE	DESCRIPTION	RECOVERY
FET overload (OCP)	$I_{SINK} \geq I_{OCP}$	Operating	Output current is clamped to I_{OCP}	$I_O < I_{OCP}$
Load dump	$38\text{ V} < V_{CC} < 40\text{ V}$	Operating	Device will operate for a transient duration	$V_{CC} \leq 38\text{ V}$
Reverse supply	$-22\text{ V} < V_{CC} < 0\text{ V}$	Disabled	Device will survive this condition	$V_{CC} \geq 2.7\text{ V}$

7.4 Device Functional Modes

The DRV5013-Q1 device is active only when V_{CC} is between 2.7 and 38 V.

When a reverse supply condition exists, the device is inactive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV5013-Q1 device is used in magnetic-field sensing applications.

8.2 Typical Applications

8.2.1 Standard Circuit

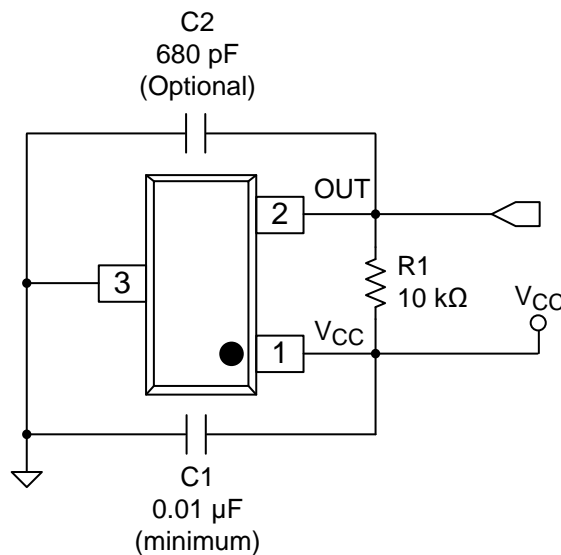


Figure 18. Typical Application Circuit

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	3.2 to 3.4 V
System bandwidth	f_{BW}	10 kHz

8.2.1.2 Detailed Design Procedure

Table 3. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C1	V_{CC}	GND	A 0.01- μ F (minimum) ceramic capacitor rated for V_{CC}
C2	OUT	GND	Optional: Place a ceramic capacitor to GND
R1	OUT	REF ⁽¹⁾	Requires a resistor pullup

(1) REF is not a pin on the DRV5013-Q1 device, but a REF supply-voltage pullup is required for the OUT pin; the OUT pin may be pulled up to V_{CC} .

8.2.1.2.1 Configuration Example

In a 3.3-V system, $3.2\text{ V} \leq V_{\text{ref}} \leq 3.4\text{ V}$. Use Equation 3 to calculate the allowable range for R1.

$$\frac{V_{\text{ref max}}}{30\text{ mA}} \leq R1 \leq \frac{V_{\text{ref min}}}{100\text{ }\mu\text{A}} \tag{3}$$

For this design example, use Equation 4 to calculate the allowable range of R1.

$$\frac{3.4\text{ V}}{30\text{ mA}} \leq R1 \leq \frac{3.2\text{ V}}{100\text{ }\mu\text{A}} \tag{4}$$

Therefore:

$$113\text{ }\Omega \leq R1 \leq 32\text{ k}\Omega \tag{5}$$

After finding the allowable range of R1 (Equation 5), select a value between 500 Ω and 32 k Ω for R1.

Assuming a system bandwidth of 10 kHz, use Equation 6 to calculate the value of C2.

$$2 \times f_{\text{BW}}\text{ (Hz)} < \frac{1}{2\pi \times R1 \times C2} \tag{6}$$

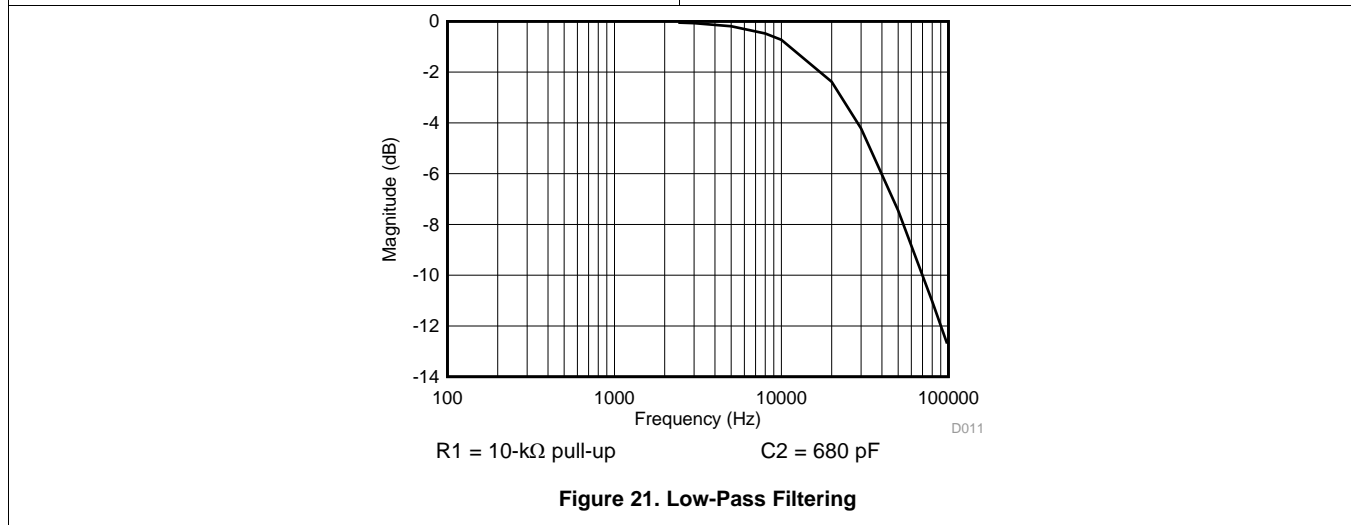
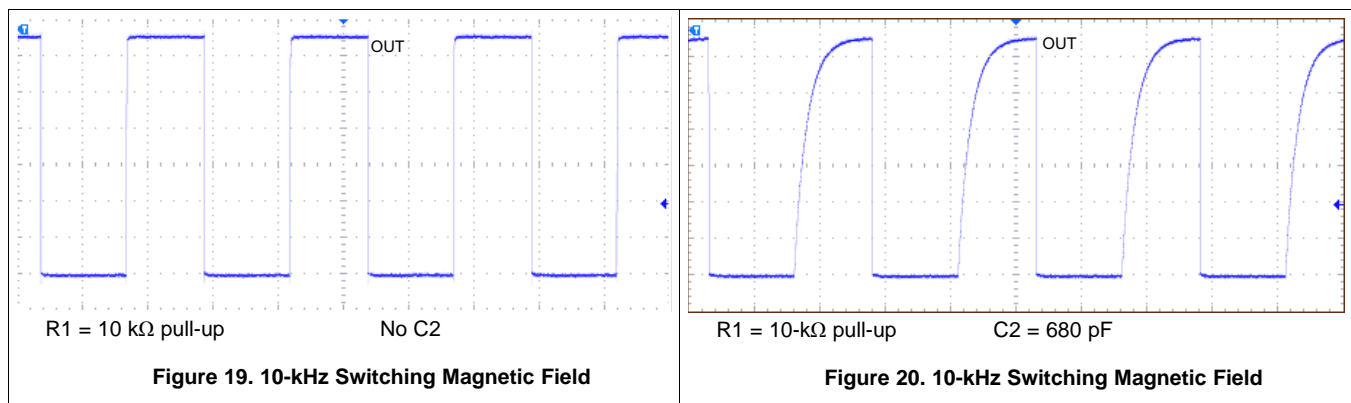
For this design example, use Equation 7 to calculate the value of C2.

$$2 \times 10\text{ kHz} < \frac{1}{2\pi \times R1 \times C2} \tag{7}$$

An R1 value of 10 k Ω and a C2 value less than 820 pF satisfy the requirement for a 10-kHz system bandwidth.

A selection of R1 = 10 k Ω and C2 = 680 pF would cause a low-pass filter with a corner frequency of 23.4 kHz.

8.2.1.3 Application Curves



8.2.2 Alternative Two-Wire Application

For systems that require minimal wire count, the device output can be connected to V_{CC} through a resistor, and the total supplied current can be sensed near the controller.

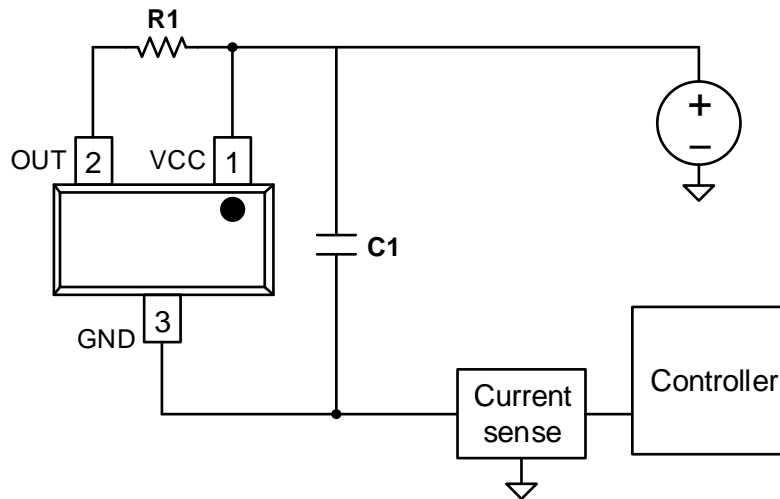


Figure 22. 2-Wire Application

Current can be sensed using a shunt resistor or other circuitry.

8.2.2.1 Design Requirements

Table 4 lists the related design parameters.

Table 4. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	12 V
OUT resistor	R1	1 k Ω
Bypass capacitor	C1	0.1 μ F
Current when $B < B_{RP}$	$I_{RELEASE}$	About 3 mA
Current when $B > B_{OP}$	$I_{OPERATE}$	About 15 mA

8.2.2.2 Detailed Design Procedure

When the open-drain output of the device is high-impedance, current through the path equals the I_{CC} of the device (approximately 3 mA).

When the output pulls low, a parallel current path is added, equal to $V_{CC} / (R1 + r_{DS(on)})$. Using 12 V and 1 k Ω , the parallel current is approximately 12 mA, making the total current approximately 15 mA.

The local bypass capacitor C1 should be at least 0.1 μ F, and a larger value if there is high inductance in the power line interconnect.

9 Power Supply Recommendations

The DRV5013-Q1 device is designed to operate from an input voltage supply (V_M) range between 2.7 and 38 V. A 0.01- μ F (minimum) ceramic capacitor rated for V_{CC} must be placed as close to the DRV5013-Q1 device as possible.

10 器件和文档支持

10.1 器件支持

10.1.1 器件命名规则

图 23 显示了读取 DRV5013-Q1 器件完整器件名称的图例。

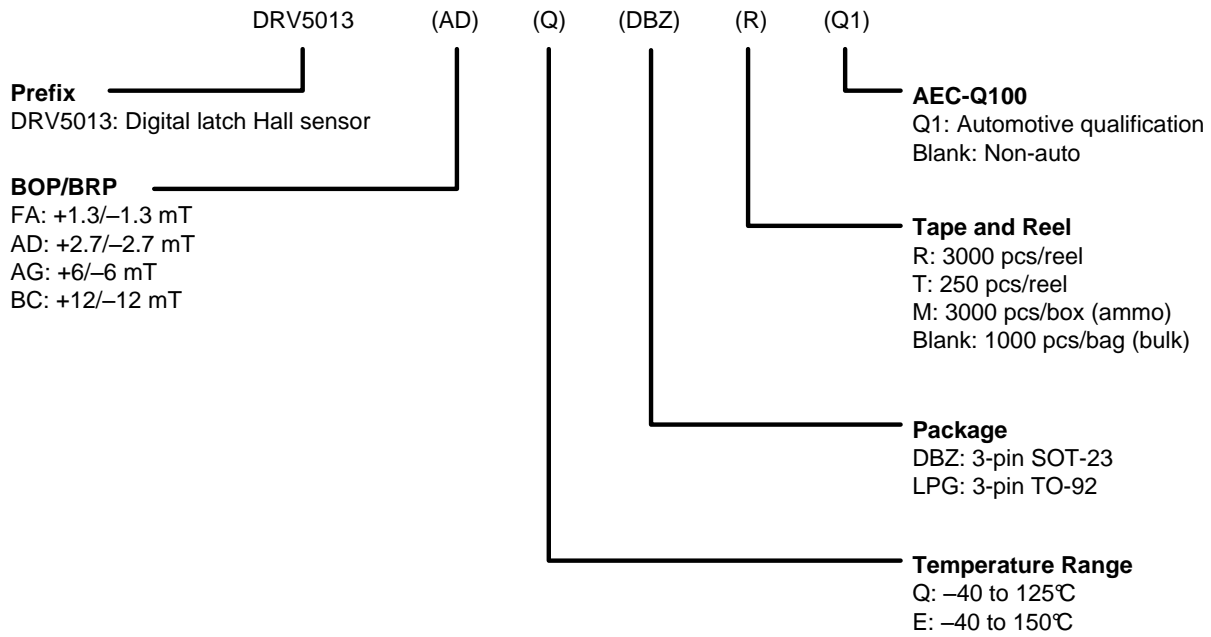


图 23. 器件命名规则

10.1.2 器件标记

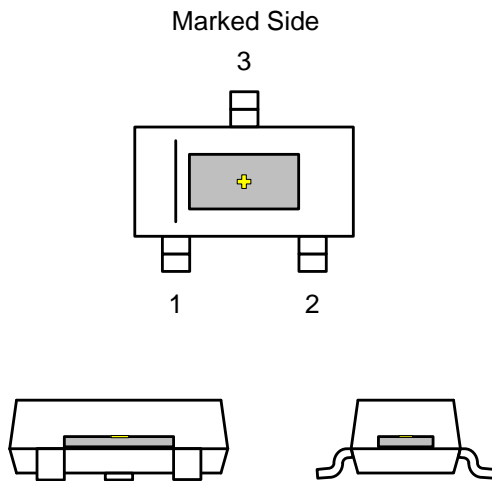


图 24. SOT-23 (DBZ) 封装

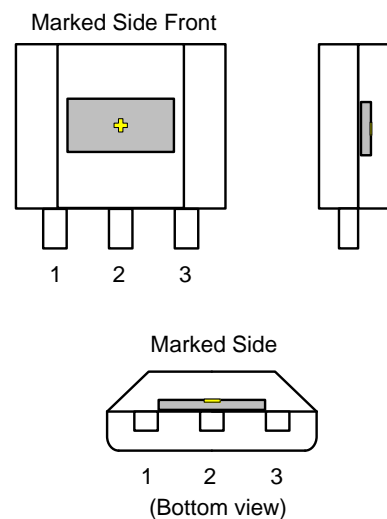


图 25. TO-92 (LPG) 封装

✦ 表示霍尔效应传感器（未按比例显示）。霍尔元件置于封装中央位置，容差为 $\pm 100\mu\text{m}$ 。在 DBZ 封装中，霍尔元件与封装底部的距离为 $0.7\text{mm} \pm 50\mu\text{m}$ ；在 LPG 封装中，霍尔元件与封装底部的距离为 $0.987\text{mm} \pm 50\mu\text{m}$ 。

10.2 接收文档更新通知

要接收文档更新通知，请访问 www.ti.com.cn 您器件对应的产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档的修订历史记录。

10.3 社区资源

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.4 商标

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10.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

10.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5013ADEDDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	+NJAD	Samples
DRV5013ADEDDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	+NJAD	Samples
DRV5013ADELPGMQ1	ACTIVE	TO-92	LPG	3	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 150	+NJAD	Samples
DRV5013ADELPGQ1	ACTIVE	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 150	+NJAD	Samples
DRV5013ADQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NKAD	Samples
DRV5013ADQDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NKAD	Samples
DRV5013ADQLPGMQ1	ACTIVE	TO-92	LPG	3	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	+NKAD	Samples
DRV5013ADQLPGQ1	ACTIVE	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	+NKAD	Samples
DRV5013AGEDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	+NJAG	Samples
DRV5013AGEDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	+NJAG	Samples
DRV5013AGELPGMQ1	ACTIVE	TO-92	LPG	3	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 150	+NJAG	Samples
DRV5013AGELPGQ1	ACTIVE	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 150	+NJAG	Samples
DRV5013AGQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NKAG	Samples
DRV5013AGQDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NKAG	Samples
DRV5013AGQLPGMQ1	ACTIVE	TO-92	LPG	3	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	+NKAG	Samples
DRV5013AGQLPGQ1	ACTIVE	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	+NKAG	Samples
DRV5013BCEDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	+NJBC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5013BCEDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	+NJBC	Samples
DRV5013BCELPGMQ1	ACTIVE	TO-92	LPG	3	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 150	+NJBC	Samples
DRV5013BCELPGQ1	ACTIVE	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 150	+NJBC	Samples
DRV5013BCQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NKBC	Samples
DRV5013BCQDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NKBC	Samples
DRV5013BCQLPGMQ1	ACTIVE	TO-92	LPG	3	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	+NKBC	Samples
DRV5013BCQLPGQ1	ACTIVE	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	+NKBC	Samples
DRV5013FAEDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	+NJFA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF DRV5013-Q1 :

- Catalog: [DRV5013](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



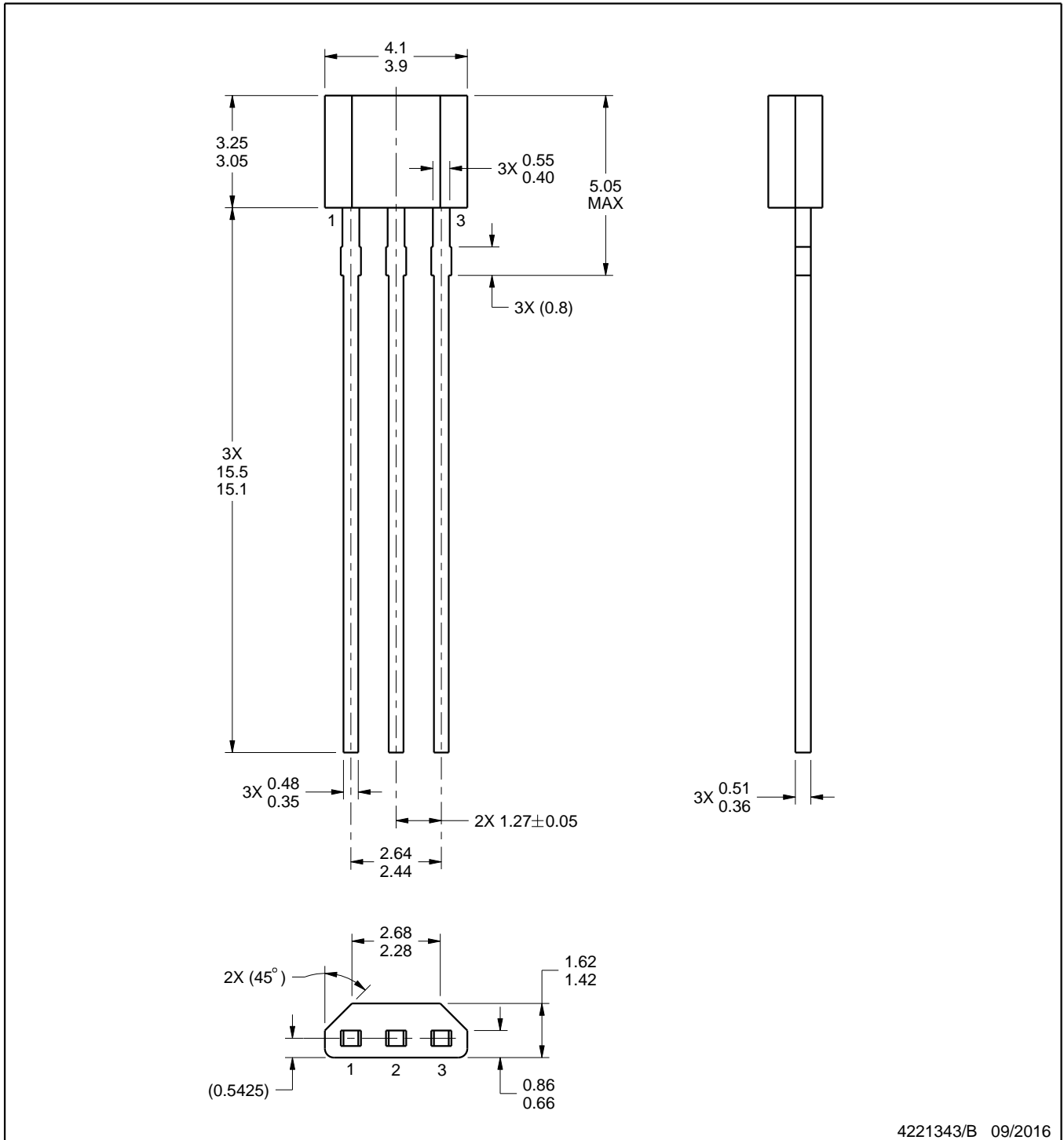
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5013ADEDDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013ADEDDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013ADQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013ADQDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013AGEDDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013AGEDDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013AGQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013AGQDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013BCEDDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013BCEDDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013BCQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013BCQDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5013FAEDDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5013ADEDDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013ADEDDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5013ADQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013ADQDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5013AGEDDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013AGEDDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5013AGQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013AGQDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5013BCEDDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013BCEDDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5013BCQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5013BCQDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5013FAEDDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0



4221343/B 09/2016

NOTES:

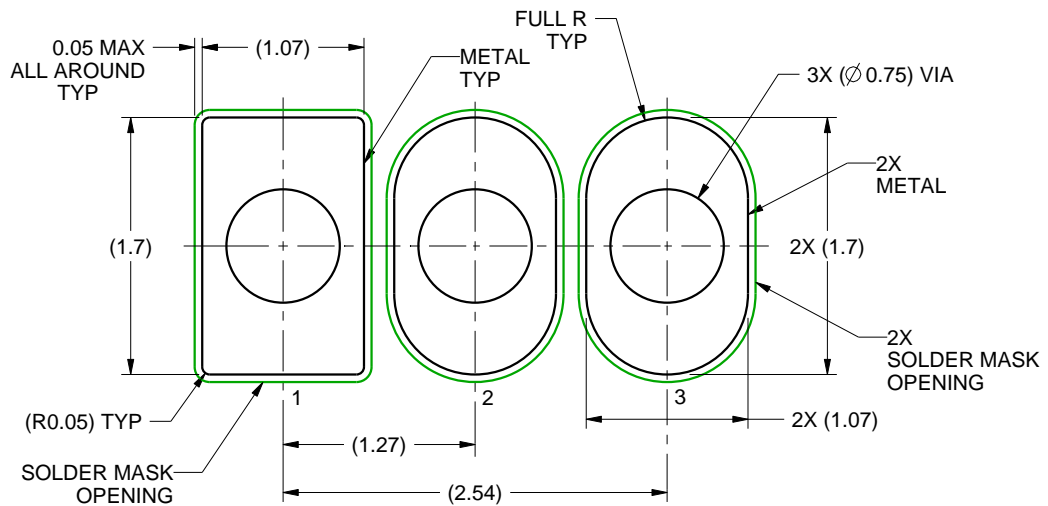
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

LPG0003A

TO-92 - 5.05 mm max height

TO-92



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

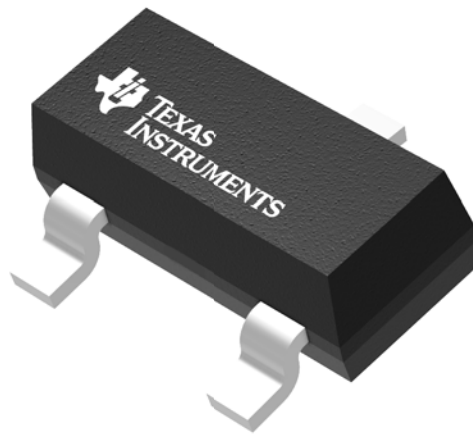
4221343/B 09/2016

GENERIC PACKAGE VIEW

DBZ 3

SOT-23 - 1.12 mm max height

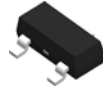
SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203227/C

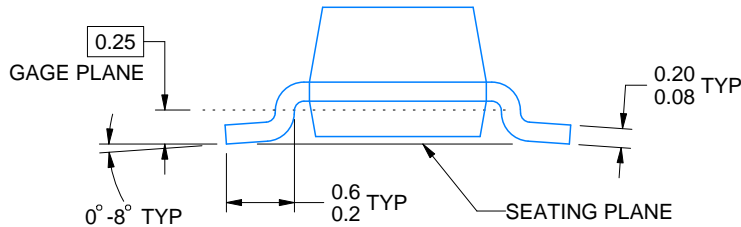
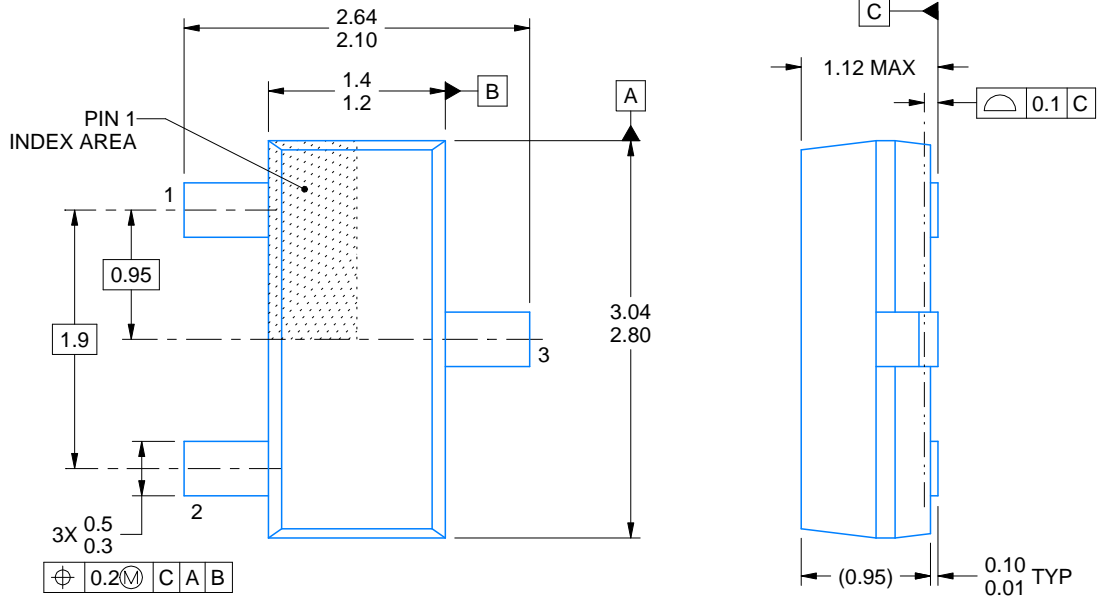
DBZ0003A



PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



4214838/C 04/2017

NOTES:

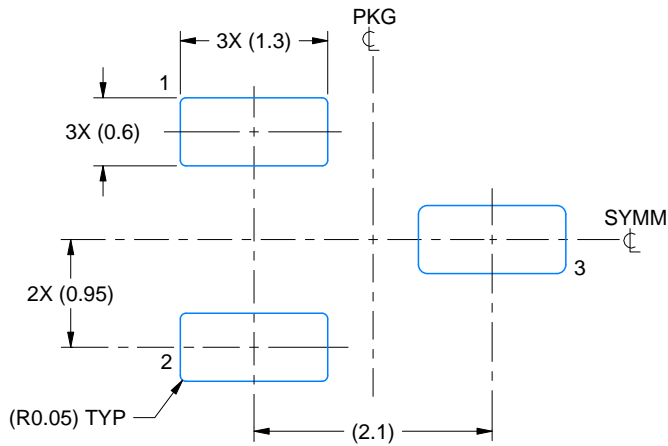
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.

EXAMPLE BOARD LAYOUT

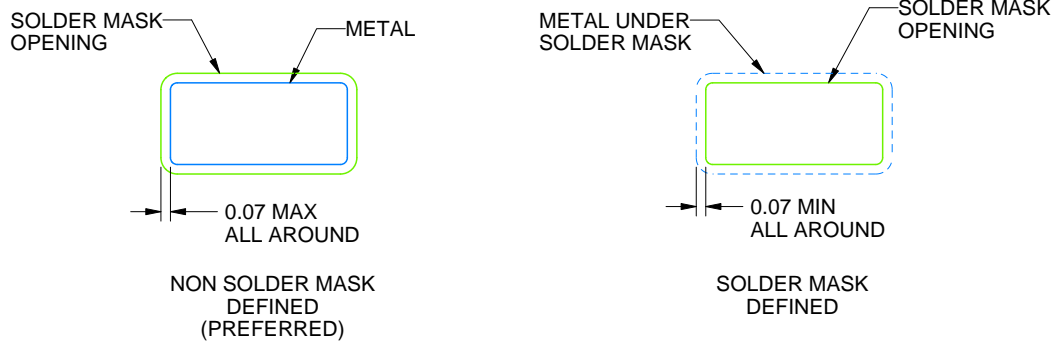
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

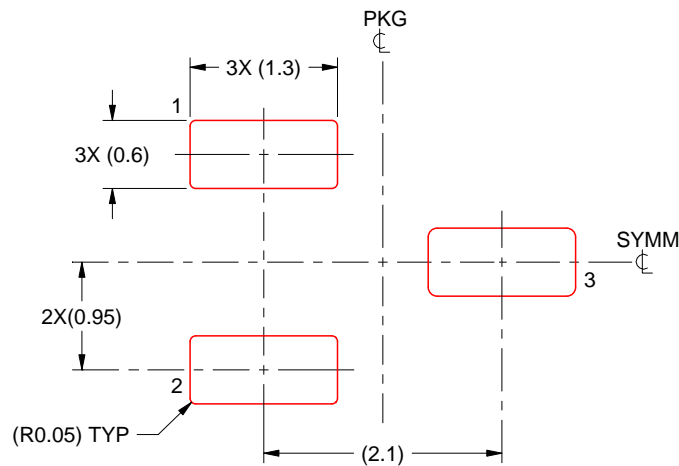
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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