# CC2630 SimpleLink™ 6LoWPAN、ZigBee® 无线 MCU

## 1 器件概述

### 1.1 特性

- 微控制器
  - 强大的 ARM® Cortex®-M3
  - EEMBC CoreMark®评分：142
  - 高达 48MHz 的时钟速度
  - 128KB 系统内可编程闪存
  - ROM 中的 TI-RTOS 和 蓝牙®软件
  - 高达 28KB 系统 SRAM，其中 20KB 为超低泄漏静态随机存取存储器 (SRAM)
  - 8KB SRAM，适用于缓存或系统 RAM 使用
  - 2 引脚 cJTAG 和 JTAG 调试
  - 支持无线升级 (OTA)
- 超低功耗传感器控制器
  - 可独立于系统其余部分自主运行
  - 16 位架构
  - 2KB 超低泄漏代码和数据 SRAM
- 高效代码尺寸架构，只读存储器 (ROM) 中装载驱动程序、IEEE 802.15.4 MAC、 和引导加载程序
- 封装符合 RoHS 标准
  - 4mm × 4mm RSM VQFN32 封装（10 个 GPIO）
  - 5mm × 5mm RHB VQFN32 封装（15 个 GPIO）
  - 7mm × 7mm RGZ VQFN48 封装（31 个 GPIO）
- 外设
  - 所有数字外设引脚均可连接任意 GPIO
  - 四个通用定时器模块（8 × 16 位或 4 × 32 位，均采用脉宽调制 (PWM)）
  - 12 位模数转换器 (ADC)、200MSPS、8 通道模拟多路复用器
  - 持续时间比较器
  - 超低功耗模拟比较器
  - 可编程电流源
  - UART
  - 2 个同步串行接口 (SSI)（SPI、MICROWIRE 和 TI）
  - I2C
  - I2S
  - 实时时钟 (RTC)
  - AES-128 安全模块
  - 真随机数发生器 (TRNG)
  - 10、15 或 31 个 GPIO，具体取决于所用封装选项
  - 支持八个电容感测按钮
  - 集成温度传感器
- 外部系统
  - 片上内部 DC-DC 转换器

  - 极少的外部组件
  - 无缝集成 SimpleLink™CC2590 和 CC2592 范围扩展器
  - 与采用 4mm × 4mm 和 5mm × 5mm VQFN 封装的 SimpleLink CC13xx 引脚兼容
- 低功耗
  - 宽电源电压范围
    - 正常工作电压：1.8V 至 3.8V
    - 外部稳压器模式：1.7V 至 1.95V
  - 有源模式 RX：5.9mA
  - 有源模式 TX (0dBm)：6.1mA
  - 有源模式 TX (+5dBm)：9.1mA
  - 有源模式 MCU：61µA/MHz
  - 有源模式 MCU：48.5 CoreMark/mA
  - 有源模式传感器控制器：0.4mA + 8.2µA/MHz
  - 待机电流：1.1µA（RTC 运行，RAM/CPU 保持）
  - 关断电流：100nA（发生外部事件时唤醒）
- 射频 (RF) 部分
  - 2.4GHz RF 收发器，符合 IEEE 802.15.4 PHY 和 MAC
  - 出色的接收器灵敏度(–100dBm)、可选择性和阻断性能
  - 105dB 的链路预算
  - 最高达 +5dBm 的可编程输出功率
  - 单端或差分 RF 接口
  - 适用于符合各项全球射频规范的系统
    - ETSI EN 300 328（欧洲）
    - EN 300 440 2 类（欧洲）
    - FCC CFR47 第 15 部分（美国）
    - ARIB STD-T66（日本）
- 工具和开发环境
  - 功能全面的低成本开发套件
  - 针对不同 RF 配置的多种参考设计
  - 数据包监听器 PC 软件
  - Sensor Controller Studio
  - SmartRF™Studio
  - SmartRF Flash Programmer2
  - IAR Embedded Workbench®（用于 ARM）
  - Code Composer Studio™
  - CCS Cloud


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## 1.2 应用

- 家庭和楼宇自动化
- 照明控制
- 警报和安全
- 电子货架标签
- Proximity Tag
- 无线传感器网络
- 能量采集、无电池传感器和传动器
- 智能电网

## 1.3 说明

CC2630 器件是一款无线微控制器 (MCU)，主要适用于 ZigBee®和 6LoWPAN 应用。

此器件属于 SimpleLink™ CC26xx 系列中的经济高效型超低功耗 2.4GHz RF 器件。它具有极低的有源 RF 和 MCU 电流以及低功耗模式流耗，可确保卓越的电池使用寿命，适合小型纽扣电池供电以及在能源采集型应用中 使用。

SimpleLink Bluetooth 低功耗 CC2630 器件含有一个 32 位 ARM® Cortex®-M3 内核（与主处理器工作频率同为 48MHz），并且具有丰富的外设功能集，其中包括一个独特的超低功耗传感器控制器。此传感器控制器非常适合连接外部传感器，还适合用于在系统其余部分处于睡眠模式的情况下自主收集模拟和数字数据。因此，CC2630 器件成为 ZigBee 和 6LoWPAN 网络中电池供电和能量采集终端节点的理想选择。

CC2630 无线 MCU 的电源和时钟管理以及无线系统需要采用特定配置并由软件处理才能正确运行，这已在 TI-RTOS 中实现。TI 建议将此软件框架应用于针对器件的全部应用程序开发过程。完整的 TI-RTOS 和器件驱动程序以源代码形式免费提供，下载地址：www.ti.com。

IEEE 802.15.4 MAC 嵌入在 ROM 中，并在 ARM® Cortex®-M0 处理器上单独运行。此架构可改善整体系统性能和功耗，并释放闪存以供应用。

ZigBee 协议栈可从 www.ti.com.cn 免费获取。

器件信息(1)

| 产品型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| CC2630F128RGZ | VQFN (48) | 7.00mm x 7.00mm |
| CC2630F128RHB | VQFN (32) | 5.00mm x 5.00mm |
| CC2630F128RSM | VQFN (32) | 4.00mm x 4.00mm |

(1) 详细信息请参见 节 9。

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## 1.4 功能框图

图 1-1给出了 CC2630 器件的框图。

中的功能框图

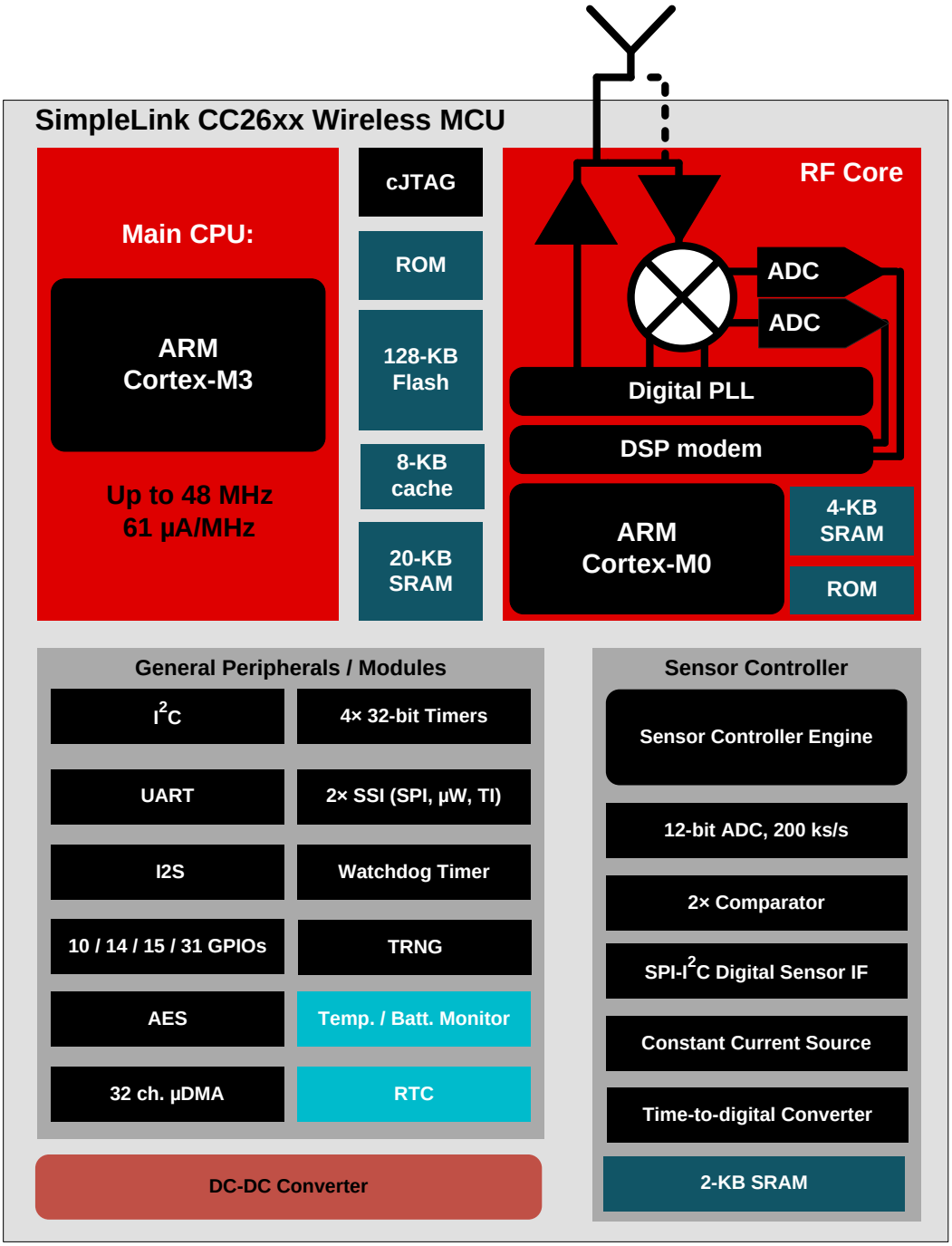


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图 **1-1.** 方框图


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## 2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from October 15, 2015 to July 5, 2016** **Page**

- 已添加 分离 VDDS 电源轨特性 ..... 1
- 已添加 2Mbps *Bluetooth* 低功耗 ..... 1
- Added option for up to 80-Ω ESR when $C_L$ is 6 pF or lower ..... 18
- Added motional inductance recommendation to the *24-MHz XOSC* table ..... 18
- Added tolerance for RCOSC_LF and RTC accuracy content ..... 19
- Updated the Soc ADC internal voltage reference specification in Section 5.12 ..... 19
- Moved all SSI parameters to Section 5.18 ..... 21
- Added SPI timing parameters ..... 21
- Added VOH and VOL min and max values for 4-mA and 8-mA load ..... 23
- Added min and max values for VIH and VIL ..... 24
- Added 0-dBm setting to the *TX Current Consumption vs Supply Voltage (VDDS)* graph ..... 26
- Changed Figure 5-11, *Receive Mode Current vs Supply Voltage (VDDS)* ..... 26
- Added Figure 5-20, *Supply Current vs Temperature* ..... 27
- Added application circuit schematics and layout for 5XD and 4XS ..... 37

**Changes from February 21, 2015 to October 15, 2015** **Page**

- Removed RHB package option from CC2620 ..... 7
- Added motional inductance recommendation to the *24-MHz XOSC* table ..... 18
- Added SPI timing parameters ..... 21
- Added VOH and VOL min and max values for 4-mA and 8-mA load ..... 23
- Added min and max values for VIH and VIL ..... 24
- Added *IEEE 802.15.4 Sensitivity vs Channel Frequency* ..... 26
- Added *RF Output Power vs Channel Frequency* ..... 26
- Added Figure 5-11, *Receive Mode Current vs Supply Voltage (VDDS)* ..... 26
- Changed Figure 5-19, *SoC ADC ENOB vs Sampling Frequency (Input Frequency = FS / 10)* ..... 27
- Clarified Brown Out Detector status and functionality in the *Power Modes* table. ..... 34
- Added application circuit schematics and layout for 5XD and 4XS ..... 37


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# 3 Device Comparison

**Table 3-1. Device Family Overview**

| Device | PHY Support | Flash (KB) | RAM (KB) | GPIO | Package(1) |
|---|---|---|---|---|---|
| CC2640F128xxx | Bluetooth low energy (Normal) | 128 | 20 | 31, 15, 10 | RGZ, RHB, RSM |
| CC2650F128xxx | Multi-Protocol(2) | 128 | 20 | 31, 15, 10 | RGZ, RHB, RSM |
| CC2630F128xxx | IEEE 802.15.4 Zigbee(/6LoWPAN) | 128 | 20 | 31, 15, 10 | RGZ, RHB, RSM |
| CC2620F128xxx | IEEE 802.15.4 (RF4CE) | 128 | 20 | 31, 10 | RGZ, RSM |

(1) Package designator replaces the xxx in device name to form a complete device name, RGZ is 7-mm × 7-mm VQFN48, RHB is 5-mm × 5-mm VQFN32, RSM is 4-mm × 4-mm VQFN32, and YFV is 2.7-mm × 2.7-mm DSBGA.
(2) The CC2650 device supports all PHYs and can be reflashed to run all the supported standards.

## 3.1 Related Products

**Wireless Connectivity**

The wireless connectivity portfolio offers a wide selection of low-power RF solutions suitable for a broad range of applications. The offerings range from fully customized solutions to turn key offerings with pre-certified hardware and software (protocol).

**Sub-1 GHz**

Long-range, low-power wireless connectivity solutions are offered in a wide range of Sub-1 GHz ISM bands.

**Companion Products**

Review products that are frequently purchased or used in conjunction with this product.

**SimpleLink™ CC2650 Wireless MCU LaunchPad™ Kit**

The CC2650 LaunchPad™ development kit brings easy Bluetooth® low energy connectivity to the LaunchPad kit ecosystem with the SimpleLink ultra-low power CC26xx family of devices. This LaunchPad kit also supports development for multi-protocol support for the SimpleLink multi-standard CC2650 wireless MCU and the rest of CC26xx family of products: CC2630 wireless MCU for ZigBee®/6LoWPAN and CC2640 wireless MCU for Bluetooth low energy.

**Reference Designs for CC2630**

TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

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# 4 Terminal Configuration and Functions

## 4.1 Pin Diagram – RGZ Package

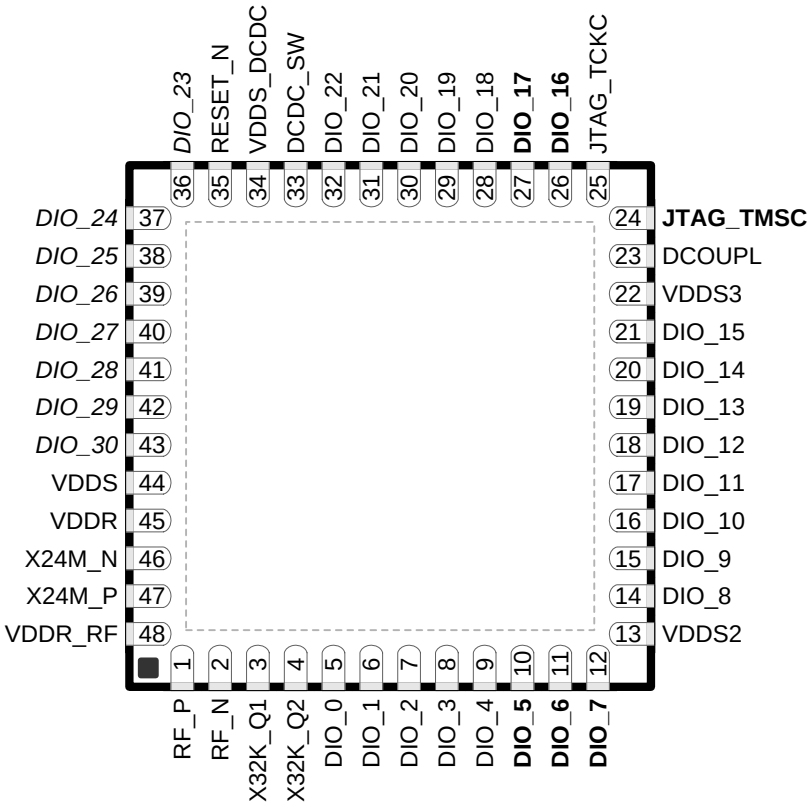


**Figure 4-1. RGZ Package**
**48-Pin VQFN**
**(7-mm × 7-mm) Pinout, 0.5-mm Pitch**

I/O pins marked in Figure 4-1 in **bold** have high-drive capabilities; they are the following:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 24, JTAG_TMSC
- Pin 26, DIO_16
- Pin 27, DIO_17

I/O pins marked in Figure 4-1 in *italics* have analog capabilities; they are the following:

- Pin 36, DIO_23
- Pin 37, DIO_24
- Pin 38, DIO_25
- Pin 39, DIO_26
- Pin 40, DIO_27
- Pin 41, DIO_28
- Pin 42, DIO_29
- Pin 43, DIO_30


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## 4.2 Signal Descriptions – RGZ Package

**Table 4-1. Signal Descriptions – RGZ Package**

| NAME | NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| DCDC_SW | 33 | Power | Output from internal DC-DC(1) |
| DCOUPL | 23 | Power | 1.27-V regulated digital-supply decoupling capacitor(2) |
| DIO_0 | 5 | Digital I/O | GPIO, Sensor Controller |
| DIO_1 | 6 | Digital I/O | GPIO, Sensor Controller |
| DIO_2 | 7 | Digital I/O | GPIO, Sensor Controller |
| DIO_3 | 8 | Digital I/O | GPIO, Sensor Controller |
| DIO_4 | 9 | Digital I/O | GPIO, Sensor Controller |
| DIO_5 | 10 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_6 | 11 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_7 | 12 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_8 | 14 | Digital I/O | GPIO |
| DIO_9 | 15 | Digital I/O | GPIO |
| DIO_10 | 16 | Digital I/O | GPIO |
| DIO_11 | 17 | Digital I/O | GPIO |
| DIO_12 | 18 | Digital I/O | GPIO |
| DIO_13 | 19 | Digital I/O | GPIO |
| DIO_14 | 20 | Digital I/O | GPIO |
| DIO_15 | 21 | Digital I/O | GPIO |
| DIO_16 | 26 | Digital I/O | GPIO, JTAG_TDO, high-drive capability |
| DIO_17 | 27 | Digital I/O | GPIO, JTAG_TDI, high-drive capability |
| DIO_18 | 28 | Digital I/O | GPIO |
| DIO_19 | 29 | Digital I/O | GPIO |
| DIO_20 | 30 | Digital I/O | GPIO |
| DIO_21 | 31 | Digital I/O | GPIO |
| DIO_22 | 32 | Digital I/O | GPIO |
| DIO_23 | 36 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_24 | 37 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_25 | 38 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_26 | 39 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_27 | 40 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_28 | 41 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_29 | 42 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_30 | 43 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| JTAG_TMSC | 24 | Digital I/O | JTAG TMSC, high-drive capability |
| JTAG_TCKC | 25 | Digital I/O | JTAG TCKC |
| RESET_N | 35 | Digital input | Reset, active-low. No internal pullup. |
| RF_P | 1 | RF I/O | Positive RF input signal to LNA during RX<br>Positive RF output signal to PA during TX |
| RF_N | 2 | RF I/O | Negative RF input signal to LNA during RX<br>Negative RF output signal to PA during TX |
| VDDR | 45 | Power | 1.7-V to 1.95-V supply, typically connect to output of internal DC-DC(2)(3) |
| VDDR_RF | 48 | Power | 1.7-V to 1.95-V supply, typically connect to output of internal DC-DC(2)(4) |
| VDDS | 44 | Power | 1.8-V to 3.8-V main chip supply(1) |

(1) For more details, see the technical reference manual (listed in 节 8.3).
(2) Do not supply external circuitry from this pin.
(3) If internal DC-DC is not used, this pin is supplied internally from the main LDO.
(4) If internal DC-DC is not used, this pin must be connected to VDDR for supply from the main LDO.

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**Table 4-1. Signal Descriptions – RGZ Package (continued)**

| NAME | NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| VDDS2 | 13 | Power | 1.8-V to 3.8-V DIO supply(1) |
| VDDS3 | 22 | Power | 1.8-V to 3.8-V DIO supply(1) |
| VDDS_DCDC | 34 | Power | 1.8-V to 3.8-V DC-DC supply |
| X32K_Q1 | 3 | Analog I/O | 32-kHz crystal oscillator pin 1 |
| X32K_Q2 | 4 | Analog I/O | 32-kHz crystal oscillator pin 2 |
| X24M_N | 46 | Analog I/O | 24-MHz crystal oscillator pin 1 |
| X24M_P | 47 | Analog I/O | 24-MHz crystal oscillator pin 2 |
| EGP | | Power | Ground – Exposed Ground Pad |


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## 4.3 Pin Diagram – RHB Package

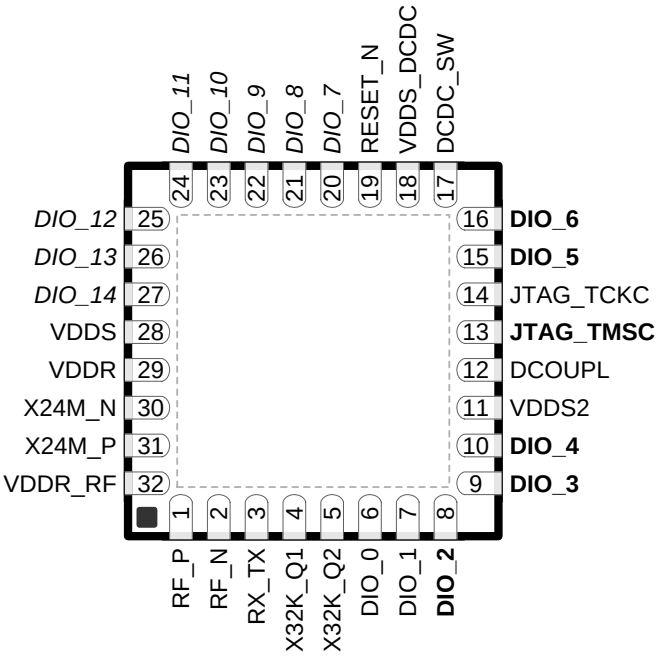


**Figure 4-2. RHB Package**
**32-Pin VQFN**
**(5-mm × 5-mm) Pinout, 0.5-mm Pitch**

I/O pins marked in Figure 4-2 in **bold** have high-drive capabilities; they are the following:

- Pin 8, DIO_2
- Pin 9, DIO_3
- Pin 10, DIO_4
- Pin 13, JTAG_TMSC
- Pin 15, DIO_5
- Pin 16, DIO_6

I/O pins marked in Figure 4-2 in *italics* have analog capabilities; they are the following:

- Pin 20, DIO_7
- Pin 21, DIO_8
- Pin 22, DIO_9
- Pin 23, DIO_10
- Pin 24, DIO_11
- Pin 25, DIO_12
- Pin 26, DIO_13
- Pin 27, DIO_14

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## 4.4 Signal Descriptions – RHB Package

**Table 4-2. Signal Descriptions – RHB Package**

| NAME | NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| DCDC_SW | 17 | Power | Output from internal DC-DC (1) |
| DCOUPL | 12 | Power | 1.27-V regulated digital-supply decoupling (2) |
| DIO_0 | 6 | Digital I/O | GPIO, Sensor Controller |
| DIO_1 | 7 | Digital I/O | GPIO, Sensor Controller |
| DIO_2 | 8 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_3 | 9 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_4 | 10 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_5 | 15 | Digital I/O | GPIO, High drive capability, JTAG_TDO |
| DIO_6 | 16 | Digital I/O | GPIO, High drive capability, JTAG_TDI |
| DIO_7 | 20 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_8 | 21 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_9 | 22 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_10 | 23 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_11 | 24 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_12 | 25 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_13 | 26 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_14 | 27 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| JTAG_TMSC | 13 | Digital I/O | JTAG TMSC, high-drive capability |
| JTAG_TCKC | 14 | Digital I/O | JTAG TCKC |
| RESET_N | 19 | Digital input | Reset, active-low. No internal pullup. |
| RF_N | 2 | RF I/O | Negative RF input signal to LNA during RX<br>Negative RF output signal to PA during TX |
| RF_P | 1 | RF I/O | Positive RF input signal to LNA during RX<br>Positive RF output signal to PA during TX |
| RX_TX | 3 | RF I/O | Optional bias pin for the RF LNA |
| VDDR | 29 | Power | 1.7-V to 1.95-V supply, typically connect to output of internal DC-DC (3) (2) |
| VDDR_RF | 32 | Power | 1.7-V to 1.95-V supply, typically connect to output of internal DC-DC (2) (4) |
| VDDS | 28 | Power | 1.8-V to 3.8-V main chip supply (1) |
| VDDS2 | 11 | Power | 1.8-V to 3.8-V GPIO supply (1) |
| VDDS_DCDC | 18 | Power | 1.8-V to 3.8-V DC-DC supply |
| X32K_Q1 | 4 | Analog I/O | 32-kHz crystal oscillator pin 1 |
| X32K_Q2 | 5 | Analog I/O | 32-kHz crystal oscillator pin 2 |
| X24M_N | 30 | Analog I/O | 24-MHz crystal oscillator pin 1 |
| X24M_P | 31 | Analog I/O | 24-MHz crystal oscillator pin 2 |
| EGP | | Power | Ground – Exposed Ground Pad |

(1) See technical reference manual (listed in 节 8.3) for more details.
(2) Do not supply external circuitry from this pin.
(3) If internal DC-DC is not used, this pin is supplied internally from the main LDO.
(4) If internal DC-DC is not used, this pin must be connected to VDDR for supply from the main LDO.


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## 4.5 Pin Diagram – RSM Package

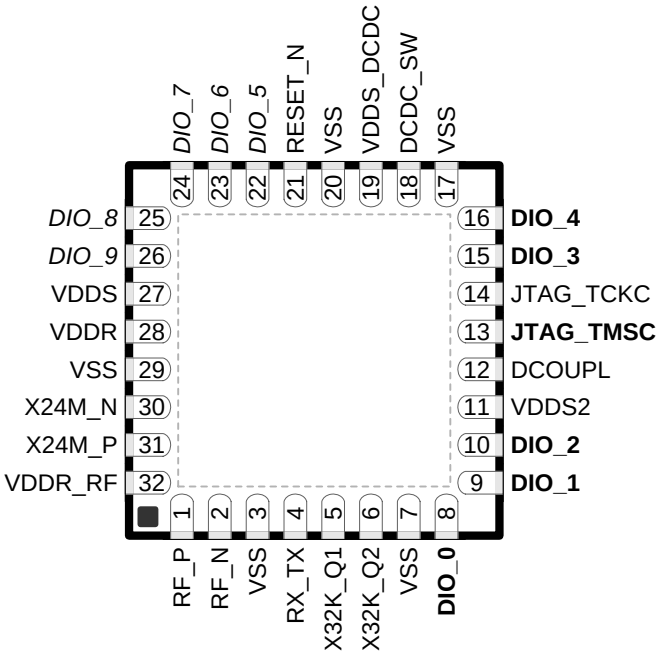


**Figure 4-3. RSM Package**
**32-Pin VQFN**
**(4-mm × 4-mm) Pinout, 0.4-mm Pitch**

I/O pins marked in Figure 4-3 in **bold** have high-drive capabilities; they are as follows:

- Pin 8, DIO_0
- Pin 9, DIO_1
- Pin 10, DIO_2
- Pin 13, JTAG_TMSC
- Pin 15, DIO_3
- Pin 16, DIO_4

I/O pins marked in Figure 4-3 in *italics* have analog capabilities; they are as follows:

- Pin 22, DIO_5
- Pin 23, DIO_6
- Pin 24, DIO_7
- Pin 25, DIO_8
- Pin 26, DIO_9

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## 4.6 Signal Descriptions – RSM Package

**Table 4-3. Signal Descriptions – RSM Package**

| NAME | NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| DCDC_SW | 18 | Power | Output from internal DC-DC.(1). Tie to ground for external regulator mode (1.7-V to 1.95-V operation) |
| DCOUPL | 12 | Power | 1.27-V regulated digital-supply decoupling capacitor(2) |
| DIO_0 | 8 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_1 | 9 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_2 | 10 | Digital I/O | GPIO, Sensor Controller, high-drive capability |
| DIO_3 | 15 | Digital I/O | GPIO, High-drive capability, JTAG_TDO |
| DIO_4 | 16 | Digital I/O | GPIO, High-drive capability, JTAG_TDI |
| DIO_5 | 22 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_6 | 23 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_7 | 24 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_8 | 25 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| DIO_9 | 26 | Digital/Analog I/O | GPIO, Sensor Controller, Analog |
| JTAG_TMSC | 13 | Digital I/O | JTAG TMSC |
| JTAG_TCKC | 14 | Digital I/O | JTAG TCKC |
| RESET_N | 21 | Digital Input | Reset, active-low. No internal pullup. |
| RF_N | 2 | RF I/O | Negative RF input signal to LNA during RX<br>Negative RF output signal to PA during TX |
| RF_P | 1 | RF I/O | Positive RF input signal to LNA during RX<br>Positive RF output signal to PA during TX |
| RX_TX | 4 | RF I/O | Optional bias pin for the RF LNA |
| VDDR | 28 | Power | 1.7-V to 1.95-V supply, typically connect to output of internal DC-DC.(2)(3) |
| VDDR_RF | 32 | Power | 1.7-V to 1.95-V supply, typically connect to output of internal DC-DC(2)(4) |
| VDDS | 27 | Power | 1.8-V to 3.8-V main chip supply(1) |
| VDDS2 | 11 | Power | 1.8-V to 3.8-V GPIO supply(1) |
| VDDS_DCDC | 19 | Power | 1.8-V to 3.8-V DC-DC supply. Tie to ground for external regulator mode (1.7-V to 1.95-V operation). |
| VSS | 3, 7, 17, 20, 29 | Power | Ground |
| X32K_Q1 | 5 | Analog I/O | 32-kHz crystal oscillator pin 1 |
| X32K_Q2 | 6 | Analog I/O | 32-kHz crystal oscillator pin 2 |
| X24M_N | 30 | Analog I/O | 24-MHz crystal oscillator pin 1 |
| X24M_P | 31 | Analog I/O | 24-MHz crystal oscillator pin 2 |
| EGP | | Power | Ground – Exposed Ground Pad |

(1) See technical reference manual (listed in 节 8.3) for more details.
(2) Do not supply external circuitry from this pin.
(3) If internal DC-DC is not used, this pin is supplied internally from the main LDO.
(4) If internal DC-DC is not used, this pin must be connected to VDDR for supply from the main LDO.


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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage (VDDS, VDDS2, and VDDS3) | VDDR supplied by internal DC-DC regulator or internal GLDO. VDDS_DCDC connected to VDDS on PCB. | –0.3 | 4.1 | V |
| Supply voltage (VDDS(3) and VDDR) | External regulator mode (VDDS and VDDR pins connected on PCB) | –0.3 | 2.25 | V |
| Voltage on any digital pin(4)(5) | | –0.3 | VDDSx + 0.3, max 4.1 | V |
| Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X24M_N and X24M_P | | –0.3 | VDDR + 0.3, max 2.25 | V |
| Voltage on ADC input ($V_{in}$) | Voltage scaling enabled | –0.3 | VDDS | V |
| | Voltage scaling disabled, internal reference | –0.3 | 1.49 | |
| | Voltage scaling disabled, VDDS as reference | –0.3 | VDDS / 2.9 | |
| Input RF level | | | 5 | dBm |
| $T_{stg}$ | Storage temperature | –40 | 150 | °C |

(1) All voltage values are with respect to ground, unless otherwise noted.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) In external regulator mode, VDDS2 and VDDS3 must be at the same potential as VDDS.
(4) Including analog-capable DIO.
(5) Each pin is referenced to a specific VDDSx (VDDS, VDDS2 or VDDS3). For a pin-to-VDDS mapping table, see Table 6-3.

## 5.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1) | All pins | ±2500 | V |
| | | Charged device model (CDM), per JESD22-C101(2) | RF pins | ±750 | |
| | | | Non-RF pins | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Ambient temperature | | | –40 | 85 | °C |
| Operating supply voltage (VDDS and VDDR), external regulator mode | For operation in 1.8-V systems (VDDS and VDDR pins connected on PCB, internal DC-DC cannot be used) | | 1.7 | 1.95 | V |
| Operating supply voltage VDDS | For operation in battery-powered and 3.3-V systems (internal DC-DC can be used to minimize power consumption) | | 1.8 | 3.8 | V |
| Operating supply voltages VDDS2 and VDDS3 | | VDDS < 2.7 V | 1.8 | 3.8 | V |
| Operating supply voltages VDDS2 and VDDS3 | | VDDS ≥ 2.7 V | 1.9 | 3.8 | V |

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## 5.4 Power Consumption Summary

Measured on the TI CC2650EM-5XD reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V with internal DC-DC converter, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{core}$ | Core current consumption | Reset. RESET_N pin asserted or VDDS below Power-on-Reset threshold | | 100 | | nA |
| | | Shutdown. No clocks running, no retention | | 150 | | |
| | | Standby. With RTC, CPU, RAM and (partial) register retention. RCOSC_LF | | 1.1 | | µA |
| | | Standby. With RTC, CPU, RAM and (partial) register retention. XOSC_LF | | 1.3 | | |
| | | Standby. With Cache, RTC, CPU, RAM and (partial) register retention. RCOSC_LF | | 2.8 | | |
| | | Standby. With Cache, RTC, CPU, RAM and (partial) register retention. XOSC_LF | | 3.0 | | |
| | | Idle. Supply Systems and RAM powered. | | 550 | | |
| | | Active. Core running CoreMark | | 1.45 mA + 31 µA/MHz | | |
| | | Radio RX (1) | | 5.9 | | mA |
| | | Radio RX (2) | | 6.1 | | |
| | | Radio TX, 0-dBm output power (1) | | 6.1 | | |
| | | Radio TX, 5-dBm output power (2) | | 9.1 | | |
| **Peripheral Current Consumption (Adds to core current $I_{core}$ for each peripheral unit activated)** (3) | | | | | | |
| $I_{peri}$ | Peripheral power domain | Delta current with domain enabled | | 20 | | µA |
| | Serial power domain | Delta current with domain enabled | | 13 | | µA |
| | RF Core | Delta current with power domain enabled, clock enabled, RF core idle | | 237 | | µA |
| | µDMA | Delta current with clock enabled, module idle | | 130 | | µA |
| | Timers | Delta current with clock enabled, module idle | | 113 | | µA |
| | $I^2C$ | Delta current with clock enabled, module idle | | 12 | | µA |
| | I2S | Delta current with clock enabled, module idle | | 36 | | µA |
| | SSI | Delta current with clock enabled, module idle | | 93 | | µA |
| | UART | Delta current with clock enabled, module idle | | 164 | | µA |

(1) Single-ended RF mode is optimized for size and power consumption. Measured on CC2650EM-4XS.
(2) Differential RF mode is optimized for RF performance. Measured on CC2650EM-5XD.
(3) $I_{peri}$ is not supported in Standby or Shutdown.

## 5.5 General Characteristics

Measured on the TI CC2650EM-5XD reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **FLASH MEMORY** | | | | | |
| Supported flash erase cycles before failure | | 100 | | | k Cycles |
| Flash page/sector erase current | Average delta current | | 12.6 | | mA |
| Flash page/sector size | | | 4 | | KB |
| Flash write current | Average delta current, 4 bytes at a time | | 8.15 | | mA |
| Flash page/sector erase time (1) | | | 8 | | ms |
| Flash write time (1) | 4 bytes at a time | | 8 | | µs |

(1) This number is dependent on Flash aging and will increase over time and erase cycles.


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## 5.6 IEEE 802.15.4 (Offset Q-PSK DSSS, 250 kbps) – RX

Measured on the TI CC2650EM-5XD reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Receiver sensitivity | Differential mode. Measured at the CC2650EM-5XD SMA connector, PER = 1% | | –100 | | dBm |
| Receiver sensitivity | Single-ended mode. Measured on CC2650EM-4XS, at the SMA connector, PER = 1% | | –97 | | dBm |
| Receiver saturation | Measured at the CC2650EM-5XD SMA connector, PER = 1% | | +4 | | dBm |
| Adjacent channel rejection | Wanted signal at –82 dBm, modulated interferer at ±5 MHz, PER = 1% | | 39 | | dB |
| Alternate channel rejection | Wanted signal at –82 dBm, modulated interferer at ±10 MHz, PER = 1% | | 52 | | dB |
| Channel rejection, ±15 MHz or more | Wanted signal at –82 dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1% | | 57 | | dB |
| Blocking and desensitization, 5 MHz from upper band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 64 | | dB |
| Blocking and desensitization, 10 MHz from upper band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 64 | | dB |
| Blocking and desensitization, 20 MHz from upper band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 65 | | dB |
| Blocking and desensitization, 50 MHz from upper band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 68 | | dB |
| Blocking and desensitization, –5 MHz from lower band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 63 | | dB |
| Blocking and desensitization, –10 MHz from lower band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 63 | | dB |
| Blocking and desensitization, –20 MHz from lower band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 65 | | dB |
| Blocking and desensitization, –50 MHz from lower band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 67 | | dB |
| Spurious emissions, 30 MHz to 1000 MHz | Conducted measurement in a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66 | | –71 | | dBm |
| Spurious emissions, 1 GHz to 12.75 GHz | Conducted measurement in a 50 Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66 | | –62 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | >200 | | ppm |
| Symbol rate error tolerance | Difference between incoming symbol rate and the internally generated symbol rate | | >1000 | | ppm |
| RSSI dynamic range | | | 100 | | dB |
| RSSI accuracy | | | ±4 | | dB |

## 5.7 IEEE 802.15.4 (Offset Q-PSK DSSS, 250 kbps) – TX

Measured on the TI CC2650EM-5XD reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Output power, highest setting | Delivered to a single-ended 50-Ω load through a balun | | 5 | | dBm |
| Output power, highest setting | Measured on CC2650EM-4XS, delivered to a single-ended 50-Ω load | | 2 | | dBm |
| Output power, lowest setting | Delivered to a single-ended 50-Ω load through a balun | | –21 | | dBm |
| Error vector magnitude | At maximum output power | | 2% | | |

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### IEEE 802.15.4 (Offset Q-PSK DSSS, 250 kbps) – TX *(continued)*

Measured on the TI CC2650EM-5XD reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Spurious emission conducted measurement | f < 1 GHz, outside restricted bands | | –43 | | dBm |
| | f < 1 GHz, restricted bands ETSI | | –65 | | |
| | f < 1 GHz, restricted bands FCC | | –76 | | |
| | f > 1 GHz, including harmonics | | –46 | | |
| | Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan) | | | | |

## 5.8 24-MHz Crystal Oscillator (XOSC_HF)

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.(1)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| ESR Equivalent series resistance(2) | 6 pF < $C_L$ ≤ 9 pF | | 20 | 60 | Ω |
| ESR Equivalent series resistance(2) | 5 pF < $C_L$ ≤ 6 pF | | | 80 | Ω |
| $L_M$ Motional inductance(2) | Relates to load capacitance ($C_L$ in Farads) | | < 1.6 × $10^{-24}$ / $C_L^2$ | | H |
| $C_L$ Crystal load capacitance(2) | | 5 | | 9 | pF |
| Crystal frequency(2)(3) | | | 24 | | MHz |
| Crystal frequency tolerance(2)(4) | | –40 | | 40 | ppm |
| Start-up time(3)(5) | | | 150 | | µs |

(1) Probing or otherwise stopping the XTAL while the DC-DC converter is enabled may cause permanent damage to the device.
(2) The crystal manufacturer's specification must satisfy this requirement
(3) Measured on the TI CC2650EM-5XD reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V
(4) Includes initial tolerance of the crystal, drift over temperature, ageing and frequency pulling due to incorrect load capacitance. As per IEEE 802.15.4 specification.
(5) Kick-started based on a temperature and aging compensated RCOSC_HF using precharge injection.

## 5.9 32.768-kHz Crystal Oscillator (XOSC_LF)

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Crystal frequency(1) | | | 32.768 | | kHz |
| ESR Equivalent series resistance(1) | | | 30 | 100 | kΩ |
| $C_L$ Crystal load capacitance(1) | | 6 | | 12 | pF |

(1) The crystal manufacturer's specification must satisfy this requirement


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## 5.10 48-MHz RC Oscillator (RCOSC_HF)

Measured on the TI CC2650EM-5XD reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Frequency | | | 48 | | MHz |
| Uncalibrated frequency accuracy | | | ±1% | | |
| Calibrated frequency accuracy(1) | | | ±0.25% | | |
| Start-up time | | | 5 | | µs |

(1) Accuracy relative to the calibration source (XOSC_HF).

## 5.11 32-kHz RC Oscillator (RCOSC_LF)

Measured on the TI CC2650EM-5XD reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Calibrated frequency(1) | | | 32.8 | | kHz |
| Temperature coefficient | | | 50 | | ppm/°C |

(1) The frequency accuracy of the Real Time Clock (RTC) is not directly dependent on the frequency accuracy of the 32-kHz RC Oscillator. The RTC can be calibrated to an accuracy within ±500 ppm of 32.768 kHz by measuring the frequency error of RCOSC_LF relative to XOSC_HF and compensating the RTC tick speed. The procedure is explained in *Running Bluetooth® Low Energy on CC2640 Without 32 kHz Crystal*.

## 5.12 ADC Characteristics

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Input voltage range | | 0 | | VDDS | V |
| | Resolution | | | 12 | | Bits |
| | Sample rate | | | | 200 | ksps |
| | Offset | Internal 4.3-V equivalent reference(2) | | 2 | | LSB |
| | Gain error | Internal 4.3-V equivalent reference(2) | | 2.4 | | LSB |
| DNL(3) | Differential nonlinearity | | | >–1 | | LSB |
| INL(4) | Integral nonlinearity | | | ±3 | | LSB |
| ENOB | Effective number of bits | Internal 4.3-V equivalent reference(2), 200 ksps, 9.6-kHz input tone | | 9.8 | | Bits |
| | | VDDS as reference, 200 ksps, 9.6-kHz input tone | | 10 | | |
| | | Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone | | 11.1 | | |
| THD | Total harmonic distortion | Internal 4.3-V equivalent reference(2), 200 ksps, 9.6-kHz input tone | | –65 | | dB |
| | | VDDS as reference, 200 ksps, 9.6-kHz input tone | | –69 | | |
| | | Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone | | –71 | | |
| SINAD, SNDR | Signal-to-noise and Distortion ratio | Internal 4.3-V equivalent reference(2), 200 ksps, 9.6-kHz input tone | | 60 | | dB |
| | | VDDS as reference, 200 ksps, 9.6-kHz input tone | | 63 | | |
| | | Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone | | 69 | | |
| SFDR | Spurious-free dynamic range | Internal 4.3-V equivalent reference(2), 200 ksps, 9.6-kHz input tone | | 67 | | dB |
| | | VDDS as reference, 200 ksps, 9.6-kHz input tone | | 72 | | |
| | | Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone | | 73 | | |

(1) Using IEEE Std 1241™-2010 for terminology and test methods.
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V.
(3) No missing codes. Positive DNL typically varies from +0.3 to +3.5, depending on device (see Figure 5-21).
(4) For a typical example, see Figure 5-22.

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## ADC Characteristics *(continued)*

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Conversion time | Serial conversion, time-to-output, 24-MHz clock | | 50 | | clock-cycles |
| Current consumption | Internal 4.3-V equivalent reference(2) | | 0.66 | | mA |
| Current consumption | VDDS as reference | | 0.75 | | mA |
| Reference voltage | Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TIRTOS API in order to include the gain/offset compensation factors stored in FCFG1. | | 4.3(2)(5) | | V |
| Reference voltage | Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TIRTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: Vref = 4.3 V × 1408 / 4095 | | 1.48 | | V |
| Reference voltage | VDDS as reference (Also known as *RELATIVE*) (input voltage scaling enabled) | | VDDS | | V |
| Reference voltage | VDDS as reference (Also known as *RELATIVE*) (input voltage scaling disabled) | | VDDS / 2.82(5) | | V |
| Input impedance | 200 ksps, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time | | >1 | | MΩ |

(5) Applied voltage must be within absolute maximum ratings (Section 5.1) at all times.

## 5.13 Temperature Sensor

Measured on the TI CC2650EM-5XD reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Resolution | | | 4 | | °C |
| Range | | –40 | | 85 | °C |
| Accuracy | | | ±5 | | °C |
| Supply voltage coefficient(1) | | | 3.2 | | °C/V |

(1) Automatically compensated when using supplied driver libraries.

## 5.14 Battery Monitor

Measured on the TI CC2650EM-5XD reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Resolution | | | 50 | | mV |
| Range | | 1.8 | | 3.8 | V |
| Accuracy | | | 13 | | mV |

## 5.15 Continuous Time Comparator

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage range | | 0 | | VDDS | V |
| External reference voltage | | 0 | | VDDS | V |
| Internal reference voltage | DCOUPL as reference | | 1.27 | | V |
| Offset | | | 3 | | mV |
| Hysteresis | | | <2 | | mV |
| Decision time | Step from –10 mV to 10 mV | | 0.72 | | µs |
| Current consumption when enabled(1) | | | 8.6 | | µA |

(1) Additionally, the bias module must be enabled when running in standby mode.


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## 5.16 Low-Power Clocked Comparator

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage range | | 0 | | VDDS | V |
| Clock frequency | | | 32 | | kHz |
| Internal reference voltage, VDDS / 2 | | | 1.49–1.51 | | V |
| Internal reference voltage, VDDS / 3 | | | 1.01–1.03 | | V |
| Internal reference voltage, VDDS / 4 | | | 0.78–0.79 | | V |
| Internal reference voltage, DCOUPL / 1 | | | 1.25–1.28 | | V |
| Internal reference voltage, DCOUPL / 2 | | | 0.63–0.65 | | V |
| Internal reference voltage, DCOUPL / 3 | | | 0.42–0.44 | | V |
| Internal reference voltage, DCOUPL / 4 | | | 0.33–0.34 | | V |
| Offset | | | <2 | | mV |
| Hysteresis | | | <5 | | mV |
| Decision time | Step from –50 mV to 50 mV | | <1 | | clock-cycle |
| Current consumption when enabled | | | 362 | | nA |

## 5.17 Programmable Current Source

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Current source programmable output range | | | 0.25–20 | | µA |
| Resolution | | | 0.25 | | µA |
| Current consumption(1) | Including current source at maximum programmable output | | 23 | | µA |

(1) Additionally, the bias module must be enabled when running in standby mode.

## 5.18 Synchronous Serial Interface (SSI)

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| S1(1) $t_{clk\_per}$ (SSIClk period) | Device operating as SLAVE | 12 | | 65024 | system clocks |
| S2(1) $t_{clk\_high}$ (SSIClk high time) | Device operating as SLAVE | | 0.5 | | $t_{clk\_per}$ |
| S3(1) $t_{clk\_low}$ (SSIClk low time) | Device operating as SLAVE | | 0.5 | | $t_{clk\_per}$ |
| S1 (TX only)(1) $t_{clk\_per}$ (SSIClk period) | One-way communication to SLAVE - Device operating as MASTER | 4 | | 65024 | system clocks |
| S1 (TX and RX)(1) $t_{clk\_per}$ (SSIClk period) | Normal duplex operation - Device operating as MASTER | 8 | | 65024 | system clocks |
| S2(1) $t_{clk\_high}$ (SSIClk high time) | Device operating as MASTER | | 0.5 | | $t_{clk\_per}$ |
| S3(1) $t_{clk\_low}$ (SSIClk low time) | Device operating as MASTER | | 0.5 | | $t_{clk\_per}$ |

(1) Refer to SSI timing diagrams Figure 5-1, Figure 5-2, and Figure 5-3.

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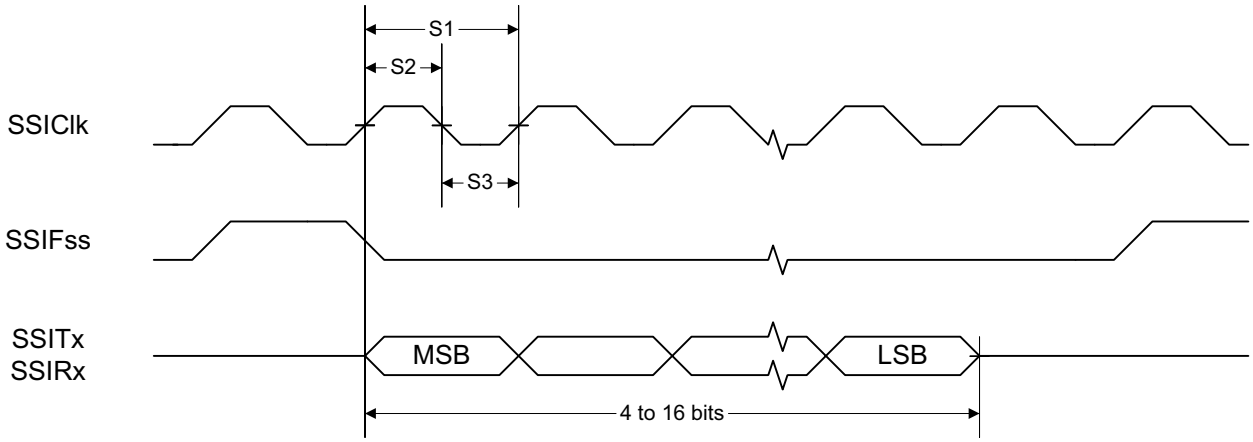


**Figure 5-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement**

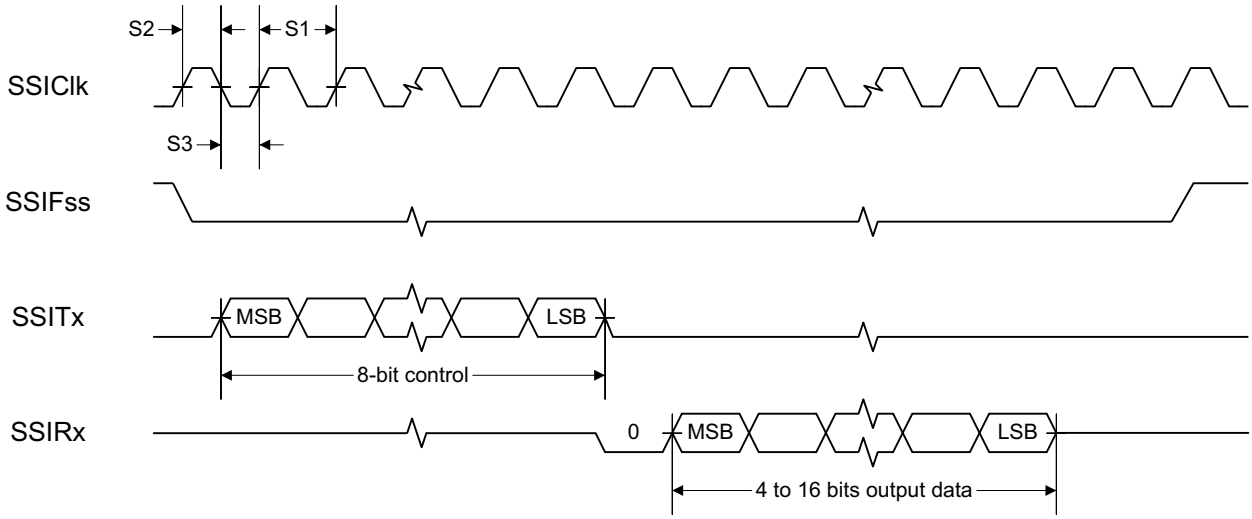


**Figure 5-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer**


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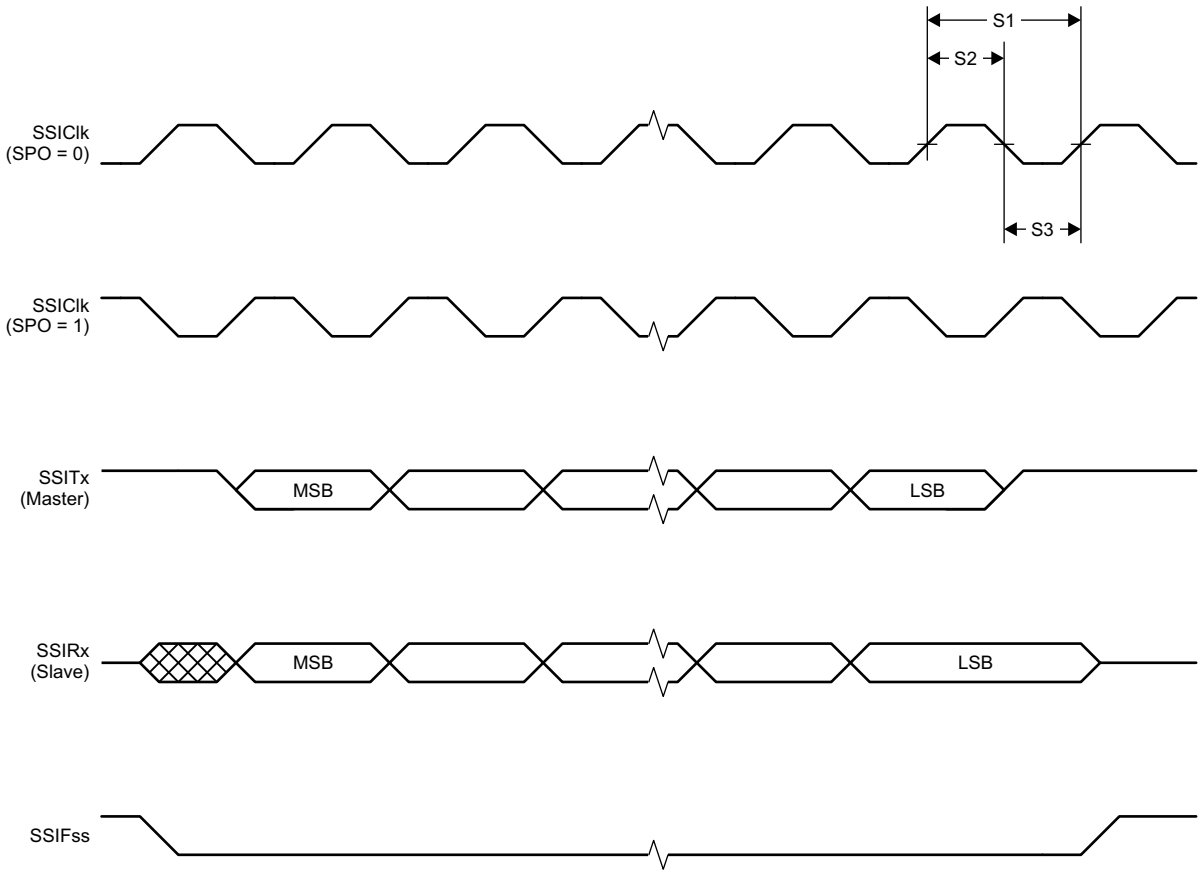


**Figure 5-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1**

## 5.19 DC Characteristics

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **$T_A$ = 25°C, $V_{DDS}$ = 1.8 V** | | | | | |
| GPIO VOH at 8-mA load | IOCURR = 2, high-drive GPIOs only | 1.32 | 1.54 | | V |
| GPIO VOL at 8-mA load | IOCURR = 2, high-drive GPIOs only | | 0.26 | 0.32 | V |
| GPIO VOH at 4-mA load | IOCURR = 1 | 1.32 | 1.58 | | V |
| GPIO VOL at 4-mA load | IOCURR = 1 | | 0.21 | 0.32 | V |
| GPIO pullup current | Input mode, pullup enabled, Vpad = 0 V | | 71.7 | | µA |
| GPIO pulldown current | Input mode, pulldown enabled, Vpad = VDDS | | 21.1 | | µA |
| GPIO high/low input transition, no hysteresis | IH = 0, transition between reading 0 and reading 1 | | 0.88 | | V |
| GPIO low-to-high input transition, with hysteresis | IH = 1, transition voltage for input read as 0 → 1 | | 1.07 | | V |
| GPIO high-to-low input transition, with hysteresis | IH = 1, transition voltage for input read as 1 → 0 | | 0.74 | | V |
| GPIO input hysteresis | IH = 1, difference between 0 → 1 and 1 → 0 points | | 0.33 | | V |
| **$T_A$ = 25°C, $V_{DDS}$ = 3.0 V** | | | | | |
| GPIO VOH at 8-mA load | IOCURR = 2, high-drive GPIOs only | | 2.68 | | V |
| GPIO VOL at 8-mA load | IOCURR = 2, high-drive GPIOs only | | 0.33 | | V |
| GPIO VOH at 4-mA load | IOCURR = 1 | | 2.72 | | V |
| GPIO VOL at 4-mA load | IOCURR = 1 | | 0.28 | | V |
| **$T_A$ = 25°C, $V_{DDS}$ = 3.8 V** | | | | | |
| GPIO pullup current | Input mode, pullup enabled, Vpad = 0 V | | 277 | | µA |

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## DC Characteristics *(continued)*

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| GPIO pulldown current | Input mode, pulldown enabled, Vpad = VDDS | | 113 | | µA |
| GPIO high/low input transition, no hysteresis | IH = 0, transition between reading 0 and reading 1 | | 1.67 | | V |
| GPIO low-to-high input transition, with hysteresis | IH = 1, transition voltage for input read as 0 → 1 | | 1.94 | | V |
| GPIO high-to-low input transition, with hysteresis | IH = 1, transition voltage for input read as 1 → 0 | | 1.54 | | V |
| GPIO input hysteresis | IH = 1, difference between 0 → 1 and 1 → 0 points | | 0.4 | | V |
| **$T_A$ = 25°C** | | | | | |
| VIH | Lowest GPIO input voltage reliably interpreted as a «High» | | | 0.8 | VDDS(1) |
| VIL | Highest GPIO input voltage reliably interpreted as a «Low» | 0.2 | | | VDDS(1) |

(1) Each GPIO is referenced to a specific VDDS pin. See the technical reference manual listed in 节 8.3 for more details.

## 5.20 Thermal Resistance Characteristics

| NAME | DESCRIPTION | RSM (°C/W)(1) (2) | RHB (°C/W)(1) (2) | RGZ (°C/W)(1) (2) |
|---|---|---|---|---|
| $R\theta_{JA}$ | Junction-to-ambient thermal resistance | 36.9 | 32.8 | 29.6 |
| $R\theta_{JC(top)}$ | Junction-to-case (top) thermal resistance | 30.3 | 24.0 | 15.7 |
| $R\theta_{JB}$ | Junction-to-board thermal resistance | 7.6 | 6.8 | 6.2 |
| $Psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | 0.3 | 0.3 |
| $Psi_{JB}$ | Junction-to-board characterization parameter | 7.4 | 6.8 | 6.2 |
| $R\theta_{JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 2.1 | 1.9 | 1.9 |

(1) °C/W = degrees Celsius per watt.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*.
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*.

Power dissipation of 2 W and an ambient temperature of 70ºC is assumed.


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## 5.21 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Rising supply-voltage slew rate | | 0 | | 100 | mV/µs |
| Falling supply-voltage slew rate | | 0 | | 20 | mV/µs |
| Falling supply-voltage slew rate, with low-power flash settings(1) | | | | 3 | mV/µs |
| Positive temperature gradient in standby(2) | No limitation for negative temperature gradient, or outside standby mode | | | 5 | °C/s |
| **CONTROL INPUT AC CHARACTERISTICS(3)** | | | | | |
| RESET_N low duration | | 1 | | | µs |

(1) For smaller coin cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-µF VDDS input capacitor (see Figure 7-1) must be used to ensure compliance with this slew rate.
(2) Applications using RCOSC_LF as sleep timer must also consider the drift in frequency caused by a change in temperature (see Section 5.11).
(3) $T_A$ = –40°C to +85°C, $V_{DDS}$ = 1.7 V to 3.8 V, unless otherwise noted.

## 5.22 Switching Characteristics

Measured on the TI CC2650EM-5XD reference design with $T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **WAKEUP AND TIMING** | | | | | |
| Idle → Active | | | 14 | | µs |
| Standby → Active | | | 151 | | µs |
| Shutdown → Active | | | 1015 | | µs |

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## 5.23 Typical Characteristics

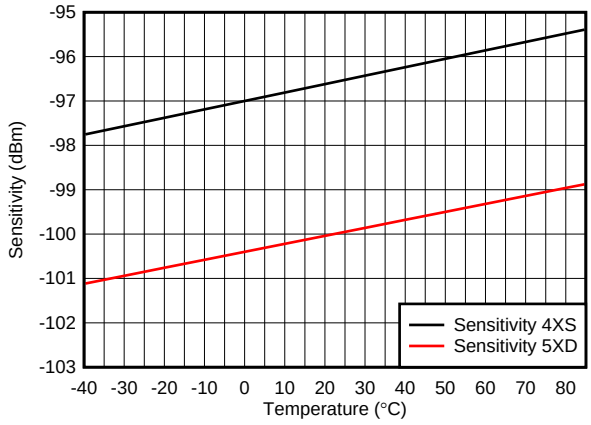


**Figure 5-4. IEEE 802.15.4 Sensitivity vs Temperature**

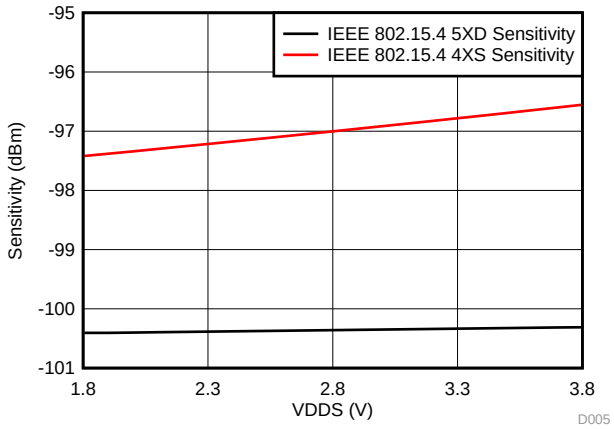


**Figure 5-5. IEEE 802.15.4 Sensitivity vs Supply Voltage (VDDS)**

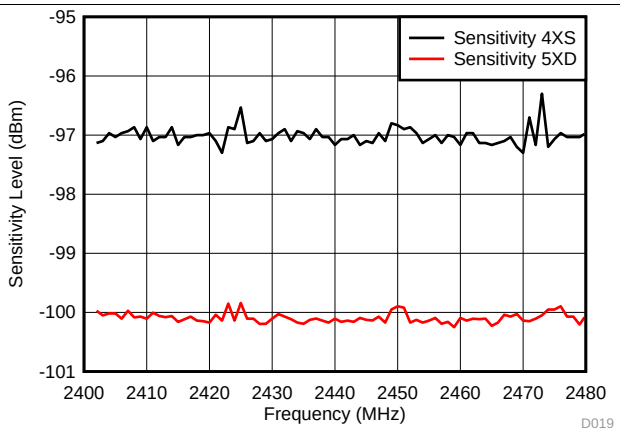


**Figure 5-6. IEEE 802.15.4 Sensitivity vs Channel Frequency**

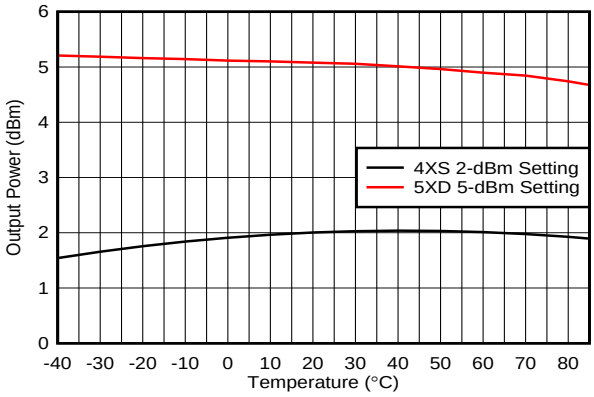


**Figure 5-7. TX Output Power vs Temperature**

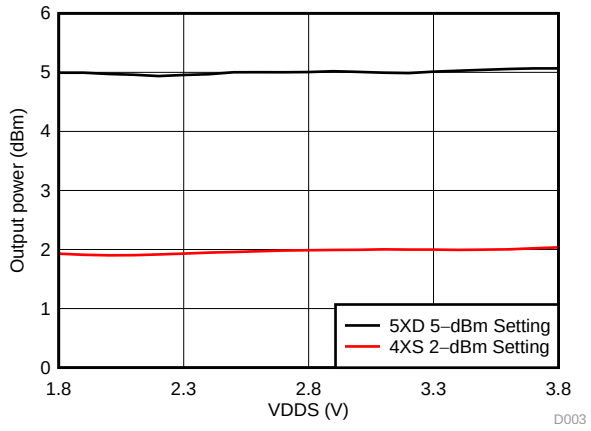


**Figure 5-8. TX Output Power vs Supply Voltage (VDDS)**

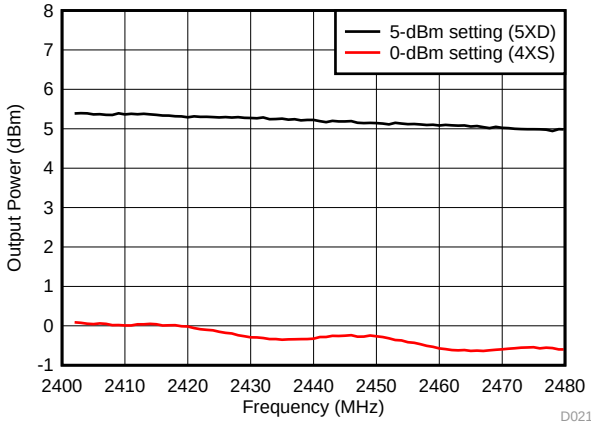


**Figure 5-9. TX Output Power vs Channel Frequency**


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## Typical Characteristics *(continued)*

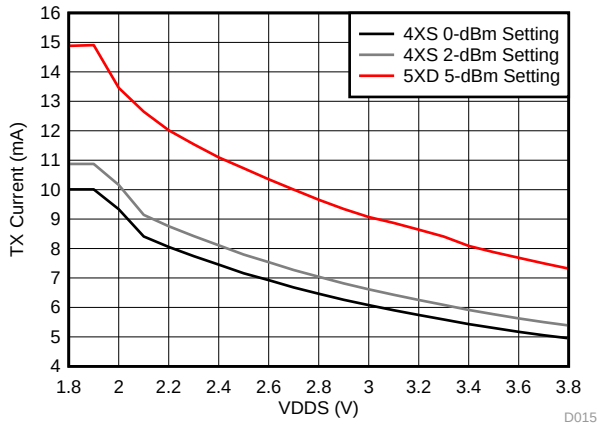


**Figure 5-10. TX Current Consumption vs Supply Voltage (VDDS)**

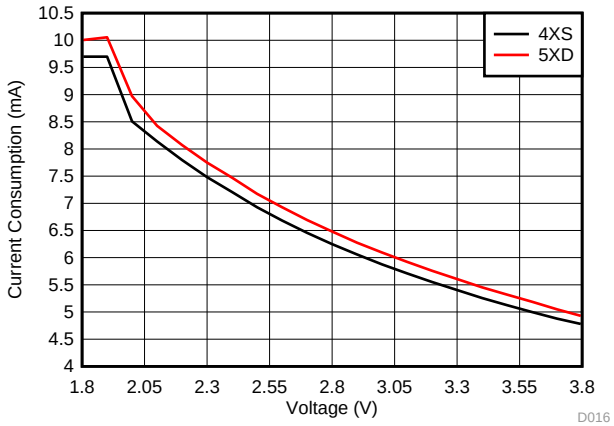


**Figure 5-11. RX Mode Current vs Supply Voltage (VDDS)**

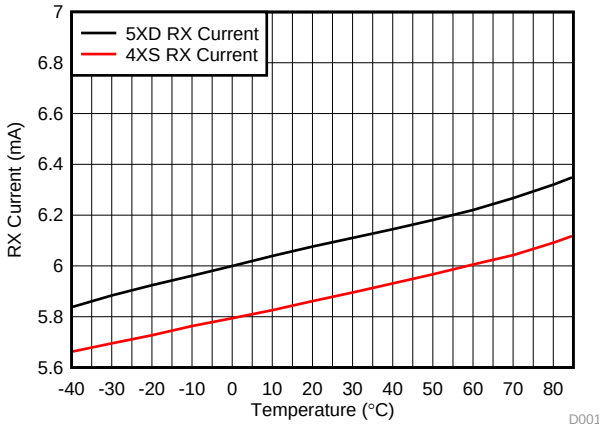


**Figure 5-12. RX Mode Current Consumption vs Temperature**

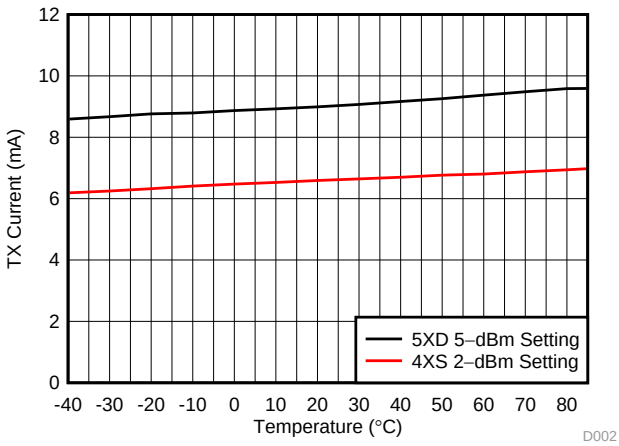


**Figure 5-13. TX Mode Current Consumption vs Temperature**

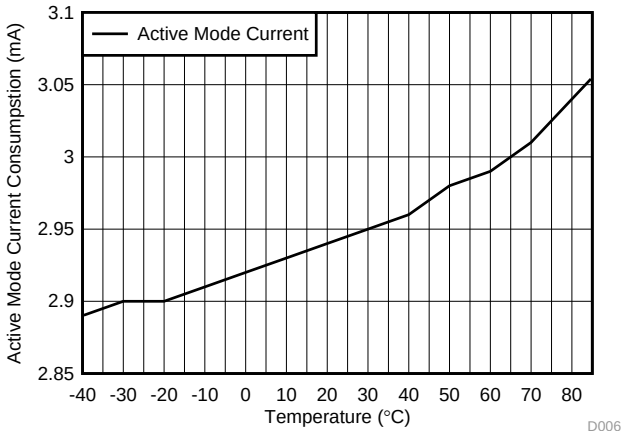


**Figure 5-14. Active Mode (MCU Running, No Peripherals) Current Consumption vs Temperature**

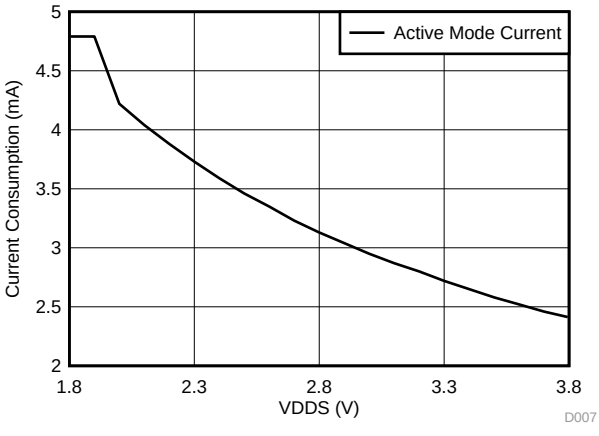


**Figure 5-15. Active Mode (MCU Running, No Peripherals) Current Consumption vs Supply Voltage (VDDS)**

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## Typical Characteristics *(continued)*

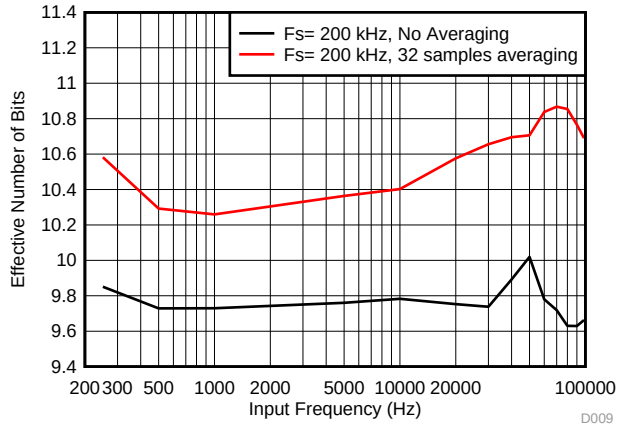


**Figure 5-16. SoC ADC Effective Number of Bits vs Input Frequency (Internal Reference, Scaling enabled)**

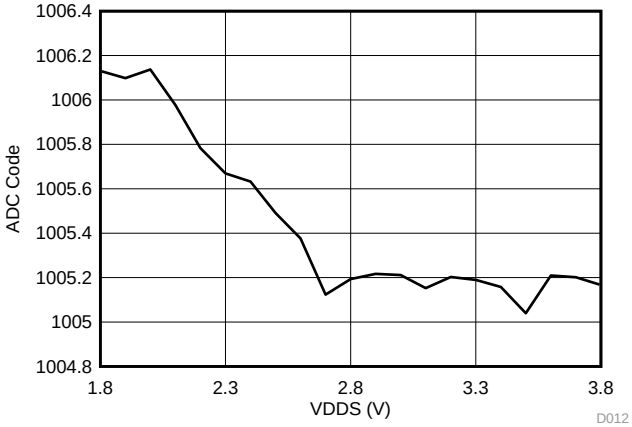


**Figure 5-17. SoC ADC Output vs Supply Voltage (Fixed Input, Internal Reference)**

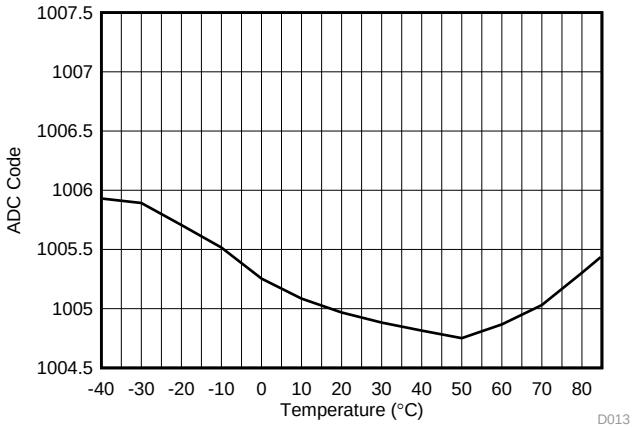


**Figure 5-18. SoC ADC Output vs Temperature (Fixed Input, Internal Reference)**

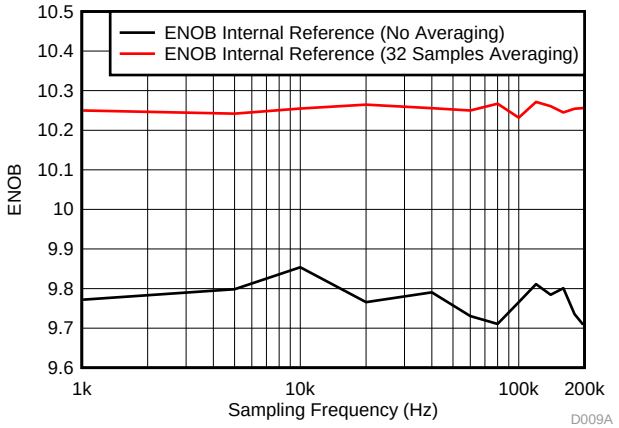


**Figure 5-19. SoC ADC ENOB vs Sampling Frequency (Scaling enabled, input frequency = FS / 10)**

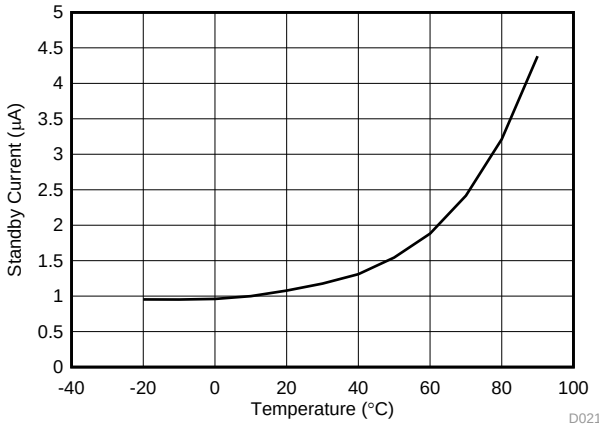


**Figure 5-20. Standby Mode Supply Current vs Temperature**


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## Typical Characteristics *(continued)*

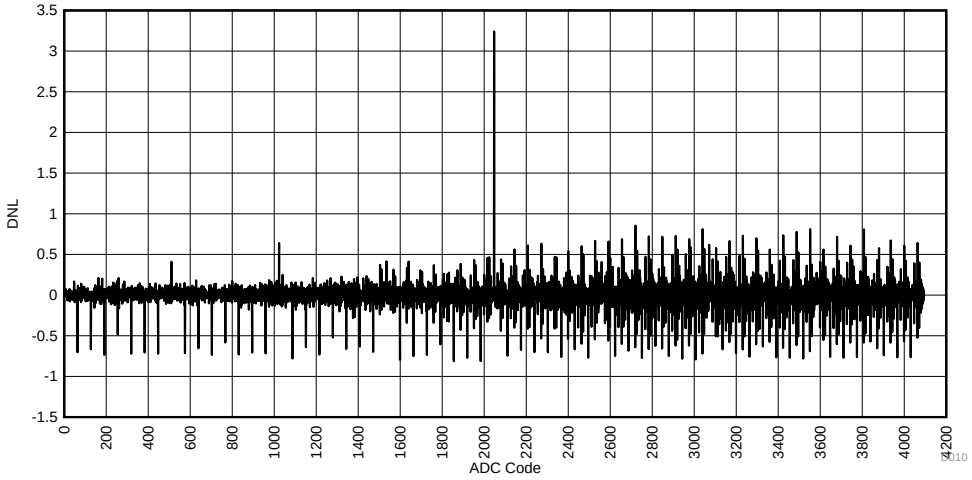


**Figure 5-21. SoC ADC DNL vs ADC Code (Internal Reference)**

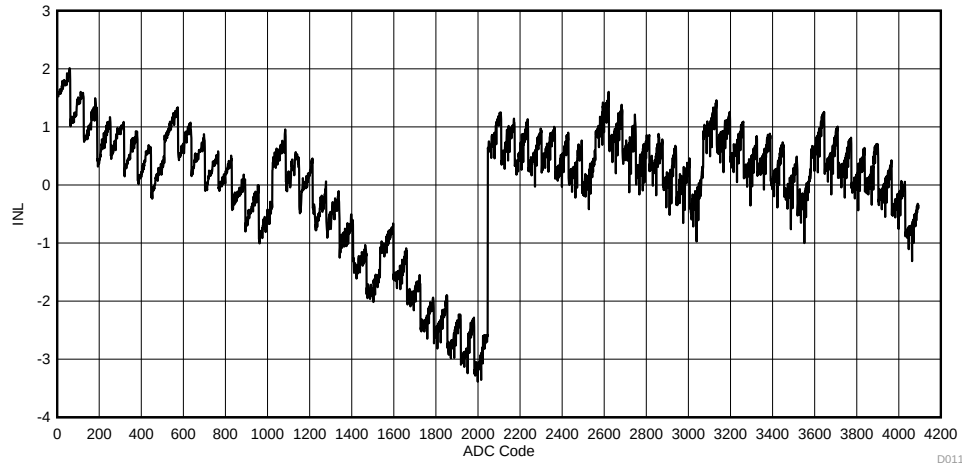


**Figure 5-22. SoC ADC INL vs ADC Code (Internal Reference)**

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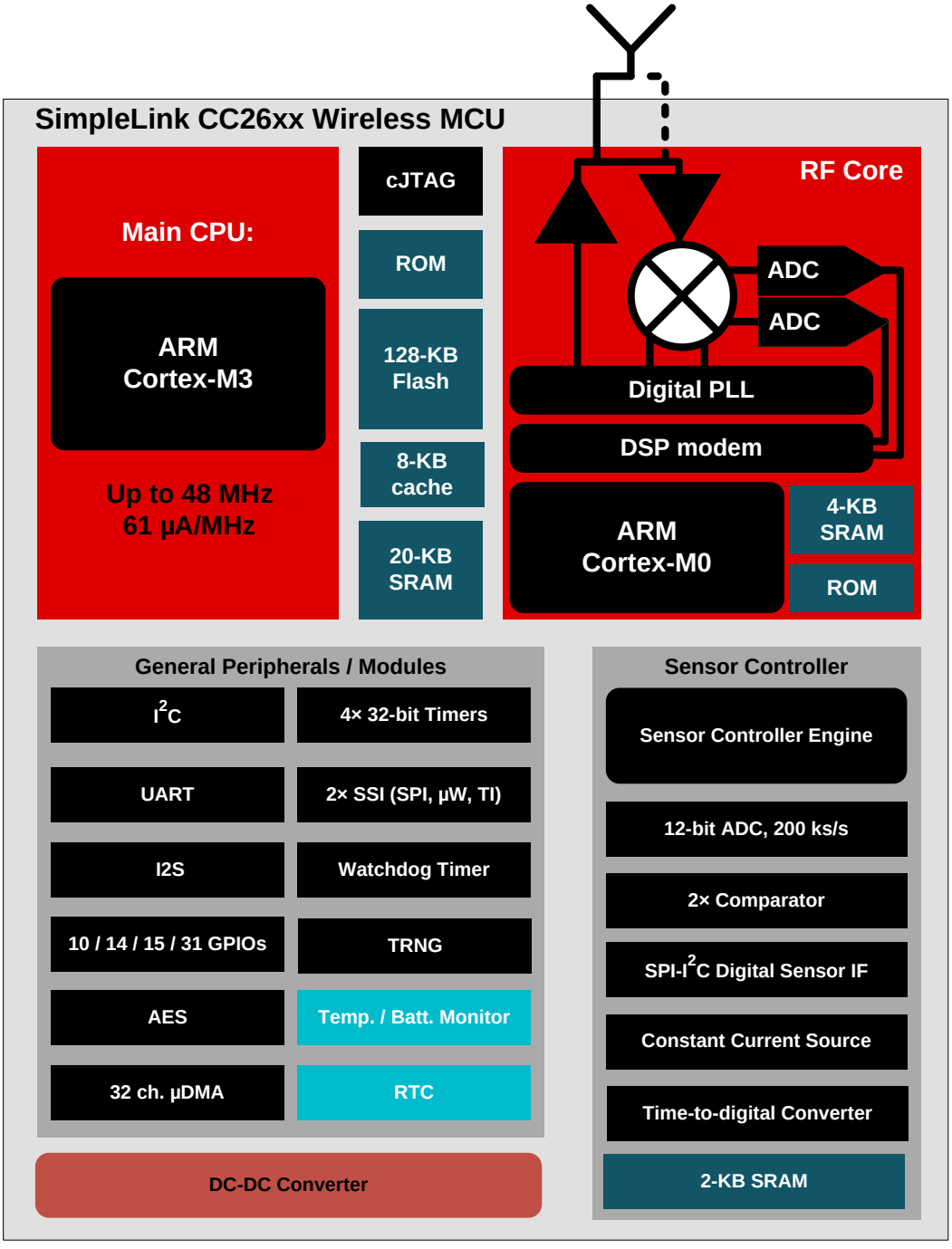
# 6 Detailed Description

## 6.1 Overview

The core modules of the CC26xx product family are shown in Section 6.2.

## 6.2 Functional Block Diagram

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## 6.3 Main CPU

The SimpleLink CC2630 Wireless MCU contains an ARM Cortex-M3 (CM3) 32-bit CPU, which runs the application and the higher layers of the protocol stack.

The CM3 processor provides a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

CM3 features include the following:

- 32-bit ARM Cortex-M3 architecture optimized for small-footprint embedded applications
- Outstanding processing performance combined with fast interrupt handling
- ARM Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications:
  - Single-cycle multiply instruction and hardware divide
  - Atomic bit manipulation (bit-banding), delivering maximum memory use and streamlined peripheral control
  - Unaligned data access, enabling data to be efficiently packed into memory
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system, and memories
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial wire trace reduces the number of pins required for debugging and tracing
- Migration from the ARM7™ processor family for better performance and power efficiency
- Optimized for single-cycle flash memory use
- Ultralow-power consumption with integrated sleep modes
- 1.25 DMIPS per MHz

## 6.4 RF Core

The RF Core contains an ARM Cortex-M0 processor that interfaces the analog RF and base-band circuitries, handles data to and from the system side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU.

The RF core is capable of autonomously handling the time-critical aspects of the radio protocols (802.15.4 ZigBee) thus offloading the main CPU and leaving more resources for the user application.

The RF core has a dedicated 4-KB SRAM block and runs initially from separate ROM memory. The ARM Cortex-M0 processor is not programmable by customers.

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## 6.5 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in standby mode. The peripherals in this domain may be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously, thereby significantly reducing power consumption and offloading the main CM3 CPU. The GPIOs that can be connected to the Sensor Controller are listed in Table 6-1.

The Sensor Controller is set up using a PC-based configuration tool, called Sensor Controller Studio, and potential use cases may be (but are not limited to):

- Analog sensors using integrated ADC
- Digital sensors using GPIOs, bit-banged $I^2C$, and SPI
- UART communication for sensor reading or debugging
- Capacitive sensing
- Waveform generation
- Pulse counting
- Keyboard scan
- Quadrature decoder for polling rotation sensors
- Oscillator calibration

**NOTE**

Texas Instruments provides application examples for some of these use cases, but not for all of them.

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the device from any state in which the comparator is active. A configurable internal reference can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller will take care of baseline tracking, hysteresis, filtering and other related functions.
- The ADC is a 12-bit, 200-ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources, including timers, I/O pins, software, the analog comparator, and the RTC.
- The Sensor Controller also includes a SPI–$I^2C$ digital interface.
- The analog modules can be connected to up to eight different GPIOs.

The peripherals in the Sensor Controller can also be controlled from the main application processor.


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**Table 6-1. GPIOs Connected to the Sensor Controller(1)**

| ANALOG CAPABLE | 7 × 7 RGZ DIO NUMBER | 5 × 5 RHB DIO NUMBER | 4 × 4 RSM DIO NUMBER |
|---|---|---|---|
| Y | 30 | 14 | |
| Y | 29 | 13 | |
| Y | 28 | 12 | |
| Y | 27 | 11 | 9 |
| Y | 26 | 9 | 8 |
| Y | 25 | 10 | 7 |
| Y | 24 | 8 | 6 |
| Y | 23 | 7 | 5 |
| N | 7 | 4 | 2 |
| N | 6 | 3 | 1 |
| N | 5 | 2 | 0 |
| N | 4 | 1 | |
| N | 3 | 0 | |
| N | 2 | | |
| N | 1 | | |
| N | 0 | | |

(1) Depending on the package size, up to 16 pins can be connected to the Sensor Controller. Up to 8 of these pins can be connected to analog modules.

## 6.6 Memory

The flash memory provides nonvolatile storage for code and data. The flash memory is in-system programmable.

The SRAM (static RAM) can be used for both storage of data and execution of code and is split into two 4-KB blocks and two 6-KB blocks. Retention of the RAM contents in standby mode can be enabled or disabled individually for each block to minimize power consumption. In addition, if flash cache is disabled, the 8-KB cache can be used as a general-purpose RAM.

The ROM provides preprogrammed embedded TI RTOS kernel, Driverlib and lower layer protocol stack software (802.15.4 MAC). It also contains a bootloader that can be used to reprogram the device using SPI or UART.

## 6.7 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface.

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## 6.8 Power Management

To minimize power consumption, the CC2630 device supports a number of power modes and power management features (see Table 6-2).

**Table 6-2. Power Modes**

| MODE | SOFTWARE CONFIGURABLE POWER MODES | | | | RESET PIN HELD |
|---|---|---|---|---|---|
| | ACTIVE | IDLE | STANDBY | SHUTDOWN | |
| **CPU** | Active | Off | Off | Off | Off |
| **Flash** | On | Available | Off | Off | Off |
| **SRAM** | On | On | On | Off | Off |
| **Radio** | Available | Available | Off | Off | Off |
| **Supply System** | On | On | Duty Cycled | Off | Off |
| Current | 1.45 mA + 31 µA/MHz | 550 µA | 1 µA | 0.15 µA | 0.1 µA |
| Wake-up Time to CPU Active(1) | – | 14 µs | 151 µs | 1015 µs | 1015 µs |
| Register Retention | Full | Full | Partial | No | No |
| SRAM Retention | Full | Full | Full | No | No |
| High-Speed Clock | XOSC_HF or RCOSC_HF | XOSC_HF or RCOSC_HF | Off | Off | Off |
| Low-Speed Clock | XOSC_LF or RCOSC_LF | XOSC_LF or RCOSC_LF | XOSC_LF or RCOSC_LF | Off | Off |
| Peripherals | Available | Available | Off | Off | Off |
| Sensor Controller | Available | Available | Available | Off | Off |
| Wake up on RTC | Available | Available | Available | Off | Off |
| Wake up on Pin Edge | Available | Available | Available | Available | Off |
| Wake up on Reset Pin | Available | Available | Available | Available | Available |
| Brown Out Detector (BOD) | Active | Active | Duty Cycled(2) | Off | N/A |
| Power On Reset (POR) | Active | Active | Active | Active | N/A |

(1) Not including RTOS overhead
(2) The Brown Out Detector is disabled between recharge periods in STANDBY. Lowering the supply voltage below the BOD threshold between two recharge periods while in STANDBY may cause the BOD to lock the device upon wake-up until a Reset/POR releases it. To avoid this, it is recommended that STANDBY mode is avoided if there is a risk that the supply voltage (VDDS) may drop below the specified operating voltage range. For the same reason, it is also good practice to ensure that a power cycling operation, such as a battery replacement, triggers a Power-on-reset by ensuring that the VDDS decoupling network is fully depleted before applying supply voltage again (for example, inserting new batteries).

In active mode, the application CM3 CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see Table 6-2).

In idle mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event will bring the processor back into active mode.

In standby mode, only the always-on domain (AON) is active. An external wake-up event, RTC event, or sensor-controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In shutdown mode, the device is turned off entirely, including the AON domain and the Sensor Controller. The I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake-up from Shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between a reset in this way, a reset-by-reset pin, or a power-on-reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the Flash memory contents.


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The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the main CPU, which means that the main CPU does not have to wake up, for example, to execute an ADC sample or poll a digital sensor over SPI. The main CPU saves both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio enables the user to configure the sensor controller and choose which peripherals are controlled and which conditions wake up the main CPU.

## 6.9 Clock Systems

The CC2630 supports two external and two internal clock sources.

A 24-MHz crystal is required as the frequency reference for the radio. This signal is doubled internally to create a 48-MHz clock.

The 32-kHz crystal is optional. The low-speed crystal oscillator is designed for use with a 32-kHz watch-type crystal.

The internal high-speed oscillator (48-MHz) can be used as a clock source for the CPU subsystem.

The internal low-speed oscillator (32.768-kHz) can be used as a reference if the low-power crystal oscillator is not used.

The 32-kHz clock source can be used as external clocking reference through GPIO.

## 6.10 General Peripherals and Modules

The I/O controller controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high drive capabilities (marked in **bold** in Section 4).

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and Texas Instruments synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz.

The UART implements a universal asynchronous receiver/transmitter function. It supports flexible baud-rate generation up to a maximum of 3 Mbps .

Timer 0 is a general-purpose timer module (GPTM), which provides two 16-bit timers. The GPTM can be configured to operate as a single 32-bit timer, dual 16-bit timers or as a PWM module.

Timer 1, Timer 2, and Timer 3 are also GPTMs. Each of these timers is functionally equivalent to Timer 0.

In addition to these four timers, the RF core has its own timer to handle timing for RF protocols; the RF timer can be synchronized to the RTC.

The $I^2C$ interface is used to communicate with devices compatible with the $I^2C$ standard. The $I^2C$ interface is capable of 100-kHz and 400-kHz operation, and can serve as both $I^2C$ master and $I^2C$ slave.

The TRNG module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear combinatorial circuit.

The watchdog timer is used to regain control if the system fails due to a software error after an external device fails to respond as expected. The watchdog timer can generate an interrupt or a reset when a predefined time-out value is reached.

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The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data transfer tasks from the CM3 CPU, allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data. Some features of the µDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes:
  - Memory-to-memory
  - Memory-to-peripheral
  - Peripheral-to-memory
  - Peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits

The AON domain contains circuitry that is always enabled, except for in Shutdown (where the digital supply is off). This circuitry includes the following:

- The RTC can be used to wake the device from any state where it is active. The RTC contains three compare and one capture registers. With software support, the RTC can be used for clock and calendar operation. The RTC is clocked from the 32-kHz RC oscillator or crystal. The RTC can also be compensated to tick at the correct frequency even when the internal 32-kHz RC oscillator is used instead of a crystal.
- The battery monitor and temperature sensor are accessible by software and give a battery status indication as well as a coarse temperature measure.

## 6.11 Voltage Supply Domains

The CC2630 device can interface to two or three different voltage domains depending on the package type. On-chip level converters ensure correct operation as long as the signal voltage on each input/output pin is set with respect to the corresponding supply pin (VDDS, VDDS2 or VDDS3). lists the pin-to-VDDS mapping.

**Table 6-3. Pin Function to VDDS Mapping Table**

| | Package | | |
|---|---|---|---|
| | **VQFN 7 × 7 (RGZ)** | **VQFN 5 × 5 (RHB)** | **VQFN 4 × 4 (RSM)** |
| **VDDS**(1) | DIO 23–30<br>Reset_N | DIO 7–14<br>Reset_N | DIO 5–9<br>Reset_N |
| **VDDS2** | DIO 0–11 | DIO 0–6<br>JTAG | DIO 0–4<br>JTAG |
| **VDDS3** | DIO 12–22<br>JTAG | N/A | N/A |

(1) VDDS_DCDC must be connected to VDDS on the PCB.

## 6.12 System Architecture

Depending on the product configuration, CC26xx can function either as a Wireless Network Processor (WNP—an IC running the wireless protocol stack, with the application running on a separate MCU), or as a System-on-Chip (SoC), with the application and protocol stack running on the ARM CM3 core inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.


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# 7 Application, Implementation, and Layout

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 7.1 Application Information

Very few external components are required for the operation of the CC2630 device. This section provides some general information about the various configuration options when using the CC2630 in an application, and then shows two examples of application circuits with schematics and layout. This is only a small selection of the many application circuit examples available as complete reference designs from the product folder on www.ti.com.

Figure 7-1 shows the various RF front-end configuration options. The RF front end can be used in differential- or single-ended configurations with the options of having internal or external biasing. These options allow for various trade-offs between cost, board space, and RF performance. Differential operation with external bias gives the best performance while single-ended operation with internal bias gives the least amount of external components and the lowest power consumption. Reference designs exist for each of these options.

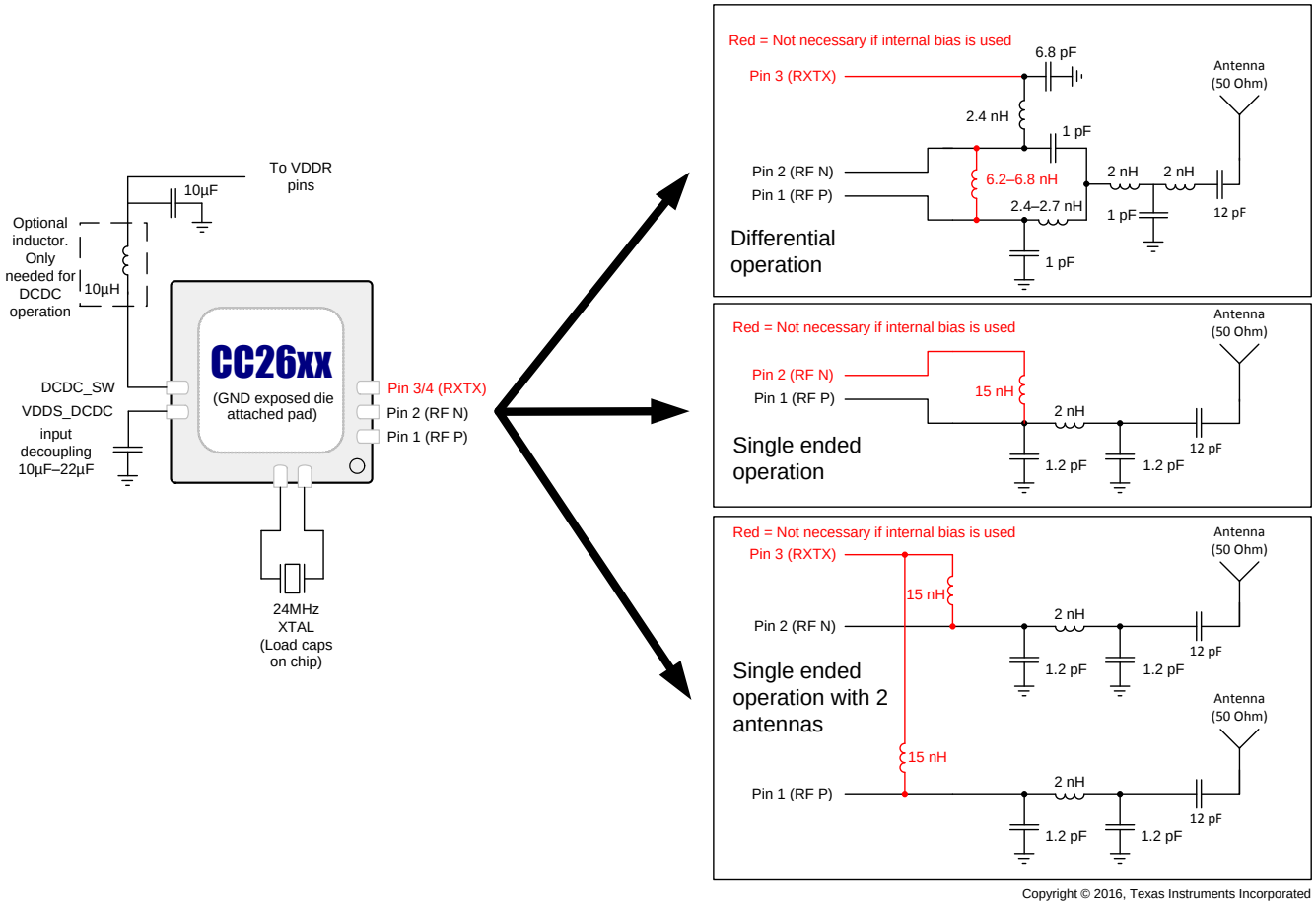


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**Figure 7-1. CC2630 Application Circuit**

Figure 7-2 shows the various supply voltage configuration options. Not all power supply decoupling capacitors or digital I/Os are shown. Exact pin positions will vary between the different package options. For a detailed overview of power supply decoupling and wiring, see the TI reference designs and the CC26xx technical reference manual (节 8.3).

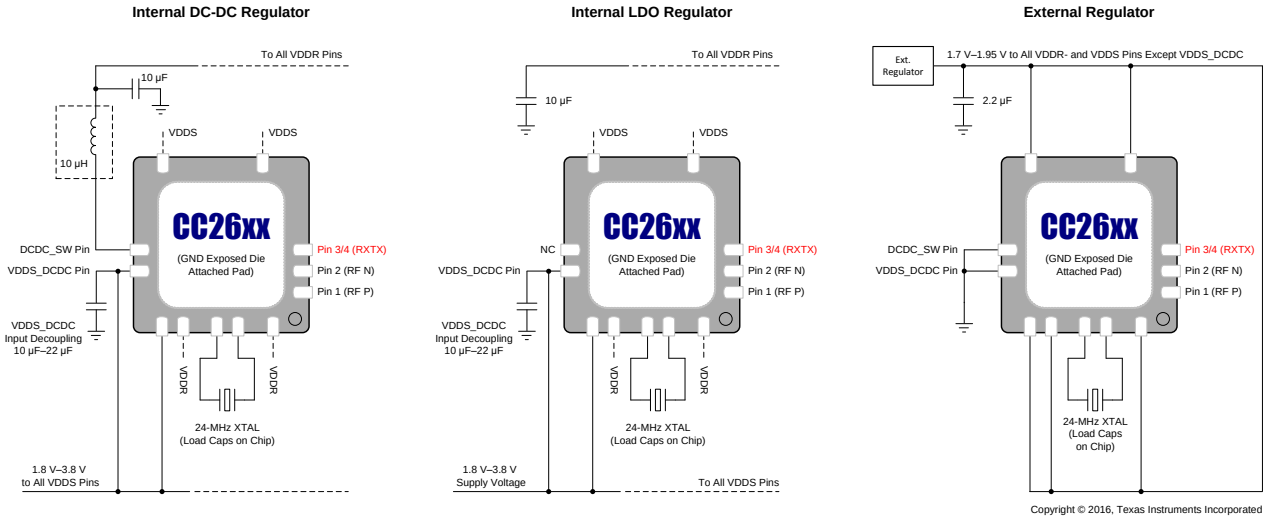


**Figure 7-2. Supply Voltage Configurations**


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## 7.2 5 × 5 External Differential (5XD) Application Circuit

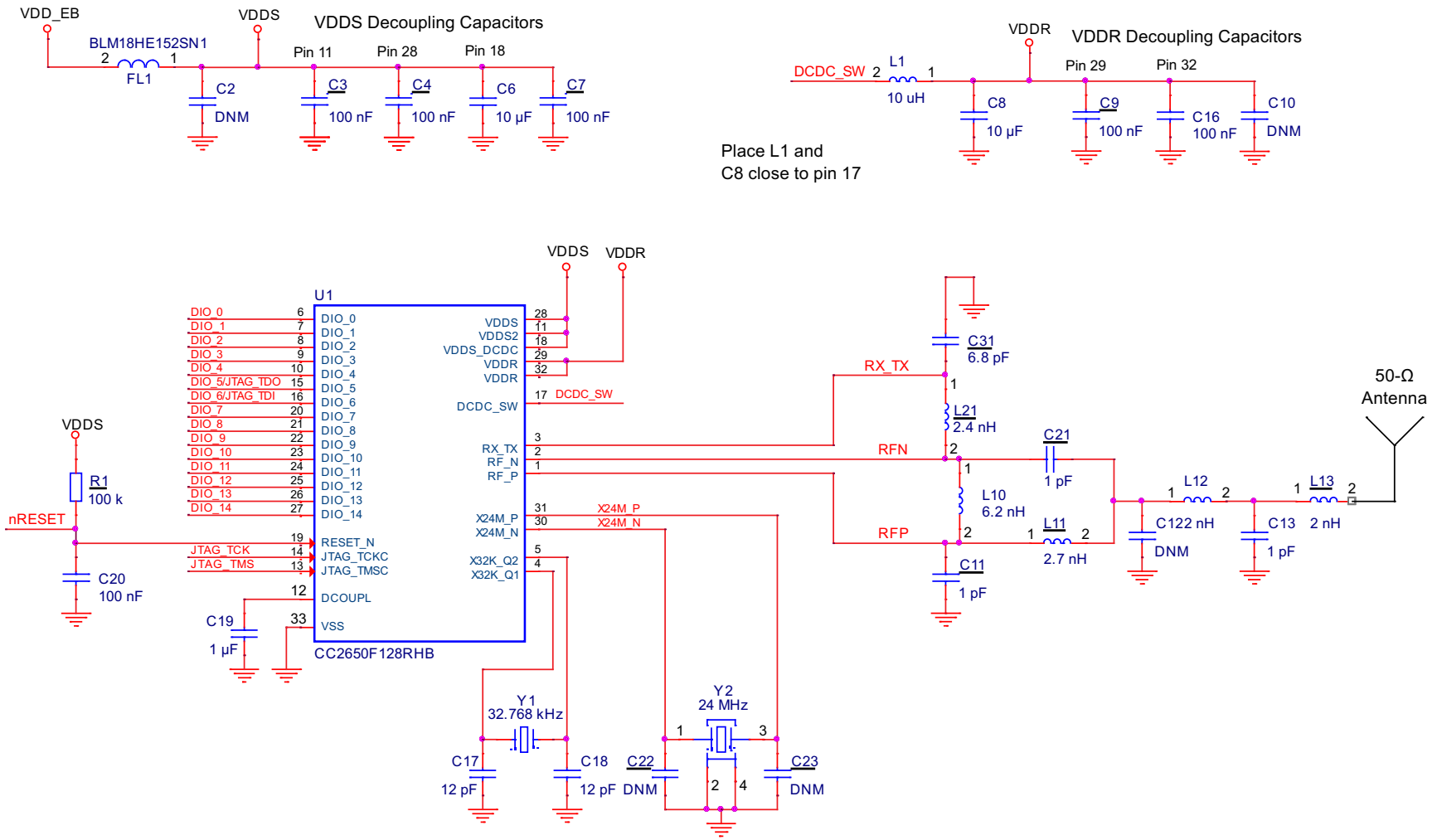


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**Figure 7-3. 5 × 5 External Differential (5XD) Application Circuit**

### 7.2.1 Layout

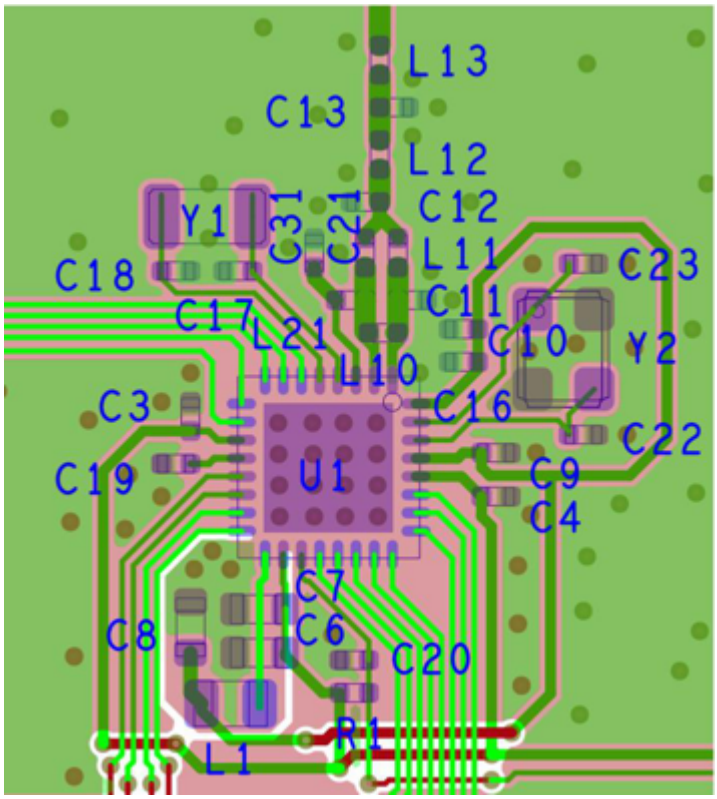


**Figure 7-4. 5 × 5 External Differential (5XD) Layout**


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## 7.3 4 × 4 External Single-ended (4XS) Application Circuit

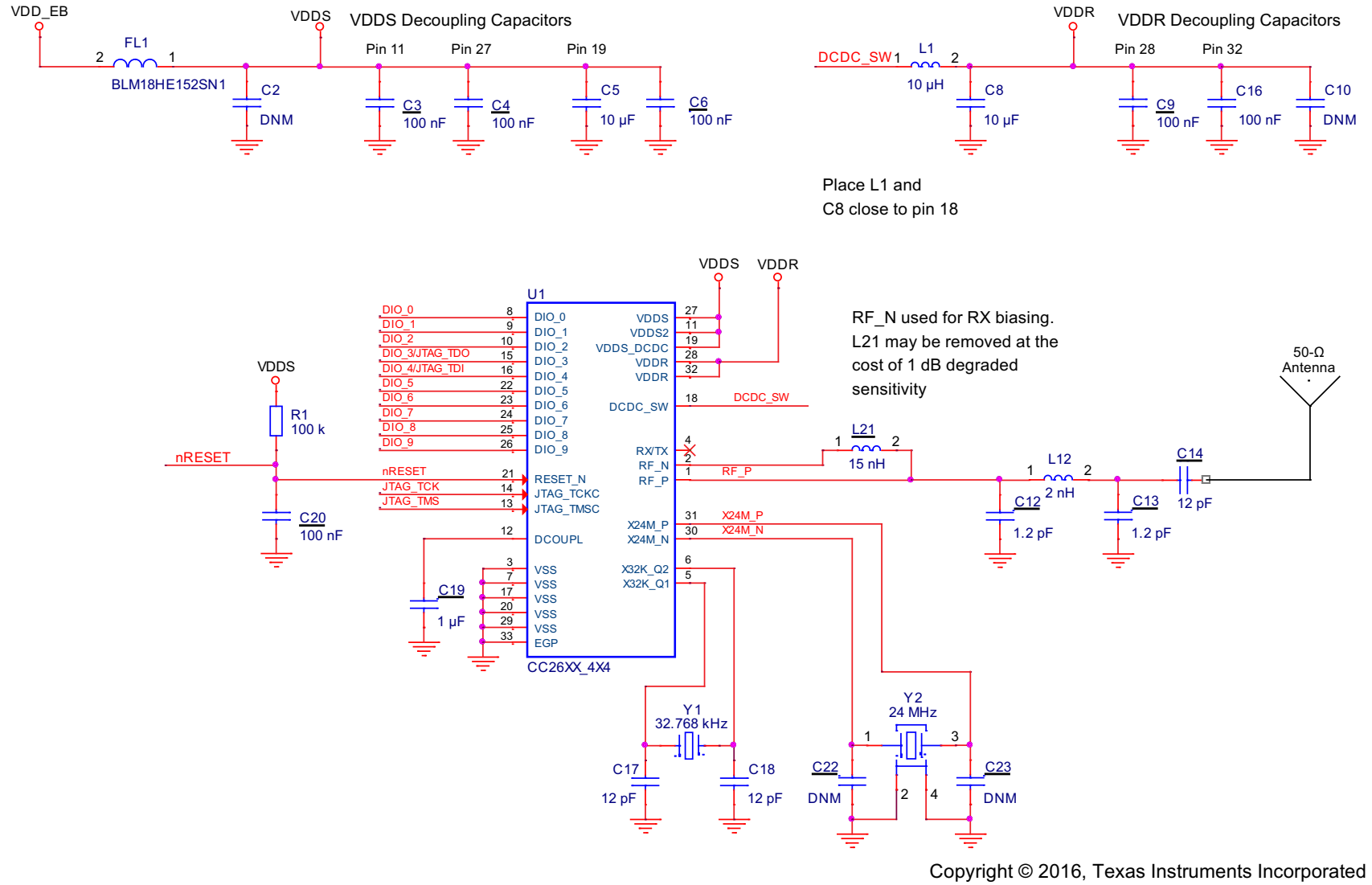


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**Figure 7-5. 4 × 4 External Single-ended (4XS) Application Circuit**

### 7.3.1 Layout

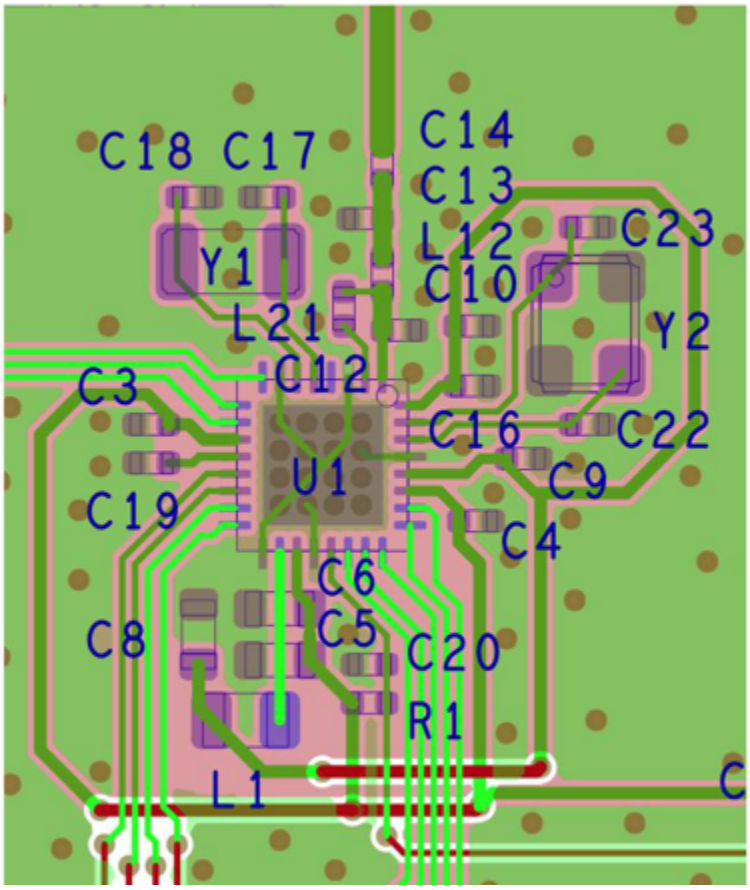


**Figure 7-6. 4 × 4 External Single-ended (4XS) Layout**


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# 8 器件和文档支持

## 8.1 器件命名规则

为了标明产品开发周期的各个产品阶段，TI 为所有预生产部件号或日期代码标记分配了前缀。每个器件都具有以下三个前缀/标识中的一个：X、P 或无（无前缀）（例如 CC2630 正在批量生产，因此未分配前缀/标识）。

器件开发进化流程：

**X** 试验器件不一定代表最终器件的电气规范标准并且不可使用生产组装流程。

**P** 原型器件不一定是最终芯片模型并且不一定符合最终电气标准规范。

无 完全合格的芯片模型的生产版本。

生产器件已进行完全特性化，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件（X 或者 P）的故障率大于标准生产器件。由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。只有合格的生产器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。这个后缀表示封装类型（例如，*RSM*）。

要获得 *CC2630* 器件（采用 *RSM*、*RHB* 或 *RGZ* 封装类型）的订购部件号，请参见本文档的封装选项附录（访问 TI 网站 www.ti.com），或者联系您的 TI 销售代表。

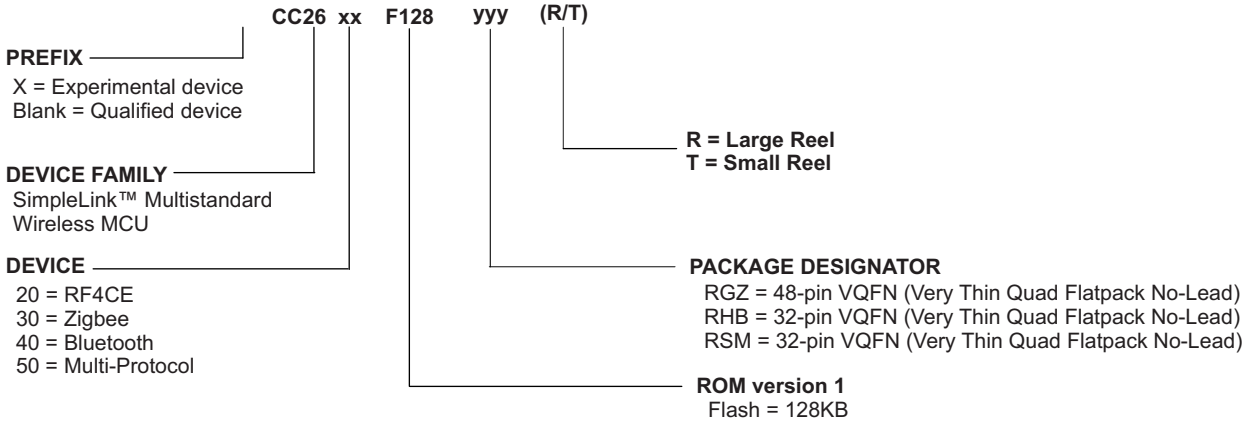


图 **8-1.** 器件命名规则

## 8.2 工具与软件

德州仪器 (TI) 提供大量的开发工具，其中包括评估处理器性能、生成代码、开发算法工具、以及完全集成和调试软件及硬件模块的工具。

以下产品支持开发 CC2630 器件 应用的开发提供支持：

**软件工具：**

SmartRF Studio 7:

SmartRF Studio 是一款 PC 应用程序，可帮助无线电系统设计人员评估早期设计过程的 RF-IC。

- 测试无线数据包收发功能，连续波收发功能
- 将相关数据写入支持的评估板或调试器，评估定制板上的 RF 性能
- 可以不搭配任何硬件使用，但此时只能生成、编辑并导出无线配置设置
- 可与德州仪器 (TI) CCxxxx 系列 RF-IC 的多款开发套件搭配使用

Sensor Controller Studio：

Sensor Controller Studio 为 CC26xx 传感器控制器提供开发环境。此传感器控制器是 CC26xx 系列中的一款专用功率优化型 CPU，可独立于系统 CPU 状态自主执行简单的后台任务。

- 允许使用 C 语言这类编程语言实现传感器控制器任务算法
- 输出传感器控制器接口驱动程序，其中整合了生成的传感器控制器机械代码和相关定义
- 通过使用集成传感器控制器任务测试和调试功能实现快速开发这有助于实现有效的传感器数据和算法验证可视化。

**IDE 和编译器：**

Code Composer Studio：

- 带有项目管理工具和编辑器的集成开发环境
- Code Composer Studio (CCS) 7.0 及更高版本内置对 CC26xx 系列器件的支持功能
- 优先支持的 XDS 调试器：XDS100v3、XDS110 和 XDS200
- 与 TI-RTOS 高度集成，支持 TI-RTOS 对象视图

IAR ARM Embedded Workbench

- 带有项目管理工具和编辑器的集成开发环境
- IAR EWARM 7.80.1 及更高版本内置对 CC26xx 系列器件的支持功能
- 广泛的调试器支持，支持 XDS100v3、XDS200、IAR I-Jet 和 Segger J-Link
- 带有项目管理工具和编辑器的集成开发环境
- 适用于 TI-RTOS 的 RTOS 插件

要获取有关 CC2630 平台的开发支持工具的完整列表，请访问德州仪器 (TI) 网站 www.ti.com。有关定价和购买信息，请联系最近的 TI 销售办事处或授权分销商。


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## 8.3 文档支持

如需接收文档更新通知，请访问 ti.com 网站上的器件产品文件夹 (**CC2630**)。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

下面列出了描述 CC2630 器件、相关外设和其他技术材料的最新文档。

技术参考手册

***《CC13xx、CC26xx SimpleLink™ 无线 MCU 技术参考手册》***

***《CC26xx SimpleLink™ 无线 MCU 勘误表》***

勘误

***《CC2630 和 CC2650 SimpleLink™ 无线 MCU 勘误表》***

## 8.4 德州仪器 (TI) 低功耗射频网站

德州仪器 (TI) 的低功耗射频网站提供所有最新产品、应用和设计笔记、FAQ 部分、新闻资讯以及活动更新。请访问 www.ti.com.cn/lprf。

## 8.5 低功耗射频电子新闻简报

通过低功耗射频电子新闻简报，您能够了解到最新的产品、新闻稿、开发者相关新闻以及关于德州仪器 (TI) 低功耗射频产品其它新闻和活动。低功耗射频电子新闻简报文章包含可获取更多在线信息的链接。

访问：www.ti.com.cn/lprfnewsletter 立即注册

## 8.6 社区资源

**下列链接提供到 TI 社区资源的连接。 链接的内容由各个分销商“按照原样”提供。 这些内容并不构成 TI 技术规范和标准且不一定反映 TI 的观点；请见 TI 的使用条款。**

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**TI 嵌入式处理器维基网页** *德州仪器 (TI) 嵌入式处理器维基网站*。此网站的建立是为了帮助开发人员从德州仪器 (TI) 的嵌入式处理器入门并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

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- 论坛、视频和博客
- 射频设计帮助
- E2E 交流互动

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- 射频电路、低功耗射频和ZigBee 设计服务
- 低功耗射频和 ZigBee 模块解决方案以及开发工具
- 射频认证服务和射频电路制造

如果需要有关模块、工程服务或开发工具的帮助：

请搜索低功耗射频开发者网络查找适合的合作伙伴。www.ti.com.cn/lprfnetwork

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## 8.7 其他信息

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此外，德州仪器 (TI) 还提供广泛的相关支持，例如开发工具、技术文档、参考设计、应用专业技术、客户支持、第三方服务以及大学计划。

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凭借丰富的供选产品解决方案、可实现的最终应用以及广泛的技术支持，德州仪器 (TI) 能够为您提供最全面的低功耗射频产品组合。

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CoreMark is a registered trademark of Embedded Microprocessor Benchmark Consortium.
IAR Embedded Workbench is a registered trademark of IAR Systems AB.
IEEE Std 1241 is a trademark of Institute of Electrical and Electronics Engineers, Incorporated.
ZigBee is a registered trademark of ZigBee Alliance, Inc.
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## 8.9 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 8.10 出口管制提示

接收方同意：如果美国或其他适用法律限制或禁止将通过非披露义务的披露方获得的任何产品或技术数据（其中包括软件）（见美国、欧盟和其他出口管理条例之定义）、或者其他适用国家条例限制的任何受管制产品或此项技术的任何直接产品出口或再出口至任何目的地，那么在没有事先获得美国商务部和其他相关政府机构授权的情况下，接收方不得在知情的情况下，以直接或间接的方式将其出口。

## 8.11 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

# 9 机械、封装和可订购信息

## 9.1 封装信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。


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# 重要声明

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CC2630F128RGZR | ACTIVE | VQFN | RGZ | 48 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | CC2630 F128 | Samples |
| CC2630F128RGZT | ACTIVE | VQFN | RGZ | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | CC2630 F128 | Samples |
| CC2630F128RHBR | ACTIVE | VQFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC2630 F128 | Samples |
| CC2630F128RHBT | ACTIVE | VQFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC2630 F128 | Samples |
| CC2630F128RSMR | ACTIVE | VQFN | RSM | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | CC2630 F128 | Samples |
| CC2630F128RSMT | ACTIVE | VQFN | RSM | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | CC2630 F128 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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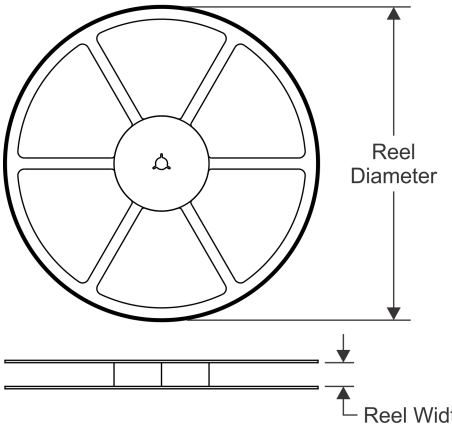
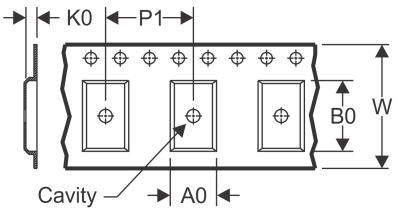
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

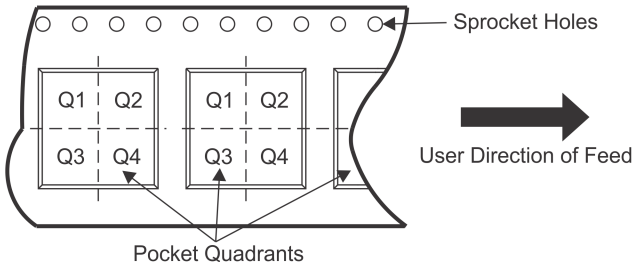



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

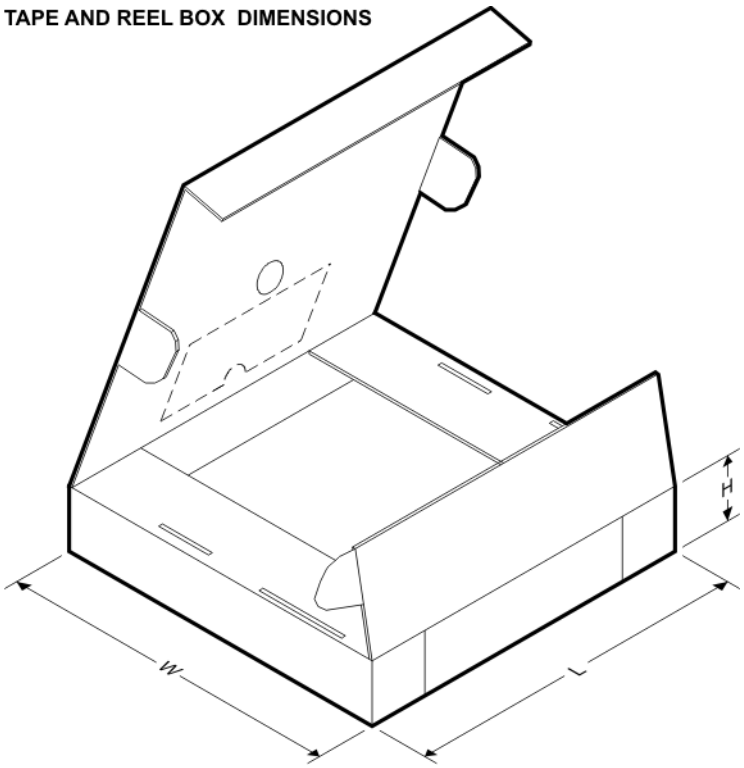
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CC2630F128RGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| CC2630F128RGZT | VQFN | RGZ | 48 | 250 | 180.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| CC2630F128RHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| CC2630F128RHBT | VQFN | RHB | 32 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| CC2630F128RSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| CC2630F128RSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

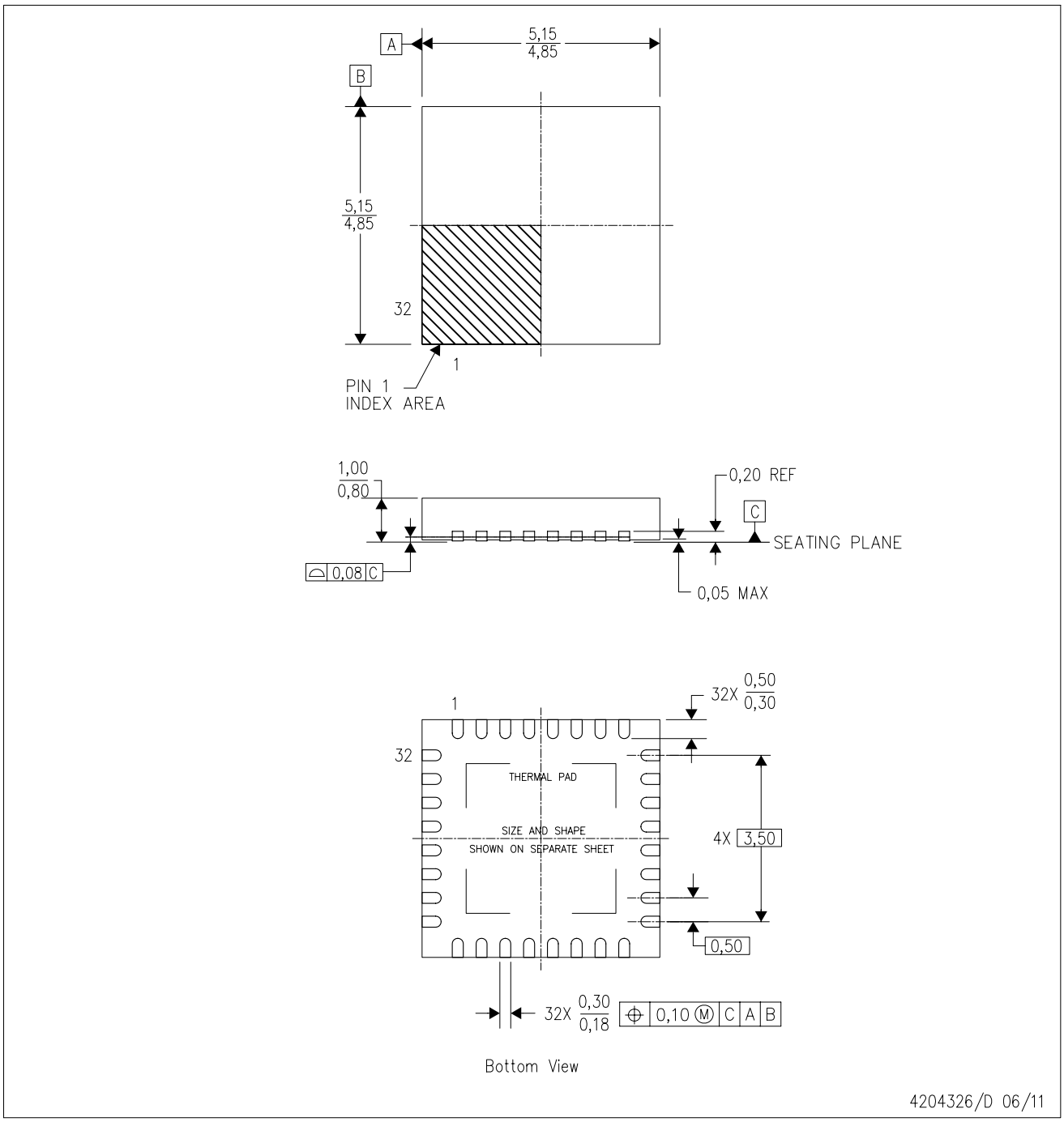
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CC2630F128RGZR | VQFN | RGZ | 48 | 2500 | 367.0 | 367.0 | 38.0 |
| CC2630F128RGZT | VQFN | RGZ | 48 | 250 | 210.0 | 185.0 | 35.0 |
| CC2630F128RHBR | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| CC2630F128RHBT | VQFN | RHB | 32 | 250 | 210.0 | 185.0 | 35.0 |
| CC2630F128RSMR | VQFN | RSM | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| CC2630F128RSMT | VQFN | RSM | 32 | 250 | 210.0 | 185.0 | 35.0 |

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

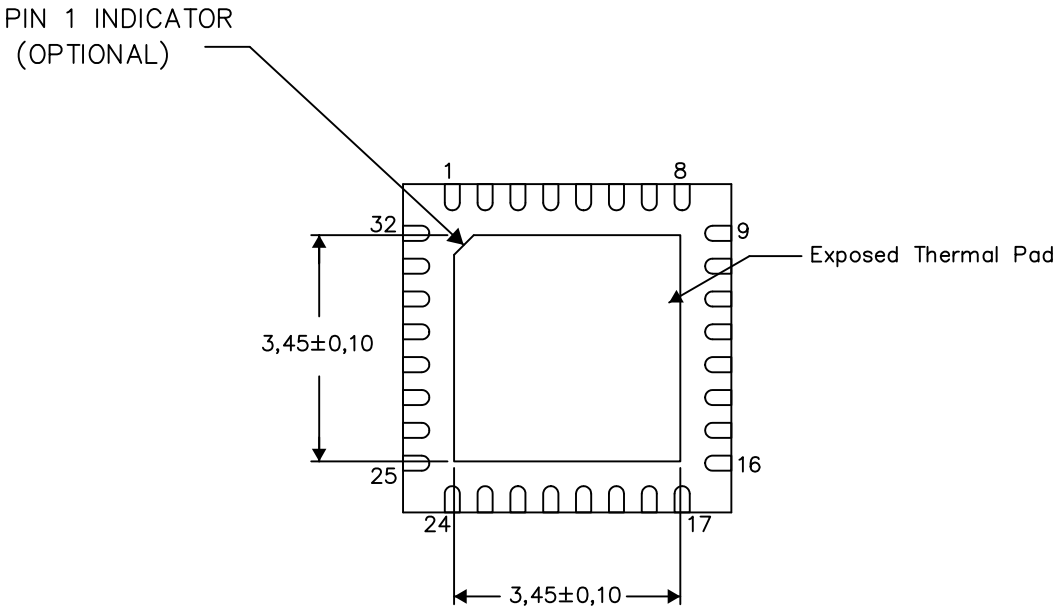
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



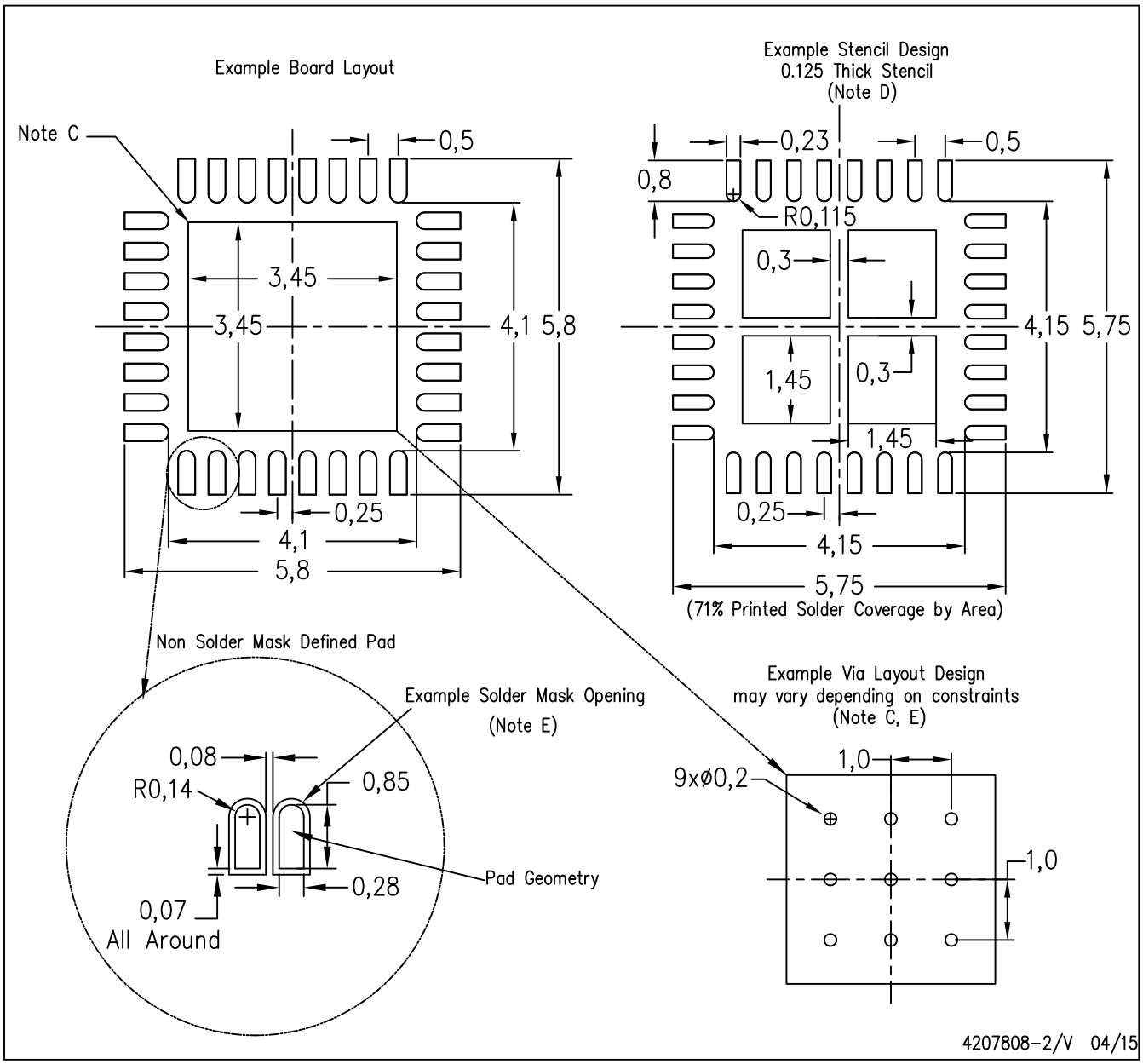

Bottom View

Exposed Thermal Pad Dimensions

4206356–2/AC 05/15

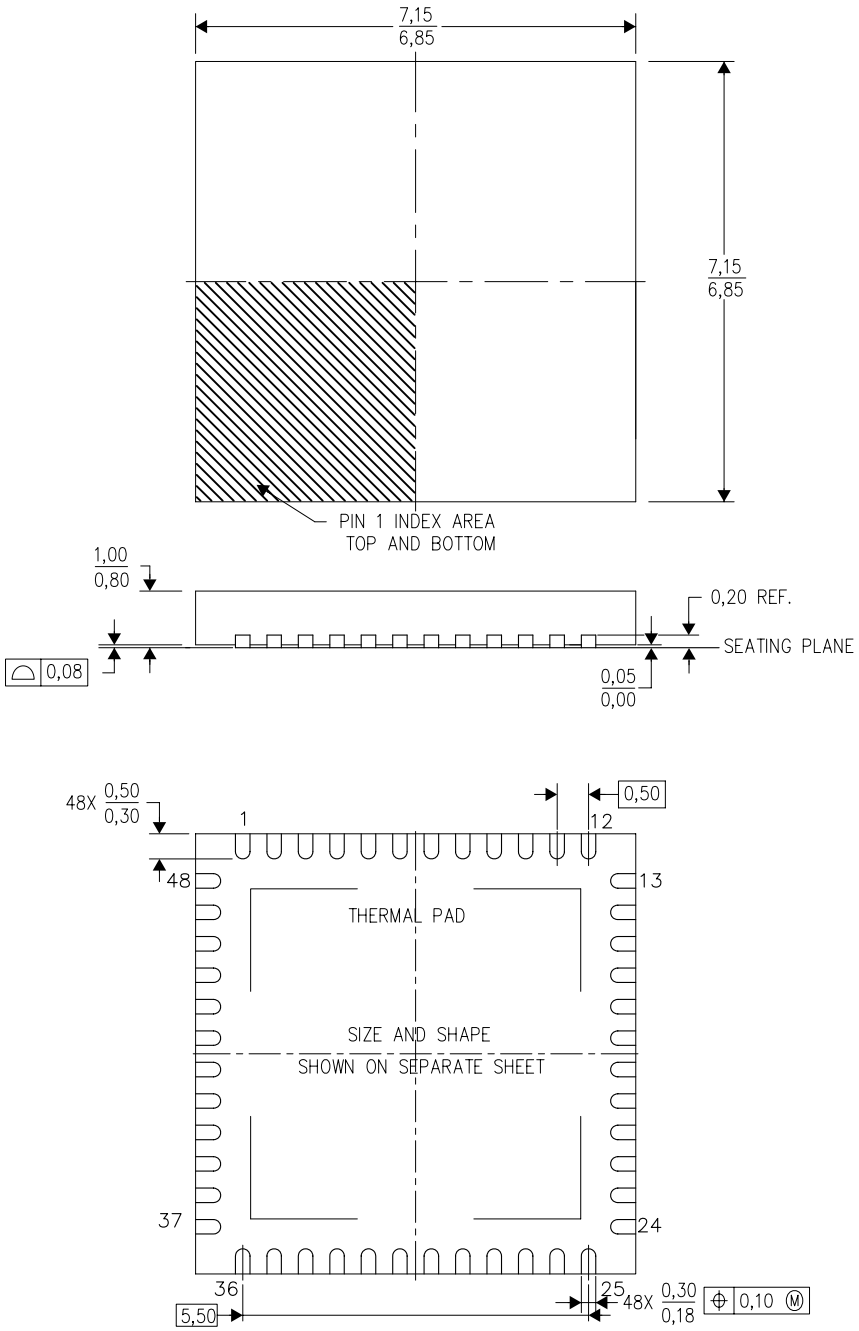
NOTE: A. All linear dimensions are in millimeters

# RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

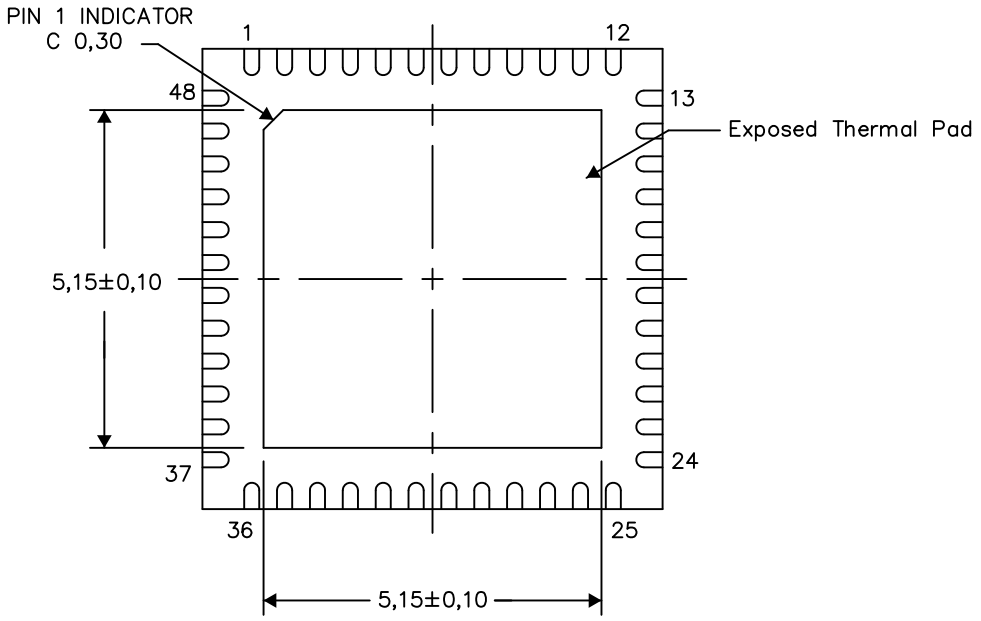
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



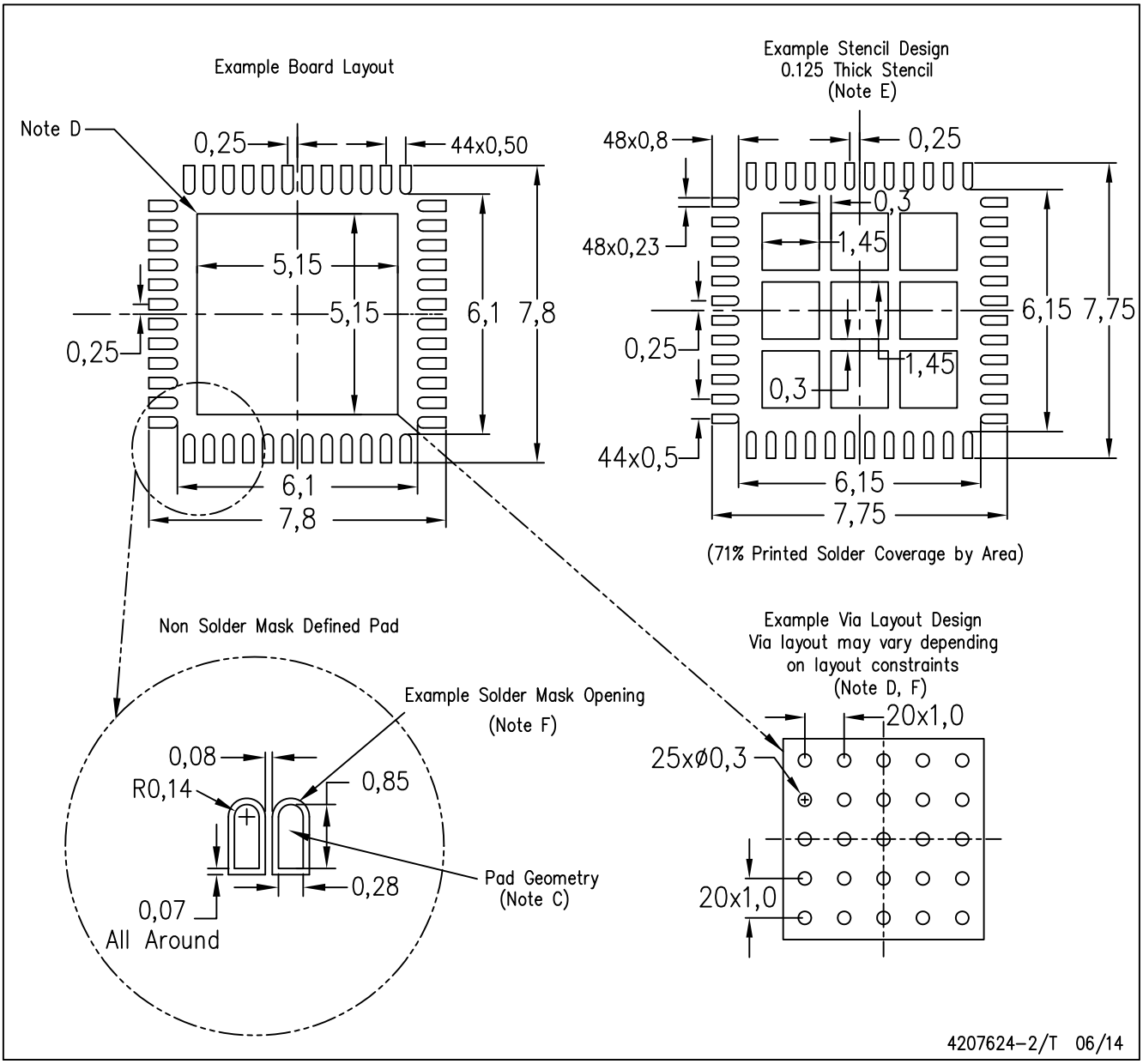

Bottom View

Exposed Thermal Pad Dimensions

4206354–2/Z 03/15

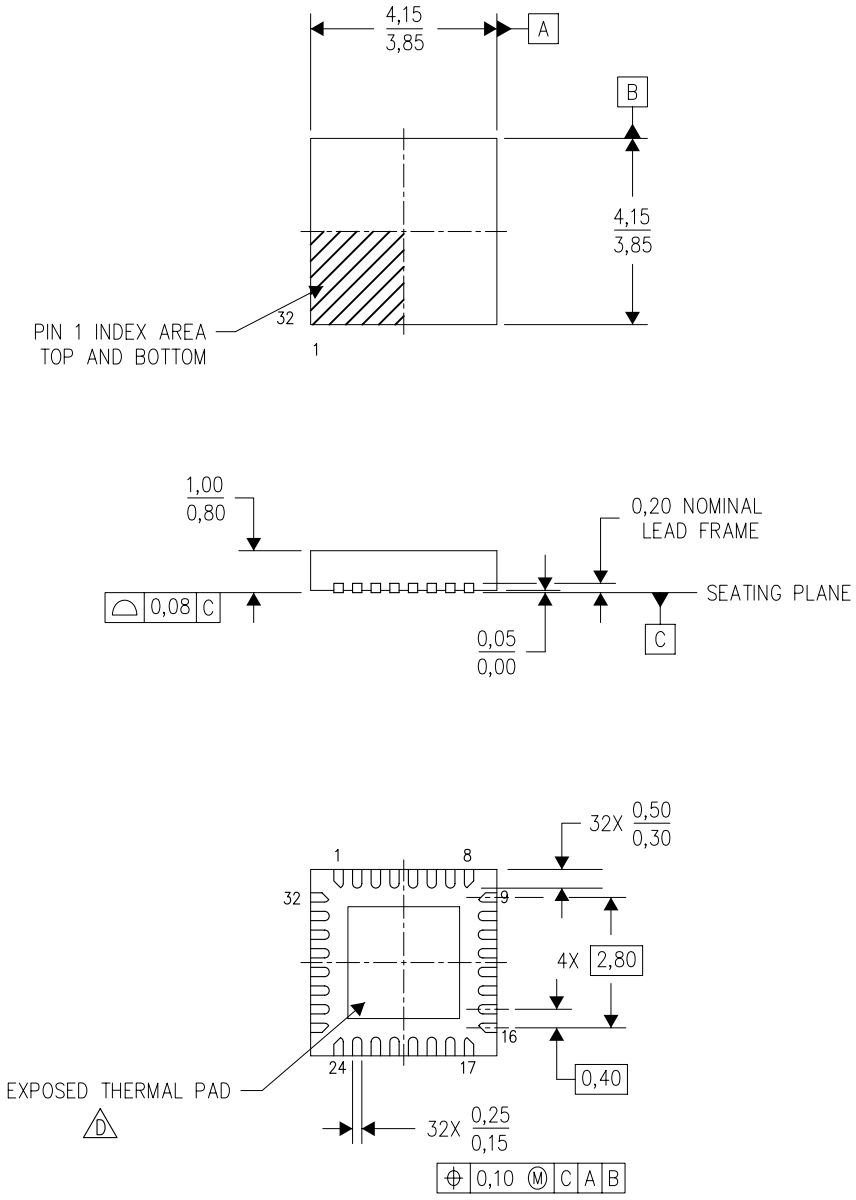
NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD




4207560/B 03/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

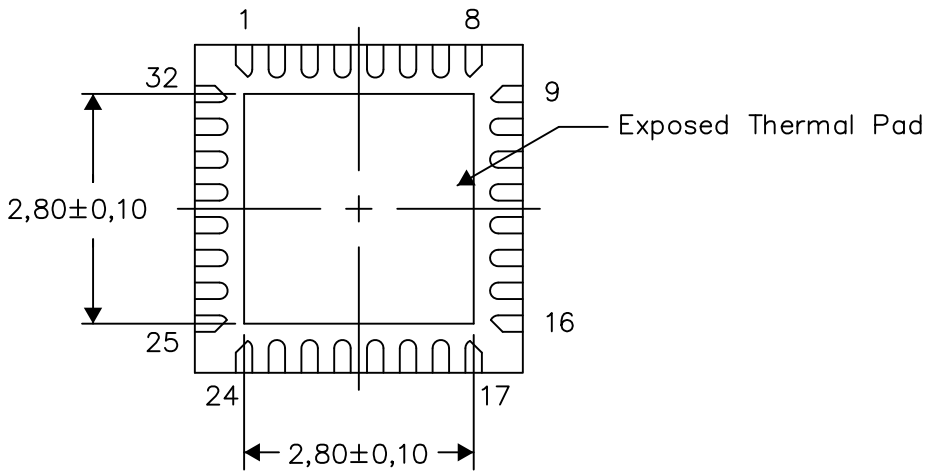
RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



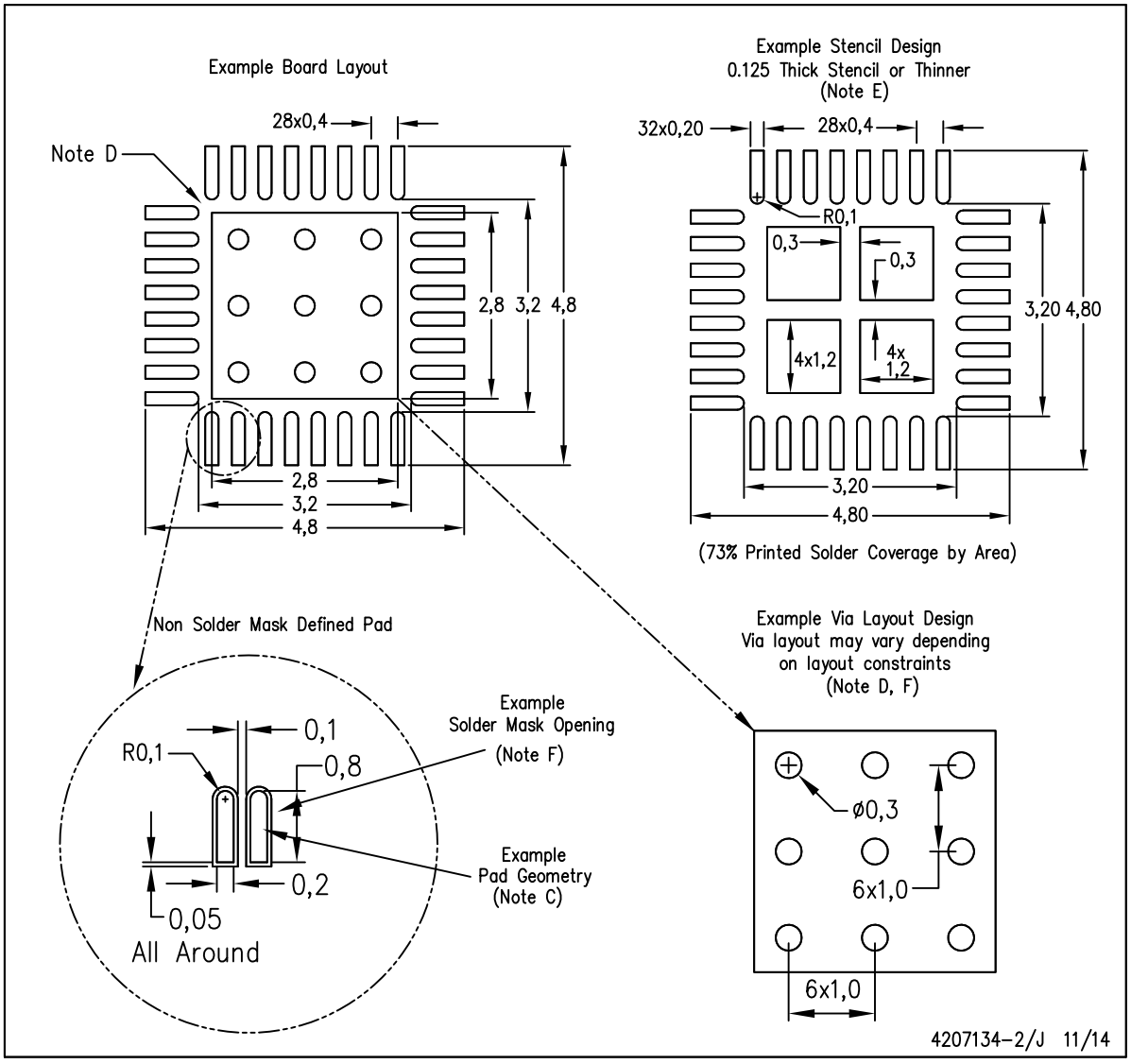

Bottom View

Exposed Thermal Pad Dimensions

4207868–2/I 07/14

NOTE: All linear dimensions are in millimeters

## RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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